Capacitor-Free Event-Based Asynchronous Digital LDO Regulator with 99.99% Current Efficiency

Ji-Hoon Song, Yeong-Hun Kim, Ho-Jin Kwark, and Kang-Yoon Lee[a]
Department of Electrical and Computer Engineering, Sungkyunkwan University
E-mail : sjh3668@g.skku.edu, skku2080@g.skku.edu, hojin131@g.skku.edu, klee@skku.edu

***Abstract* - This paper proposes a high-performance digital low-dropout regulator (DLDO) for wearable devices and IoT applications. The proposed DLDO circuit design provides fast stability and low power consumption using a PID controller and event-driven digital feedback control. The circuit utilizes a high-speed Flash-SAR ADC to feedback on the output, enabling real-time adjustment of the PID controller parameters to quickly adapt to external environmental changes and achieve a fast settling time. The proposed event-driven method minimizes circuit operation to reduce power consumption. Additionally, the limit-cycle oscillation typically occurring in the steady state is suppressed, thereby reducing output voltage ripple.**

The circuit is fabricated using a 55-nm CMOS process, with a chip area of 1800 x 1820 um². The proposed design supports an input voltage range of 0.5 – 1.2 V and an output voltage range of 0.4 – 1 V. It achieves a fast-settling time of 252 ns and a low current consumption of 1.7 µA at a 50MHz operating frequency. The peak current efficiency is 99.99%, with a maximum load current of 70 mA. The load regulation is 0.13 mV/mA, and the line regulation is 0.01 V/V.

***Keywords*— Event-Based Asynchronous Design, Digital Low-Dropout Regulator (DLDO), Dynamic Voltage Frequency Scaling (DVFS)**

I. INTRODUCTION

Recently, as the use of wireless electronic devices, such as Radio-Frequency Identification (RFID) and medical implants, has increased, communication between devices, the cloud, and other devices has also expanded, driving the active research and development of the Internet of Things (IoT) technology. Wireless electronic devices require diverse functionalities, such as eliminating external capacitors in compact integrated areas while maintaining high power efficiency. [1]

All wireless devices operate with limited-size batteries. As a result, wearable devices must function at low power, enabling fast wireless communication while minimizing weight. In recent years, research has actively focused on achieving efficient System-on-Chip (SoC) operation, even with the limitations of wearable devices, including their battery size, capacity, and power constraints. [2]

To extend the operating time of devices in constrained environments, it is essential to provide the required power consumption without frequent charging. Thus, low-power wireless device systems are crucial for achieving optimal operation in IoT applications. To ensure high power efficiency in wireless devices, it is necessary to minimize the power consumption and area of all circuit components.

The analog low-dropout regulator (LDO), which supplies appropriate operating voltages to complex systems with multiple sensors, has been widely employed as an efficient method of distributing battery supply voltages [3]. However, due to the limitations of conventional power management circuits, including the lightweight nature of wearable devices and the rapid pace of wireless communication, low power-supply voltages reduce the response speed of analog LDOs. This results in system-wide performance degradation due to external noise and other factors [4]. Consequently, ongoing research aims to replace the amplifier, external capacitor, and feedback loop of the analog LDO with digital designs.

Conventional DLDO regulators generally operate at low power by employing shift registers, proportional–integral (PI) structures, and proportional–differential (PD) structures. However, a power consumption issue persists due to the clock operation of each controller. Additionally, because of digital compensation, a ripple phenomenon occurs in DLDOs, resulting in periodic fluctuations in the output voltage. [5]

Previous studies aimed at correcting significant voltage differences have employed coarse tuning initially, followed by fine-tuning or hybrid methods. Alternatively, the arrangement of the positive MOSFET (PMOS) in the DLDO can be modified by adjusting the parameter values of the proportional–integral–derivative (PID) controller based on four external states using the PID method. [6] Furthermore, an event-driven method can be utilized to stop the clock of the controller (shift register) when the voltage enters a dead zone. [7]

This paper presents a design that utilizes a CMOS Pass Transistor Array to achieve a wide output voltage range, ensuring flexibility in various operating conditions. A PID controller and a droop detector are incorporated into the design, enabling the system to respond rapidly to fluctuations in the output voltage, thereby enhancing overall

a. Corresponding author; klee@skku.edu

Manuscript Received Jan. 2, 2025, Revised Mar. 17, 2025, Accepted Mar. 25, 2025

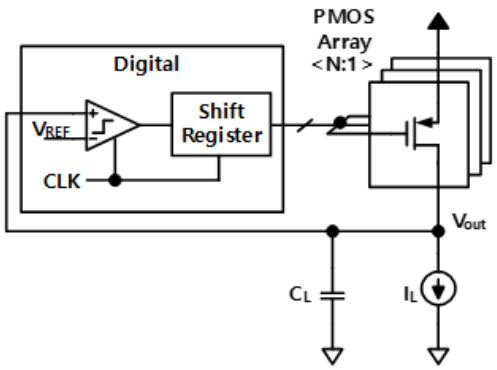

Fig. 1. Conventional DLDO Structure.

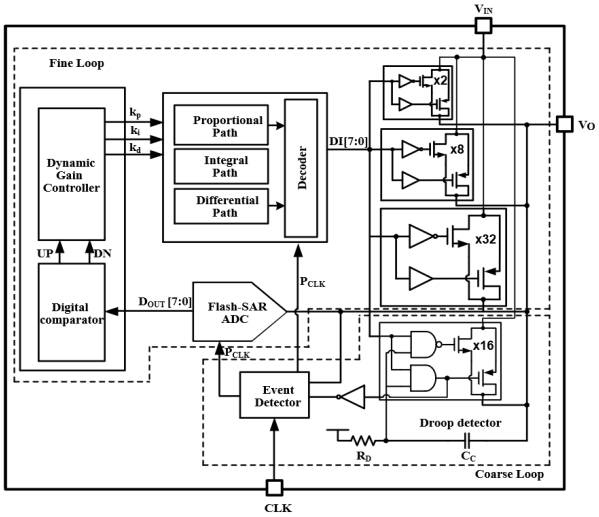

Fig. 2. Top block diagram of the proposed DLDO

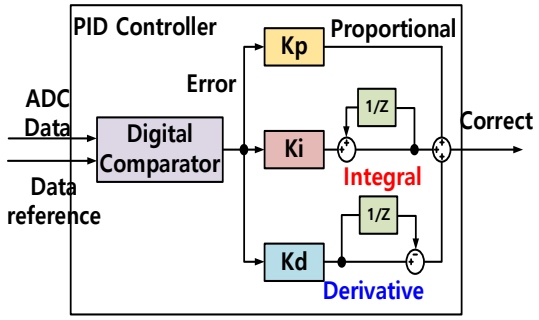

Fig. 3. PID structure.

performance and stability. Furthermore, an event-driven operating method is introduced to minimize power consumption during steady-state operation. By reducing unnecessary circuit activity, this approach significantly improves energy efficiency, making the design well-suited for low-power applications such as wearable devices and IoT systems.

II. PROPOSED DIGITAL LOW DROP OUT STRUCTURE

A. Conventional DLDO Architecture

Fig. 1 illustrates the block diagram of the basic structure of the DLDO. Unlike conventional designs that use an analog error amplifier, the DLDO employs a multi-bit analog-to-digital converter (ADC) and a comparator to determine the error between the output voltage and the target voltage. Additionally, it incorporates a shift register to regulate the supply current based on the calculated error.

As illustrated in Fig. 1, a clock is utilized to achieve higher frequency and faster response speed. However, in the case of DLDO, when a comparator periodically compares the target voltage with the supply voltage, operating at a lower frequency can result in extended response delay and increased error. Conversely, operating at a higher frequency leads to increased power consumption. Additionally, there is a potential risk of limit cycle oscillation, where a specific voltage value repeatedly occurs under steady-state conditions.

B. Proposed Top Architecture

The first component in the operation of the circuit is the ADC. As shown in Fig. 2, the ADC receives the V_out value, compares it with the target voltage, and computes the error within the dynamic gain control. Based on the error value and its differential, the corresponding parameter value is output. These output parameters influence the PID output, which quickly transfers a stable output value to the CMOS array.

The PID output is a digital code that activates the CMOS Pass Transistor, which affects the output current and voltage. When the voltage deviates from a specific target voltage range, an event is triggered, activating the clock in the dynamic gain control block and the ADC. When the voltage is within the target range, the clock is stopped to reduce power consumption and ripple phenomena. Otherwise, the dynamic gain controller generates a voltage output closer to the target voltage.

C. PID Controller

The PID controller is composed of proportional–integral–derivative operations (Fig. 3). It is in the form of a feedback loop that operates by receiving the object output value as an input. Specifically, the error is calculated by comparing the desired reference value with the input ADC value, and the calibration value of the object to be controlled is output by adding each PID operation. A type-III PID controller was adopted to compensate for the DLDO system.

The output MV value (operation variable) of a general type-III PID controller can be expressed using Equation (1).

$$MV(t) = K_p e(t) + K_i \int_0^t e(t)dt + K_d \frac{de}{dt} \quad (1)$$

K_p , K_i , and K_d are the proportional, integral, and derivative parameters, respectively. $e(t)$ denotes an error value, as shown in Equation (2).

$$e(t) = V_{ref} - V_{ADC} \quad (2)$$

V_{ref} is the reference voltage of the target and V_{ADC} is the voltage of the ADC data. Both voltage values are digital in this study.

TABLE I. SAR-ADC Performance Summary

Parameter	Value
Supply Voltage (V)	0.5 – 1.2
Input Range (V_{pp})	0.5 – 1.2
Sampling Rate (Sample/Sec)	5M
Number of Bits (Bits)	8
Clock Frequency (MHz)	50
Current Consumption (Enable Low State)	53.6 – 94.9
Current Consumption (Enable High State)	7.6 – 13.0
ENOB (Bit)	7.49

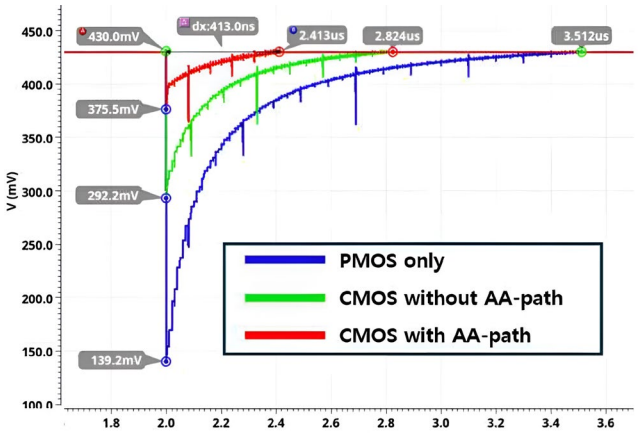

Fig. 4. Load transient result comparison with Pass Transistor and AA-Path

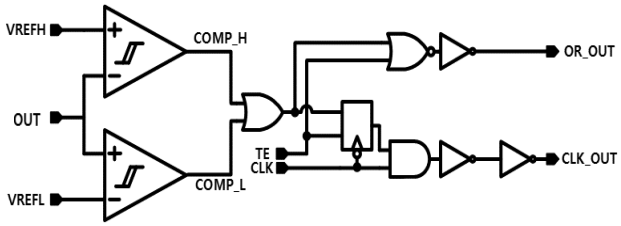

Fig. 5. Block diagram of event detector.

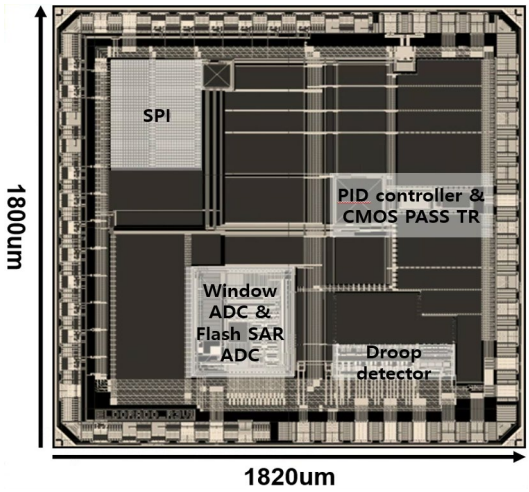

Fig. 6. Microphotograph of the proposed DLDO

Table I presents the performance summary of the SAR ADC. When operating with a 0.7 V supply voltage and an external clock frequency of 10 MHz, the average power consumption is 5.3 μW. All blocks are designed to support and enable control operation for low-power consumption. The designed ADC operates within a supply voltage range of 0.5 V to 1.2 V and features an 8-bit resolution.

D. CMOS Pass Transistor & Droop Detector

The proposed DLDO incorporates both PMOS and NMOS Pass Transistors, enabling a wide output voltage regulation range. This extended output voltage range allows the DLDO to be applied to a variety of supply voltages, making it suitable for diverse wearable and IoT applications, which often require different voltage levels to power various components. Furthermore, the design integrates a NAND-based droop detector analog assist path, which significantly enhances the output response speed by operating independently of the system's clock. This approach not only improves performance but also reduces the power consumption associated with clock-driven operations. Additionally, compared to the conventional AA-path, the new design reduces the coupling capacitor value, contributing to a more compact and efficient solution while maintaining reliable operation.

Fig. 4 compares the load transient results of the DLDO using only PMOS Pass Transistors, DLDO using CMOS Pass Transistors, and DLDO with an added AA-path, when the output current is increased from 5mA to 20mA. The DLDO using only PMOS Pass Transistors shows a drop in output voltage of around 300mV. In contrast, the DLDO using CMOS Pass Transistors demonstrates an improvement over the PMOS-only configuration due to the influence of NMOS. The DLDO with the NAND-based AA-path exhibits the fastest response to changes in output current, showing the least voltage variation. These results confirm that the addition of the AA-path enables a faster settling time in response to changes in output current.

E. Event Detector

Fig. 5 illustrates the block diagram of the event detector, which is responsible for determining whether the output voltage is within the desired range. When the output voltage falls within the VREFH and VREFL range (referred to as the dead zone), it is classified as "no event," and the system remains in a steady state. In this steady state, the operation of the feedback loop is halted, effectively preventing the limit cycle oscillation (LCO) which is a common issue in conventional DLDO circuits. By stopping the feedback loop, the circuit reduces unnecessary power consumption, which is typically caused by continuous clock operation. Furthermore, by turning off the clock-based circuit, the current efficiency is maximized, as there is minimal power dissipation from clock-driven components. This method ensures a more efficient and stable operation, especially when the system is not actively adjusting to changes in output voltage.

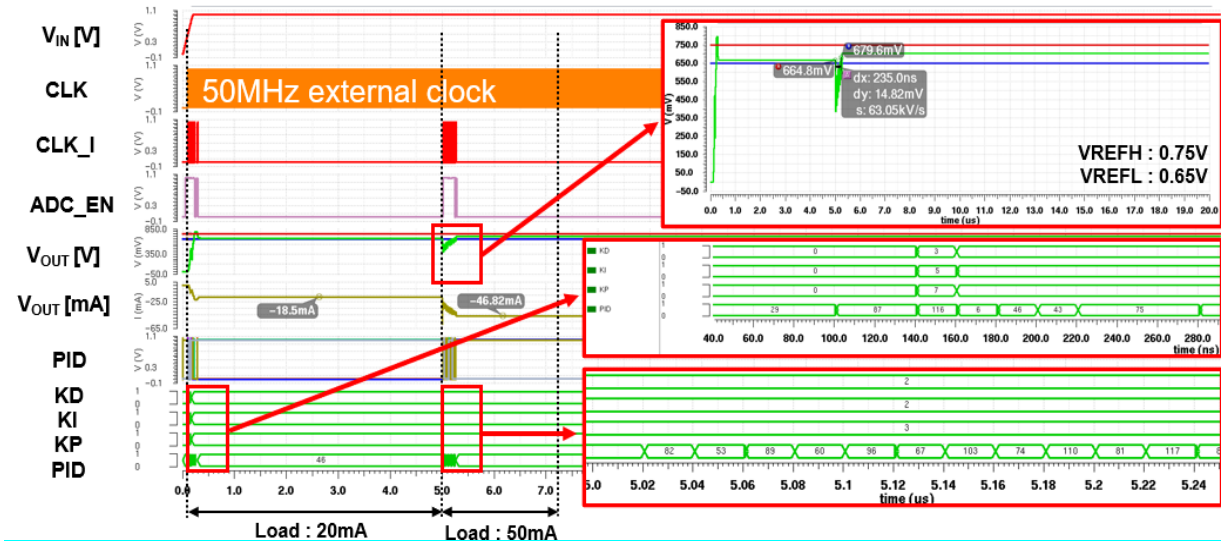

Fig. 7. Simulation result of Proposed DLDO

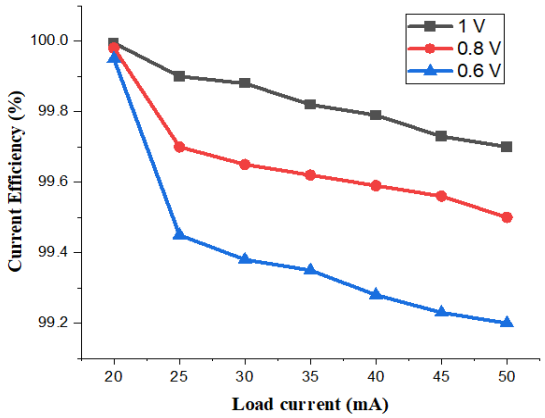

Fig. 8. Peak current efficiency of proposed DLDO

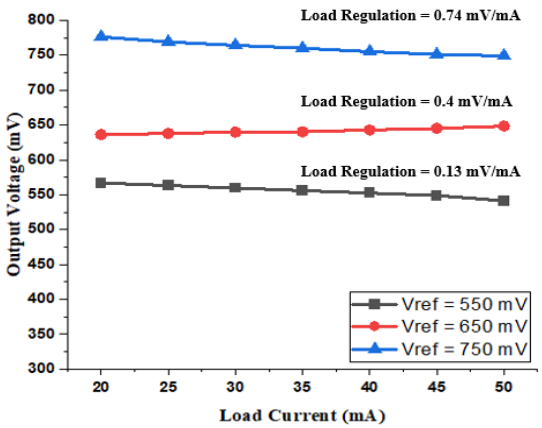

Fig. 9. Load regulation result of proposed DLDO

III. SIMULATION AND MEASUREMENT RESULTS

The chip was fabricated using a 55nm CMOS process, featuring a single polysilicon layer, six metal layers, MIM capacitors, and high-resistance polysilicon resistors. Fig. 6 shows a microphotograph of the DLDO. The active area is 1800 × 1820 um².

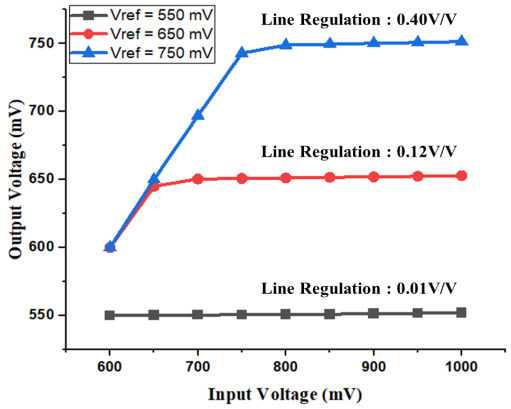

Fig. 10. Line regulation result of proposed DLDO

Fig. 7 shows the simulation of the proposed DLDO design. In this simulation, the output voltage is higher than VREFH = 0.65 V and lower than VREFL = 0.75 V, so the oscillator's clock is activated, and the ADC block and dynamic gain control block operate. When the output voltage remains within the target voltage range (VREFL = 0.65 V–VREFH = 0.75 V) for a certain period, the event detector stops operating. The simulation confirmed that the clock of the dynamic gain control block and ADC block stops, and the feedback loop operation halts. This event-driven method reduces power consumption and digital compensation ripple. Once the target voltage is reached, the clock is turned off, and the operation stops.

We performed a simulation where the load current starts at 20 mA and increases to 50 mA over time. The settling time was 235 ns, and the current consumption was 1.78 µA. The load regulation was 0.49 mV/mA. When the load current exceeds 50 mA, there is no external capacitor, so the output voltage drop becomes more severe as the load current increases. However, by implementing a PID controller, rapid correction can be achieved, ensuring a fast transient response.

Fig. 8 shows the measurement results of current efficiency according to the change in load current. The DLDO current efficiency was measured starting from an input voltage of 0.6 V and increasing by 0.2 V up to 1 V.

TABLE II. Performance Summary

Parameter	This work	[1]	[8]
Clock Frequency (MHz)	50 - 200	10	10
Process (nm)	55	28	55
Supply Voltage (V)	0.5–1.2	0.5–1.0	0.8–1.5
Output Voltage (V)	0.4–1	0.45–0.95	0.756–1.456
Quiescent Current (μA)	1.7	3.7	-
Max Load Current (mA)	70	40	10
Settling Time(μs)	0.252	0.350	0.33
Peak Current Efficiency (%)	99.995	99.97	95.14
Load Regulation (mV/mA)	0.13	2.2	2.3

As shown in Fig. 8, the highest current efficiencies are observed at 20 mA load current. Additionally, when the input voltages are 0.6 V, 0.8 V, and 1 V, high efficiencies of 99.95%, 99.98%, and 99.995% were measured, respectively.

Fig. 9 and 10 present the load and line regulation measurement results for the proposed DLDO. To calculate load regulation, the output voltage values are determined by varying the load current. As shown in Fig. 10, the measurements were taken at three different reference voltages. The lowest load regulation value measured at a 550-mV reference voltage was 0.13 mV/mA, while the highest value at 750 mV reached 0.74 mV/mA. For line regulation, the output voltage is measured as the input voltage is varied, with three distinct reference voltages used in the process.

Table II highlights the performance characteristics of the proposed DLDO.

As shown in Fig. 9, the line regulation of the proposed DLDO has been measured across a range of input voltages from 600 mV to 1 V. The results indicate that the minimum line regulation occurs at a reference voltage of 550 mV, with a value of 0.01 V/V. This suggests a very stable output voltage in response to small changes in the input voltage under low reference voltage conditions. On the other hand, the maximum line regulation occurs at a reference voltage of 750 mV, where the line regulation value is 0.40 V/V. This demonstrates that, while the output voltage remains stable, higher input voltages result in greater sensitivity to changes in input, though still maintaining a reasonable level of performance. The measured range of input voltage reflects the system's ability to handle variations in supply voltage effectively while delivering consistent output.

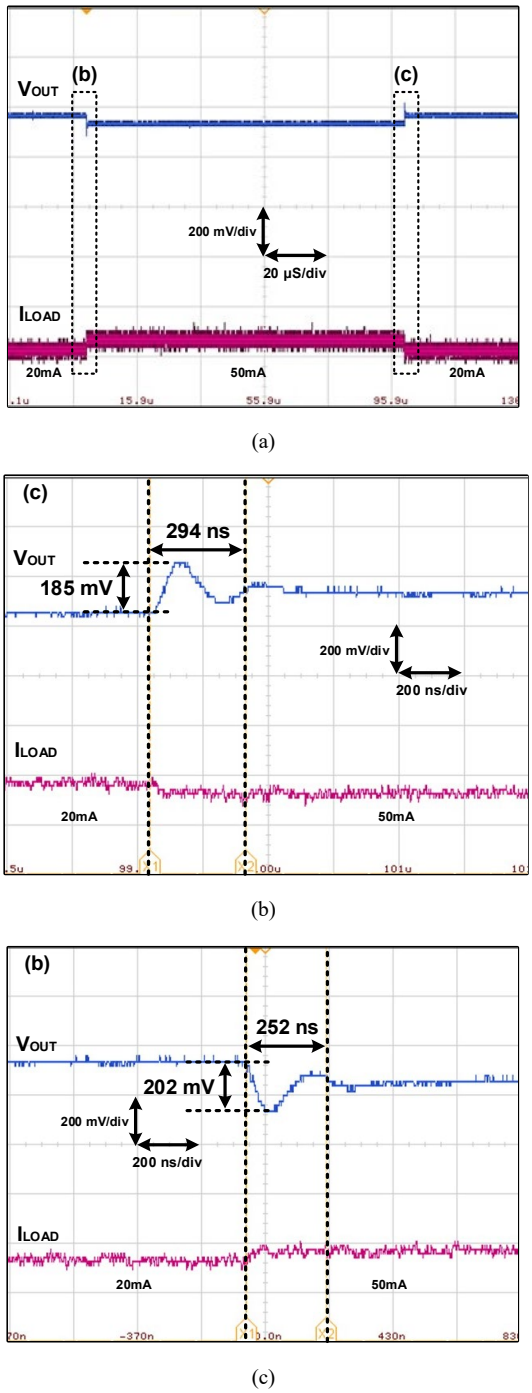

Fig. 11. (a) Minimum settling time for condition, (b) Change the load current from 20 mA to 50 mA, and (c) Change the load current from 50 mA to 20 mA.

Fig. 11 illustrates the minimum settling time of the proposed DLDO regulator under specific conditions. In this case, the input voltage is set to 1 V. The measurement was conducted by changing the load current from 20 mA to 50 mA, while maintaining a target output voltage of 650 mV. The results show that the minimum time required for the system to stabilize and reach the target voltage is 252 ns. This indicates the fast transient response of the DLDO, demonstrating its ability to quickly adapt to load variations while maintaining stable output performance.

IV. CONCLUSION

In this paper, we proposed a DLDO feedback control architecture with a dynamic-gain controller and an event-driven method for low-power and fast stability voltage control. The DLDO architecture, which includes an asynchronous self-triggering event-driven method, reduces the total operating power consumption due to load current variations compared to previous DLDO designs. Additionally, the event-driven method helps decrease the output voltage ripple and power consumption caused by the clock.

Furthermore, a PID controller was applied to generate a fast response time and precise output voltage, and CMOS PASS transistors were utilized to achieve a wide output voltage range. The proposed DLDO with a dynamic-gain controller was designed using a 55-nm CMOS process. The chip area was 1800 x 1820 um^2, though the actual active area was smaller. The transient response time was approximately 252 ns, and the quiescent current was 1.7 uA. The measured peak current efficiency was 99.99%, with zero output voltage ripple. The measured load regulation was 0.13 mV/mA, and the line regulation was 0.01 V/V.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

REFERENCES

[1] M. Asif et al., "A High Performance Adaptive Digital LDO Regulator With Dithering and Dynamic Frequency Scaling for IoT Applications," in IEEE Access, vol. 8, pp. 132200-132211, 2020

[2] J. -G. Kang, J. Park, M. -G. Jeong and C. Yoo, "Digital Low-Dropout Regulator With Voltage-Controlled Oscillator Based Control," in *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6951-6961, June 2022.

[3] J. Oh, Y. -H. Hwang, J. -E. Park, M. Seok and D. -K. Jeong, "An Output-Capacitor-Free Synthesizable Digital LDO Using CMP-Triggered Oscillator and Droop Detector," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 6, pp. 1769-1781, June 2023

[4] X. Ma, Y. Lu, Q. Li, W. -H. Ki and R. P. Martins, "An NMOS Digital LDO With NAND-Based Analog-Assisted Loop in 28-nm CMOS," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 11, pp. 4041-4052, Nov. 2020.

[5] Y. K. Cherivirala and D. D. Wentzloff, "A Capacitor-Less Digital LDO Regulator With Synthesizable PID Controller Achieving 99.75% Efficiency and 93.3-ps Response Time in 65 nm," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 5, pp. 1769-1773, May 2023.

[6] M. -K. Jeon, W. -J. Yoo, C. -G. Kim and C. Yoo, "A Stochastic Flash Analog-to-Digital Converter Linearized by Reference Swapping," in *IEEE Access*, vol. 5, pp. 23046-23051, 2017

[7] J. -E. Park, Y. -H. Hwang and D. -K. Jeong, "A 0.5-V Fully Synthesizable SAR ADC for On-Chip Distributed Waveform Monitors," in *IEEE Access*, vol. 7, pp. 63686-63697, 2019

[8] M. Asif et al., "Design of High Performance Hybrid Type Digital-Feedback Low Drop-Out Regulator Using SSCG Technique," in IEEE Access, vol. 9, pp. 28167-28176, 2021.

Ji Hoon Song received his B.S. degree from the Department of Semiconductor Engineering at Cheongju University, Cheongju, Korea, in 2020, where he is currently working toward the Combined Ph.D & M.S Course at School of Information and Communication Engineering, Sungkyunkwan University. His research interests include Power management IC and Analog Front End.

Yeong Hun Kim received his B.S. degree from the Department of Electronic Engineering at Suwon University, Hwaseong, Korea, in 2021, where he is currently working toward the M.S. and Ph.D. degrees in Electronics and Computer Engineering from Sungkyunkwan University, Suwon, Korea. His research interests include Power Management IC.

HoJin Kwark received his B.S. degree from the Department of Electronic Engineering at Chungnam National University, Daejeon, Korea, in 2023, He is currently working toward the M.S. course in Electronics and Computer Engineering from Sungkyunkwan University, Suwon, Korea. His research interests include ADC.

Kang-Yoon Lee received the B.S., M.S., and Ph.D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea, in 1996, 1998, and 2003, respectively.
From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, where he was a Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chip sets for W-CDMA, WLAN, and PHS. From 2005 to 2011, he was with the Department of Electronics Engineering, Konkuk University as an Associate Professor. Since 2012, he has

been with College of Information and Communication Engineering, Sungkyunkwan University, where he is currently a Professor. His research interests include the implementation of power integrated circuits, CMOS RF transceiver, analog integrated circuits, and analog/digital mixed-mode VLSI system design.