A High-Resolution Linear-Exponential Incremental Analog-to-Digital Converter With Digital Weight Compensation

Minkyu Yang[1], Changjoo Park, Jooeun Kim, Jeongmyeong Kim, Dalta Imam Maulana, and Wanyeong Jung[a]

School of Electrical Engineering, Korea Advanced Institute of Science and Technology

E-mail: {minq, wanyeong}@kaist.ac.kr

Abstract **- High-resolution analog-to-digital converters (ADCs) are essential for precise signal acquisition in applications such as medical imaging and high-quality audio systems. This paper presents a linear-exponential incremental ADC that addresses the key challenge of finite amplifier gain through a digital filter. Fabricated in a 65-nm CMOS process, the ADC achieves a peak signal-to-noise-and-distortion ratio (SNDR) of 87.3 dB and a total harmonic distortion (THD) of -101.8 dB for a 5.66 kHz input signal within an 18.75 kHz bandwidth. By compensating for analog imperfections in the digital domain, the proposed design achieves improved linearity and reliable high-resolution performance in demanding scenarios.**

Keywords— **Linear-exponential incremental ADC, digital filter, finite amplifier gain, weight optimization**

I. INTRODUCTION

Analog-to-digital converters (ADCs) are essential in modern signal processing systems, particularly in applications demanding high precision, such as medical imaging and high-quality audio. Among various ADC architectures, incremental ADCs have gained significant attention due to their ability to achieve high resolution through oversampling and straightforward digital filtering. These attributes make incremental ADCs well-suited for scenarios where high signal-to-noise ratio (SNR) and linearity are critical.

Incremental ADCs operate by using an oversampling approach combined with a straightforward digital filtering mechanism. As shown in Fig. 1, they are implemented using a delta-sigma modulation (DSM) system and a digital filter. The DSM system comprises an integrator, a comparator, and a digital feedback loop, which collectively perform signal integration and quantization noise suppression. During each oversampling period, the integrator accumulates the input signal, and the digital filter accumulates the comparator output to generate the final digital output. The inherent simplicity of this structure facilitates high-resolution performance while maintaining low design complexity.

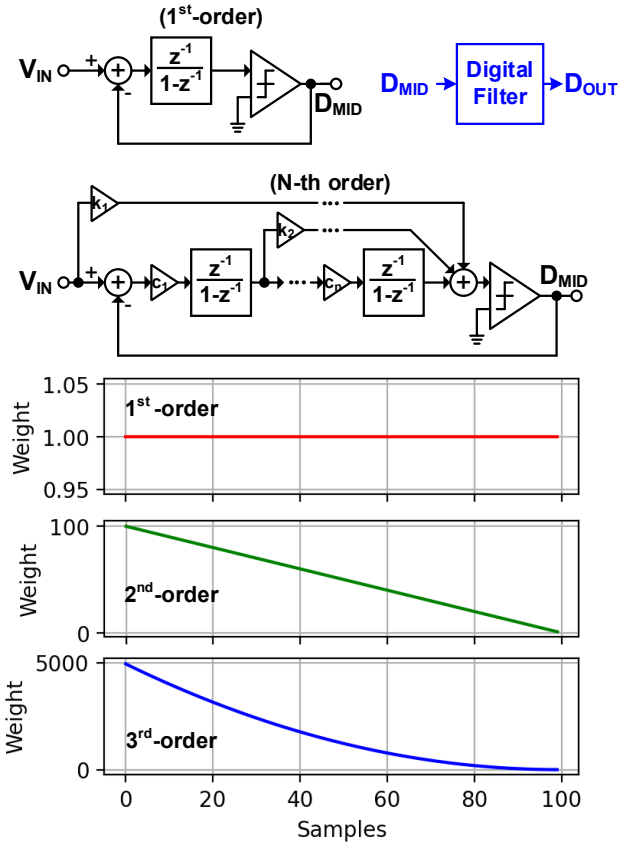


Fig. 1. The architecture of the prior incremental ADCs and their weighting trends.

To further improve performance, incremental ADCs can adopt high-order architectures by increasing the order of the integrator [1],[2]. In these designs, multiple integration stages attenuate quantization noise more effectively across the oversampling period. However, higher-order architectures introduce non-uniform signal weighting, where earlier samples contribute more heavily to the final output (Fig. 1 bottom). This uneven weighting improves SQNR performance but disturbs the noise averaging effect between samples, leading to a thermal noise penalty and greater sensitivity to circuit non-idealities [3].

To overcome these limitations, the linear-exponential incremental ADC [4] combines the noise characteristics of

a. Corresponding author; wanyeong@kaist.ac.kr

Manuscript Received Dec. 26, 2024, Revised Apr. 21, 2025, Accepted May 12, 2025

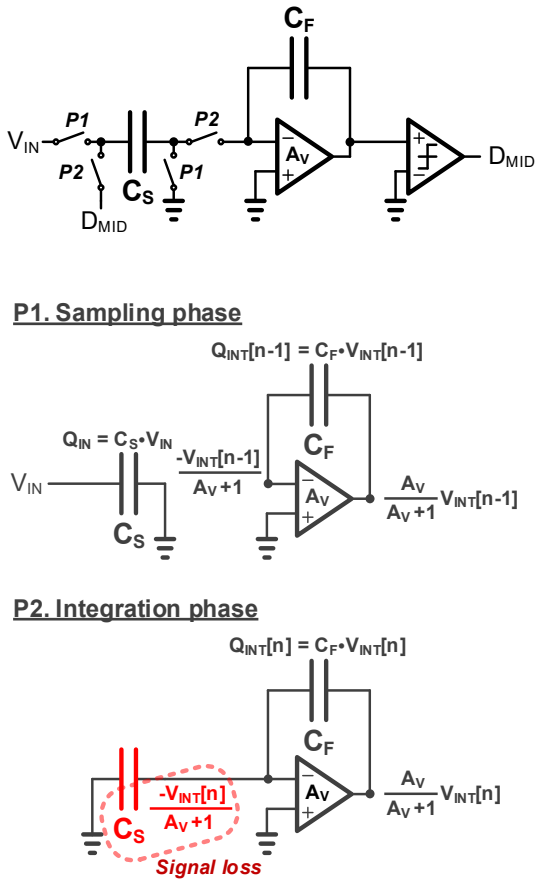


Fig. 2. Signal loss model caused by finite amplifier gain in 1st-order switched-capacitor incremental ADC.

1st-order incremental ADCs with the advantages of a positive feedback path between the integrator output and ADC input. This approach effectively leverages thermal noise averaging in the linear mode while boosting the signal-to-quantization noise ratio (SQNR) in the exponential mode, enabling operation at lower OSR comparable to other higher-order systems. However, practical non-idealities, such as accumulated signal loss caused by the finite amplifier gain of the integrator, remain prevalent. These effects significantly degrade the linearity of the digital output generated by the digital filter, ultimately making it difficult to achieve high-resolution targets.

In this paper, we present a linear-exponential incremental ADC with a digital filter to address these challenges. The switched-capacitor-based integrator, incorporating a 31-level quantizer, employs bottom-plate sampling and non-overlapping clock techniques to achieve precise delta-sigma modulation. By fine-tuning the filter weight, the digital filter effectively compensates for finite gain effects on ADC linearity, making the presented design well-suited for high-precision applications.

The remainder of this paper is organized as follows. Section II describes the architecture of the incremental ADC, including the embedded digital filter. Section III discusses the measurement results of the prototype ADC. Finally, Section IV concludes the paper.

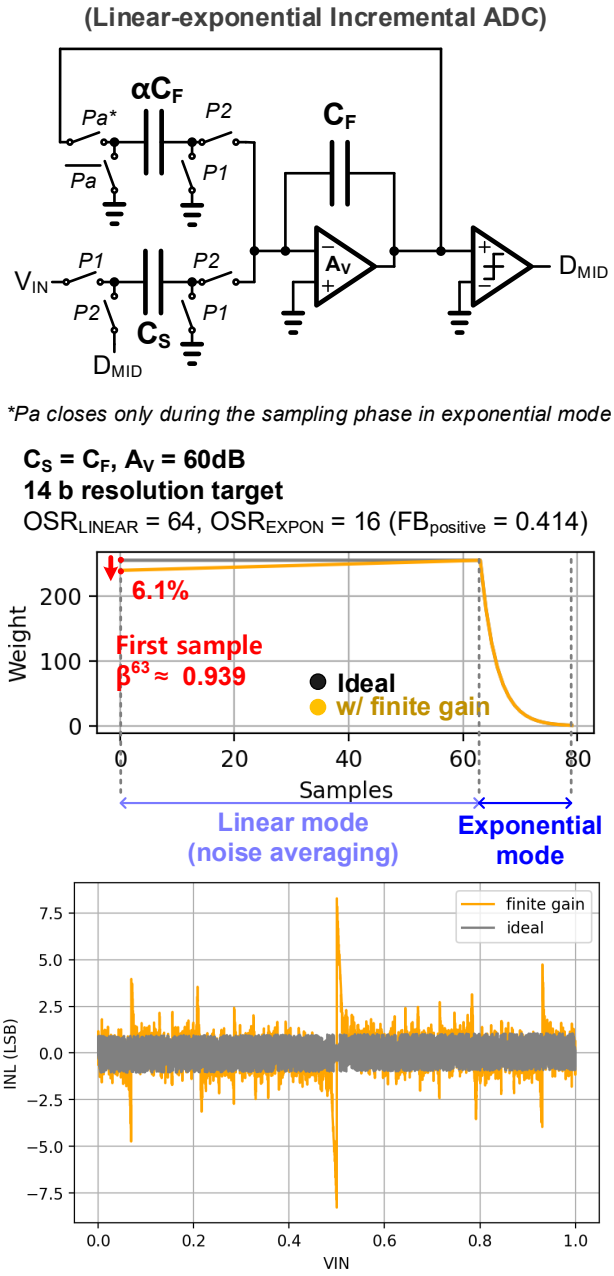


Fig. 3. Effective weighting of the linear-exponential incremental ADC (top) and its integral non-linearity performance (bottom).

II. PRESENTED LINEAR-EXPONENTIAL INCREMENTAL ADC

A. Finite Gain Effect on ADC Linearity

In incremental ADCs, achieving high resolution relies heavily on the precision of the integrator in processing input and feedback charge. However, the finite gain (A_V) of the operational amplifier causes signal loss during the transfer process, leading to cumulative errors over successive cycles.

Fig. 2 illustrates the signal loss mechanism in a switched-capacitor integrator. During the sampling phase (P1), the sampling capacitor captures the input signal while the integrator retains the previously updated signal from the prior integration phase. In the subsequent integration phase

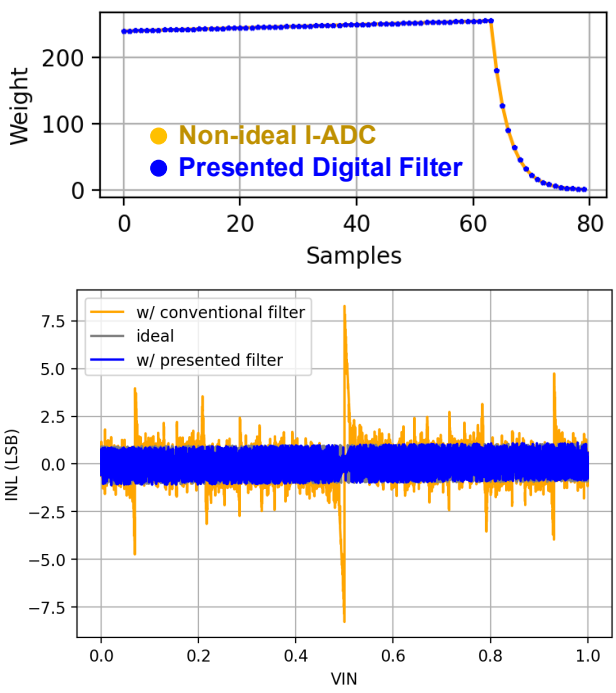


Fig. 4. Weighting correction and INL improvement using the presented digital filter.

(P2), the sampling capacitor connects to the integrator input, allowing charge transfer between them to update the integrated signal (V_{INT}). Due to the finite gain of the amplifier, complete charge transfer is restricted, leaving a residual charge in the sampling capacitor that dissipates when the next sampling phase begins. This process can be expressed as:

$$C_S \cdot V_{IN} + C_F \cdot V_{INT}[n-1] = C_S \cdot \frac{V_{INT}[n]}{A_V + 1} + C_F \cdot V_{INT}[n] \quad (1)$$

$$V_{INT}[n] = \alpha V_{IN} + \beta V_{INT}[n-1]$$
$$\alpha = \frac{(A_V+1)\cdot C_S}{C_S + (A_V+1)\cdot C_F}, \quad \beta = \frac{(A_V+1)\cdot C_F}{C_S + (A_V+1)\cdot C_F} \quad (2)$$

Here, α represents the gain of the input signal, and β reflects the integration efficiency, both of which are directly affected by the finite gain (A_V) of the amplifier. As n increases, the cumulative effects of β dominate, further amplifying the signal loss and distorting the integration process.

Fig. 3 illustrates how signal-loss-induced weighting differences translate into integrated non-linearity (INL) when A_V is 60 dB and the resolution target is 14-bit. The weight of the first linear sample (n=0) is 6.1% lower than that of the last linear sample (n=63). Although the absolute gap is small, it produces a distortion level comparable to that of a first-order incremental ADC operating at OSR = 2^{14} (14-bit target), where the first sample's weight is reduced to approximately 7.86×10^{-8} (= β^{16383}) of the last sample. Therefore, overall ADC linearity becomes highly sensitive to the integration efficiency β when a high-resolution target is required.

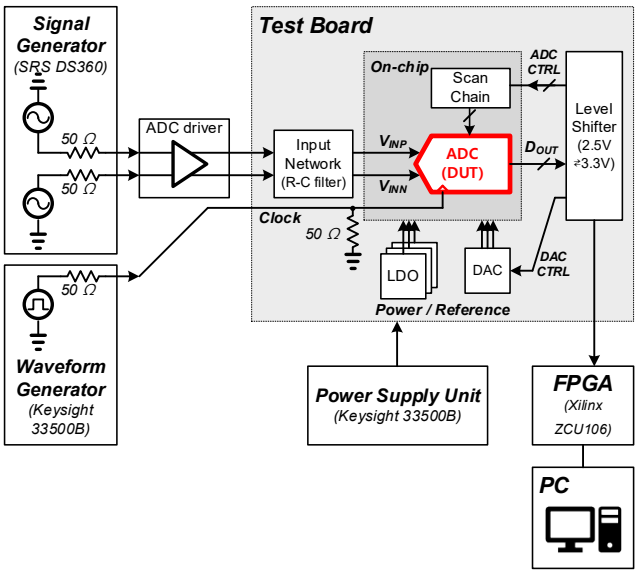


Fig. 5. Measurement setup for the prototype ADC.

B. Presented Digital Filter

A common method to address signal loss caused by finite amplifier gain in traditional incremental ADC designs is to increase the amplifier gain. Despite its effectiveness, this approach introduces significant trade-offs, such as limiting the gain-bandwidth product (GBW), which restricts achievable bandwidth (BW), or requiring higher power consumption to sustain performance. To overcome these limitations, the presented design shifts the focus from analog circuit optimization to a digital compensation strategy, leveraging the digital domain to address imperfections in the analog domain.

The digital filter in this design integrates actual sample weighting into the accumulation process, effectively compensating for the signal loss and nonlinearity introduced by finite amplifier gain. Instead of simply summing the digital output of the quantizer (D_{IN}), the filter applies a refined accumulation:

$$SUM[n] = D_{IN} + W \cdot SUM[n-1] \quad (3)$$

Here, the weighting factor W is directly derived from the integration efficiency β. Since β remains constant throughout the entire linear-mode conversion cycle, the filter implementation is both simplified and efficient, ensuring accurate weighting adjustments.

The equivalence between β and W, as well as between equations (2) and (3), allows the digital filter to accurately reflect the analog domain weighting in the digital domain. By compensating for nonlinearity caused by finite gain effects, the filter restores the INL to ideal levels. Fig. 4 demonstrates the effectiveness of this approach, showing how the INL, which deviates significantly without compensation, is brought back to near-ideal levels with the presented digital filter. Behavioral-model simulations corroborate this benefit, showing the SNDR rising from 83.8 dB to 85.0 dB (≈2.2 dB) after compensation. The results highlight the filter's ability to address weighting disparities and signal loss, ensuring consistent performance even in high-resolution applications.

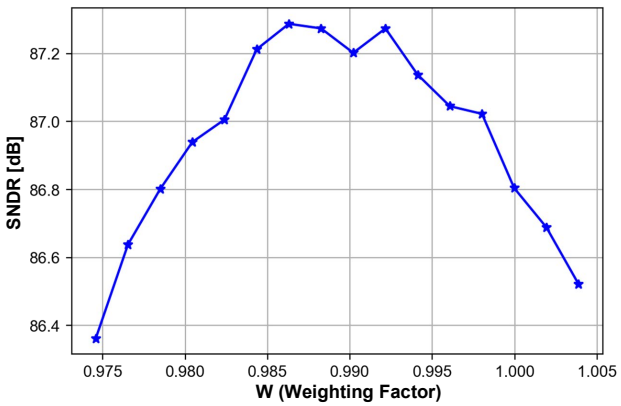


Fig. 6. Measured SNDR performance across varying weight settings.

III. MEASUREMENT RESULTS

The presented linear-exponential incremental ADC with an embedded digital filter was fabricated in a 65-nm CMOS process. It employs a conventional, fully differential, two-stage cascode amplifier in the integrator. A 14-bit (4-integer / 10-fractional) digital-filter weight was swept during characterization, and the setting that maximized measured SNDR was adopted. Its performance was evaluated using a measurement setup including a waveform generator for providing the ADC clock, a power supply unit for stable power delivery, a differential signal generator for ADC input, and an FPGA for data acquisition. The test setup also includes discrete components, such as LDOs and DACs, to ensure precise testing conditions (Fig. 5).

The overall performance of the ADC was measured for a signal bandwidth of 18.75 kHz. With an input signal frequency of 5.66 kHz and an OSR of 80, the ADC achieves a peak SNDR of 87.3 dB and a total harmonic distortion (THD) of -101.8 dB. To evaluate the effectiveness of the digital filter, the weight W was swept across its range. As shown in Fig. 6, the optimum SNDR performance was achieved with $W_{LIN} = 0.986$. At this configuration, the digital filter is effectively compensated for finite amplifier gain and mitigates positive feedback variations caused by capacitor mismatch.

IV. CONCLUSION

This work presented a linear-exponential incremental ADC with a digital filter that addresses key challenges associated with finite amplifier gain. By leveraging a digital compensation strategy, the ADC mimics analog domain weighting in the digital domain, effectively restoring linearity and achieving near-ideal INL performance. Fabricated in a 65-nm CMOS process, the ADC achieved a peak SNDR of 87.3 dB within an 18.75 kHz bandwidth, with the digital filter's weight optimization improving precision and reducing power consumption.

ACKNOWLEDGMENT

This work was supported by Institute of Information & Communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (No.2020-0-01297 and No. 2022-09-00991). The chip fabrication and EDA tools were supported by the IC Design Education Center (IDEC), Korea.

REFERENCES

[1] P. Vogelmann, J. Wagner, M. Haas and M. Ortmanns, "A Dynamic Power Reduction Technique for Incremental ΣΔ Modulators," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1455-1467, May 2019,

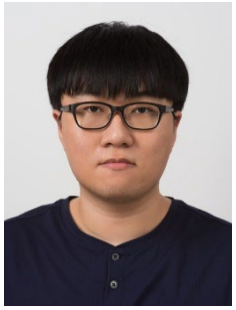
[2] V. Quiquempoix et al., "A low-power 22-bit incremental ADC," in IEEE Journal of Solid-State Circuits, vol. 41, no. 7, pp. 1562-1571, July 2006,

[3] R. Gao et al., "Weightings in Incremental ADCs: A Tutorial Review," *2023 IEEE Custom Integrated Circuits Conference (CICC),* San Antonio, TX, USA, 2023, pp. 1-8,

[4] B. Wang, S. -W. Sin, S. -P. U., F. Maloberti and R. P. Martins, "A 550- μW 20-kHz BW 100.8-dB SNDR Linear- Exponential Multi-Bit Incremental ΣΔ ADC With 256 Clock Cycles in 65-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 4, pp. 1161-1172, April 2019,

Minkyu Yang received the B.S. degree in electronic engineering from Hanyang University, Seoul, South Korea, in 2020, and the M.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2022, where he is currently pursuing the Ph.D. degree in electrical engineering. His current research interests include the design of energy-efficient analog-front-end integrated circuits.

Changjoo Park received the B.S. degree in electronic engineering from Inha University, Incheon, South Korea, in 2019 and received the M.S. degree in electrical engineering and computer science from the Gwangju Institute of Science and Technology, Gwangju, South Korea, in 2021. He is currently pursuing a Ph.D degree in electrical engineering at Korea Advanced Institute of Science and Technology, Daejeon, South Korea, since 2021. His current research interests include the design of energy-efficient analog-front-end integrated circuits.



Jooeun Kim received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2020 and 2022, respectively. He is currently pursuing a Ph.D degree in electrical engineering at the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, since 2022. His current research interests include low-power circuits and sensor interfaces.

Jeongmyeong Kim received the B.S. degree in electrical and computer engineering from Ajou University, Suwon, South Korea, in 2020, and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2022, where he is currently pursuing the Ph.D. degree in electrical engineering. His research interests include analog integrated circuit design, power management integrated circuits.

Dalta Imam Maulana received the B.S. degree in electrical engineering from Institut Teknologi Bandung, Indonesia, in 2019, and the M.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2022, where he is currently pursuing the Ph.D. degree in electrical engineering. His research interests include asynchronous circuit design, 3D IC design, and energy-efficient accelerators for AI applications.

Wanyeong Jung received the B.S. degree from Seoul National University, Seoul, South Korea, in 2012, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2014 and 2017, respectively. From 2017 to 2019, he was a post-doctoral Associate with Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA, USA. Currently, he is an Associate Professor with the School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon, South Korea. His research interests include low-power circuits and systems, energy-efficient edge computing, and the Internet of Things.