An Adaptive Gate Driver-Assisted Continuously Scalable-Conversion-Ratio Switched-Capacitor Converter

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Abstract **- This paper presents an adaptive gate driver-assisted continuously scalable-conversion-ratio (CSCR) switched-capacitor (SC) DC-DC converter. Gate-source voltage controller (GSVC) generates dynamic supply voltage to the gate driver adaptively according to the output voltage level of the converter. By adopting an adaptive gate driver to achieve soft charging between capacitor connections, the overall system generates a wide range of output with high power density and power conversion efficiency. The proposed converter generates an output range from 0.7 V to 1.8 V from an input voltage of 2.9 V. The proposed converter achieves a peak PCE of 72%. The proposed converter is implemented in TSMC 180 nm BCD process, with a chip area of 3 mm x4 mm.**

***Keywords*— Switched-capacitor converter, PMIC, voltage-conversion-ratio**

I. Introduction

In recent years, Internet of Things (IoT) technologies have been advanced to perform multiple operations with limited hardware resources. To support the end nodes of IoT applications to achieve high performance, various multi-core-based system-on-chip (SoC) designs have been introduced recently. However, to improve the battery lifetime of IoT nodes, the power management integrated circuit (PMIC) should provide a per-core dynamic voltage and frequency scaling (DVFS) scheme [1] to improve the energy efficiency of digital loads.

Switched capacitor (SC) DC-DC converters have been widely studied due to their compatibility with on-chip applications. Although these SC converters require more complex hardware designs to provide a wide output voltage (V_{OUT}) range, the converters achieve higher power density than inductor-based converters and higher PCE than LDO regulators [2]-[3]. Therefore, a wide V_{OUT} switched capacitor (SC) converter is a key component in the implementation of battery-powered IoT nodes for small form factors and long battery lifetime.

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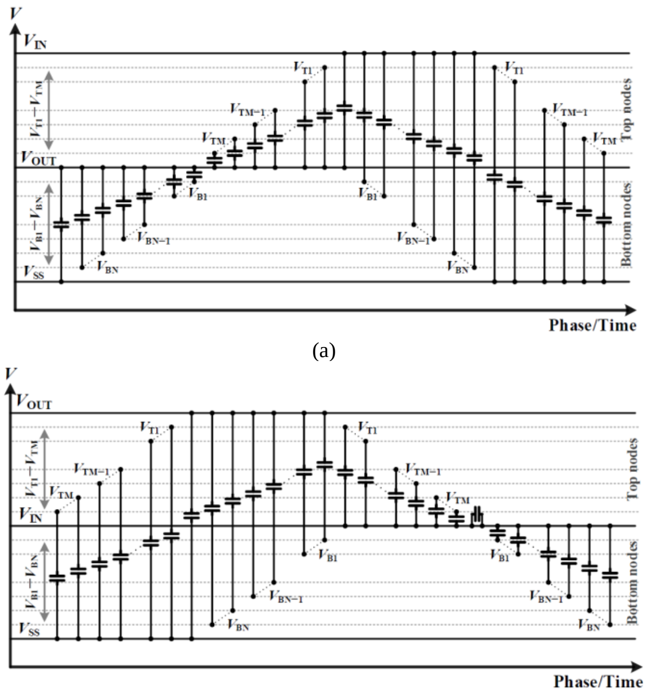


(a)

(b)

Fig. 1. Voltage versus phase diagram topology of (a) conventional single-output step-down CSCR SC converter [4] and (b) conventional single-output step-up CSCR SC converter [5].

II. Experiments

A. Prior Works

Recently, continuously scalable-conversion-ratio (CSCR) SC topologies have been proposed to overcome the discontinuity of VCR [4]-[9]. Compared with other hybrid buck-boost converters, these converters perform soft charging between flying capacitors (C_{core}s) by changing the hardware connections between C_{core}s in each phase. Therefore, the CSCR SC converters have multiple SC cores that perform interleaved charge-sharing operations. Fig. 1 shows the hardware connections of the single C_{core} of conventional CSCR SC converters. In the design of CSCR SC converters, the hardware connection sequences between the C_{core}s determine the power conversion operation of the CSCR SC converter [4]. For example, the SC core in Fig. 1(a) performs step-down conversion and the SC core in Fig. 1(b) performs step-up conversion. These CSCR SC

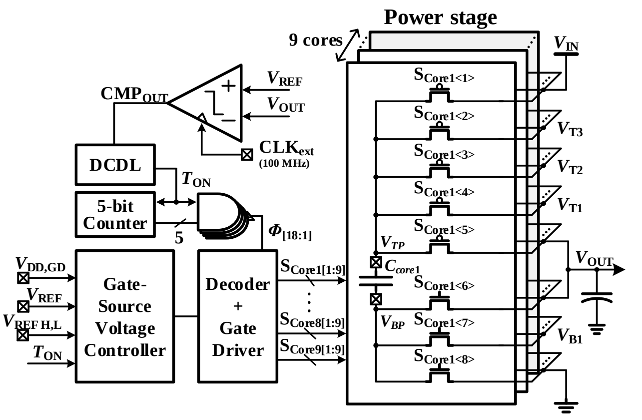


Fig. 2. Top block diagram of the proposed adaptive gate driver assisted CSCR SC converter.

converters perform power conversion operations with low charge-sharing losses and bottom plate losses. However, increasing the number of SC core cells results in larger hardware areas for the controller and gate drivers, as well as increased hardware complexity. And reducing the number of SC core cells results in an increase in charge-sharing losses due to hard-charging between the C_{core}s.

B. Top Architecture

Fig. 2 shows the top block diagram of the proposed adaptive gate driver-assisted CSCR SC converter. The proposed converter adopts a CSCR SC power stage consisting of the number of nine SC core cells, and each SC core cell consists of five switches at the top node of C_{core} (three switches connected to the top flying nodes ($V_{T1\text{-}3}$) and switches for V_{OUT} and V_{IN}) and three switches at the bottom node of C_{core} (one switch connected to the bottom flying node (V_{B1}) and switches for V_{OUT} and V_{SS}). The output of a dynamic comparator (CMP_{OUT}) triggers the on-time signal (T_{ON}) by comparing V_{OUT} with its reference voltage (V_{REF}). V_{OUT} is regulated by controlling the off-time between each T_{ON} pulse, the pulse width of which is determined by the digital controller delay line (DCDL). The five AND gates sequentially distribute the T_{ON} signal into 18 phase signals ($\Phi_{[1:18]}$), which generate signals to drive the power stage through the decoder. The gate-source voltage controller (GSVC) adaptively supplies the gate drivers with voltage (V_{DD}, GND) by monitoring V_{REF} and comparing it with reference voltages ($V_{REF,H}$ and $V_{REF,L}$).

C. GSVC Circuit

Fig. 3(a) shows the design target of the GSVC circuit. The CSCR SC topology exhibits a flat power conversion efficiency (PCE) curve, which is achieved by suppressing hard charging through gradual charge sharing between C_{core}s. However, the deviation of the output voltage from the optimum voltage (V_{opt}) at which the flying nodes ($V_{T1\text{-}2}$, $V_{B1\text{-}2}$) are uniformly distributed (as shown in Fig. 3(b)) causes the loss of charge sharing through hard charging operation, resulting in a decrease in PCE in the practical implementation of the CSCR SC topology. The case where

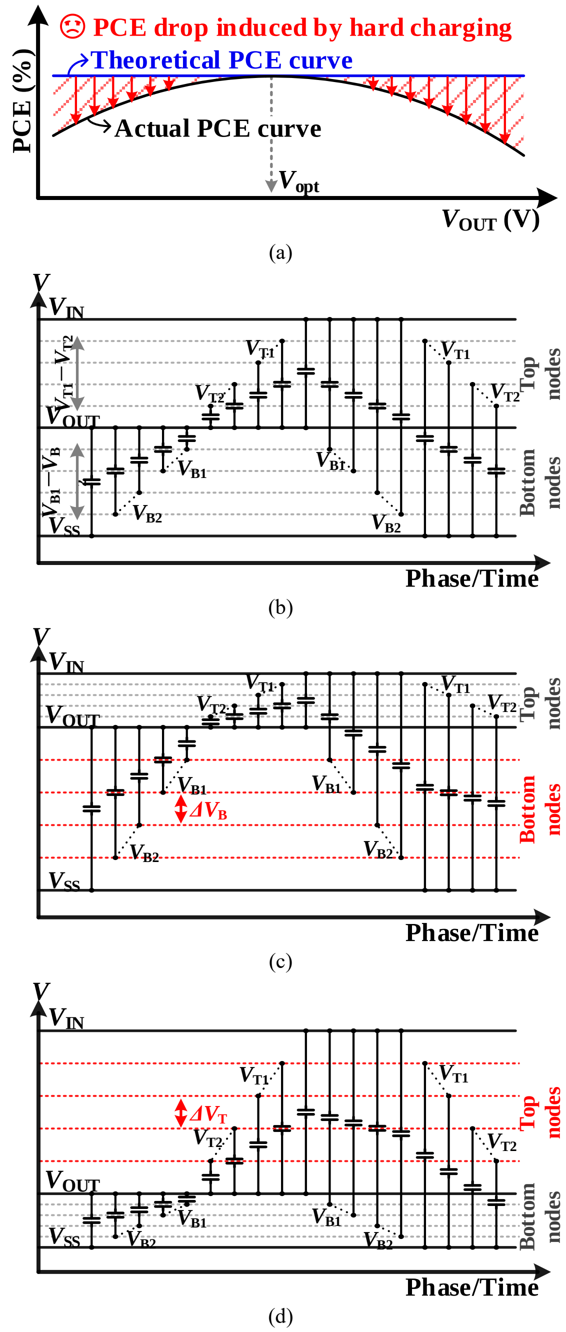
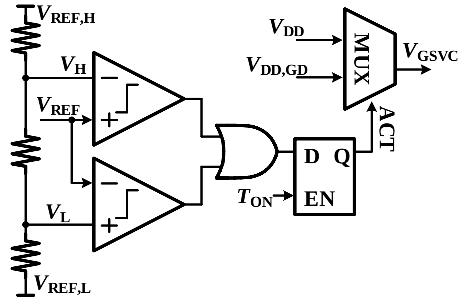


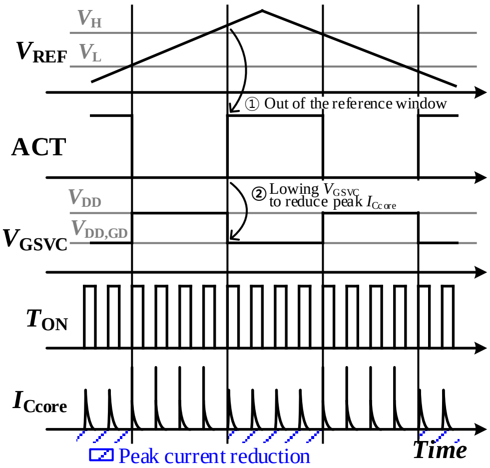
Fig. 3. Design target of GSVC for the wide output voltage range (a), the voltage versus phase diagram topology of optimum output voltage (b), the upper voltage level of V_{opt} (c), and the lower voltage level of V_{opt} (d).

V_{OUT} is regulated at the upper level of V_{opt}, the voltage difference of the bottom flying nodes (ΔV_B) is increased as shown in Fig. 3(c), resulting in charge-sharing loss at the bottom node connection between C_{core}s. Regulating V_{OUT} at the lower level of V_{opt} increases the voltage difference (ΔV_T) between the top flying nodes as shown in Fig. 3(d), resulting in charge-sharing loss at the top node connection.

Fig. 4 shows the circuit implementation of the GSVC. The GSVC employs two static comparators to compare V_{REF} and $V_{REF,H,L}$, which are divided by resistors into V_H and V_L signals, respectively. When the V_{REF} deviates from the voltage range of V_H and V_L, the activate signal (ACT) is generated. The



(a)



(b)

Fig. 4. (a) Circuit implementation of the gate-source voltage controller and (b) operation of the proposed converter.

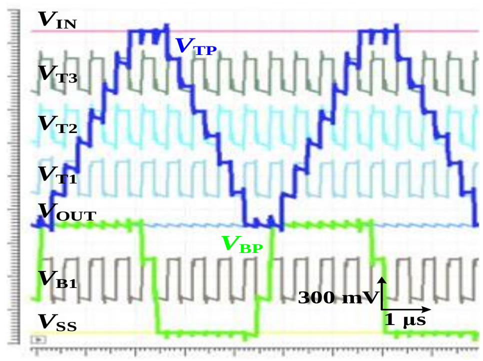


Fig. 5. Simulated waveforms of the internal nodes of the converter.

ACT signal transits through a latch when T_{ON} is high, preventing abnormal switching operation. Based on the ACT signal, the supply voltage of the switch drivers is set to either V_{DD} or $V_{DD,GD}$. The gate driver voltage level reduces the peak hard-charging current between C_{core}s (I_{Ccore}) by lowering the gate-source voltage of the switch, which increases its on-resistance.

Fig. 5 shows the simulation results of the internal voltage waveforms of the proposed converter. The three top flying nodes and one bottom flying node toggle voltages evenly, facilitated by charge sharing across the nine cores. Consequently, the C_{core}s of the CSCR cores swing as follows: the top plate nodes swing from V_{OUT} to V_{IN} through the flying nodes, while the bottom flying nodes swing from V_{SS} to V_{OUT}. As a result, the flying nodes stepwise swing from V_{SS} to V_{IN} via the flying nodes.

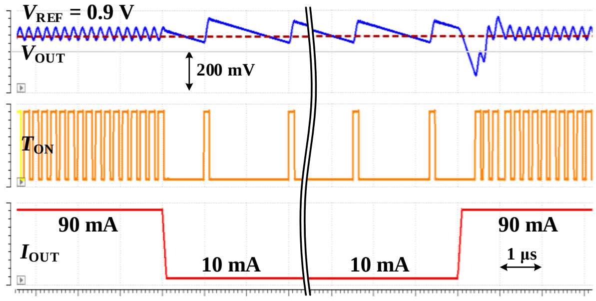
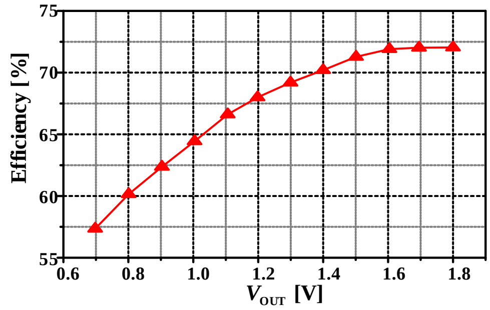
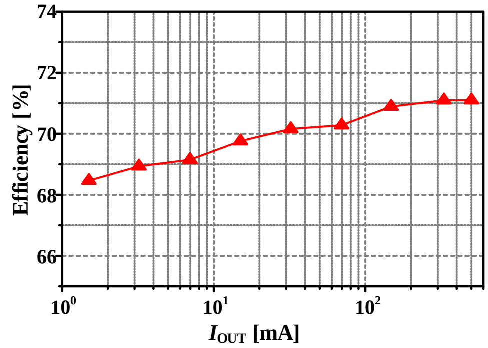


Fig. 6. Simulated I_{OUT} load transient waveforms.



(a)



(b)

Fig. 7. Simulated power conversion efficiency plots (a) with respect to V_{OUT} at V_{IN} = 2.9 V and R_{OUT} = 5Ω, and (b) with respect to I_{OUT} at V_{IN} = 2.9 V and V_{OUT} = 1.5 V.

III. RESULTS AND DISCUSSION

Fig. 6 shows simulated load transient waveforms of the converter. During the load transient from 10 mA to 90 mA, the output voltage is regulated by off-time modulation, tracking the reference voltage. Fig. 7 shows the simulated PCE results of the proposed converter. The converter covers an output voltage range of 0.7 V to 1.8 V from V_{IN} of 2.9 V as shown in Fig. 7(a). Additionally, the converter supplies I_{OUT} ranging from 1.5 mA to 500 mA at V_{OUT} of 1.5 V and V_{IN} of 2.9 V as shown in Fig. 7(b).

Fig. 8 shows the chip layout of the proposed converter. The converter is fabricated using a 180 nm BCD process, with a chip area of 3 mm x 4 mm. For the high load current, the size of the power switches was designed large. It is designed that the power switches are placed along the pad lines to reduce the length of the power metal lines and improve the PCE. The control circuits are placed at the center of the chip so that the control signals for the power stages travel through the short route.

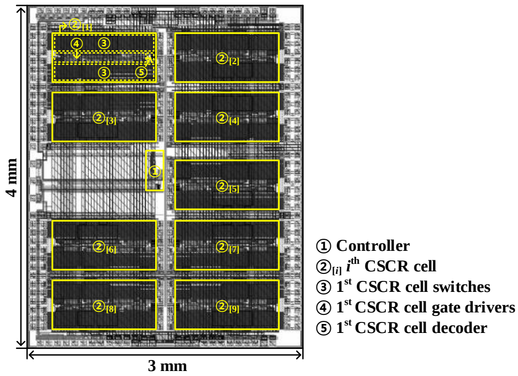


Fig. 8. Chip layout.

TABLE I. Comparison with state-of-the-art SC converters.

	[2]	[3]	[4]	[8]	**This Work**
Process	65nm CMOS	180nm BCD	28nm CMOS	65nm CMOS	**180nm BCD**
V_{IN} (V)	1.5	2.5–5	2	0.4–2.5	**2.9–3**
V_{OUT} (V)	0.18–1.19	0.1–3.67	0–2.22	0.4–2	**0.7–1.8**
# of VCR	4	9	CSCR	CSCR	**CSCR**
$C_{FLY,total}$ (nF)	400 (Off-chip)	49.23 (MOS, MIM)	0.458 (MOS, MOM)	19.8 (MOS, MOM)	**300 (Off-chip)**
$I_{OUT,max}$ (mA)	400	362*	3*	19.8*	**500**
PCE_{max} [%]	93.7	87	93	90	**72**

* Estimated based on the study

IV. Conclusion

Table I presents a performance comparison of the conventional step-down SC converters with a wide V_{OUT} range. This paper illustrated the adaptive gate driver-assisted CSCR SC converter. The power stage is composed of nine CSCR core cells with three top-flying nodes and one bottom-flying node. The proposed GSVC reduces the capacitor current modulating V_{GS} of power switches, so the energy loss mechanism between the C_{core} connections is changed from hard charging to soft charging-based operation. As a result, the converter achieves a wide output voltage range beyond the non-optimal VCR range.

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