Input-Signal-Based Power-Gated Single-Slope ADC for Low-Power CMOS Image Sensors

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Abstract **- This paper presents a low-power single-slope analog-to-digital converter (SS-ADC) that uses two comparators of the same structure to predict when a comparator flips. One of the comparators, a replica comparator, uses only half the bias current compared to the main comparator, causing the output of the comparator to flip early. By predicting the flipping time of the comparator in advance, power-gating techniques can be applied, resulting in reduced dynamic power consumption. The proposed 11-bit SS-ADC is fabricated using a 28-nm standard process, considering a resolution of 320 × 240 and an operating frame rate of 133 frames per second. Measurement results demonstrate that the power consumption of the proposed SS-ADC has decreased by approximately 17.6%. The total power consumption per column is 4.8 μW, and the figure of merit is 76.4 fJ/conversion step.**

Keywords— **Image sensor, Low-power comparator, Pixel-signal-based prediction, Positive-feedback bias sampling**

I. INTRODUCTION

With the growing demand for low-power complementary metal–oxide–semiconductor (CMOS) image sensors (CISs) in always-on applications, there has been increasing research on energy-efficient single-slope analog-to-digital converters (SS-ADCs) [1,2]. Conventional CIS architectures commonly employ N-bit SS-ADCs in a column-parallel readout structure comprising a comparator and an N-bit counter owing to their inherently high linearity. However, the static power consumption in the comparator and the dynamic power consumption in the counter with the increased toggling frequency according to the illumination conditions degrade the energy efficiency of these SS-ADCs.

To obtain low-power operation in SS-ADCs, a dynamic source follower and dynamic bias comparator structure were introduced to minimize the static power consumption [1]. However, dynamic power consumption can significantly increase because the dynamic bias comparator requires 2N clock signals for N-bit data conversion. Other low-power techniques with dynamic comparators were introduced in [2,3]. The dynamic comparator has a zero-crossing (ZC) prediction-based power-gating technique [2] that predicts the time in advance when the output of the comparator is flipped, called the zero-crossing (ZC) time. The comparator is turned off until the ZC signal turns on, and then a current source is supplied to operate the comparator immediately before the ZC signal turns on. However, because the ZC time is determined by the gain difference between the two comparators (main comparator and predictor), it is inevitably affected by changes in the process, voltage, and temperature (PVT). In addition, the output voltage of the dynamic comparators in [1–3] should be precharged to VDD and discharged close to the ground voltage (=0 V) repeatedly using a clock signal. Therefore, the comparator can easily induce kickback noise in the global ramping signal (V_{Ramp}) through parasitic capacitance, as shown in Fig. 1(a). As a result, an additional amplifier as a buffer for each column is required to alleviate the kickback noise, thereby increasing power consumption.

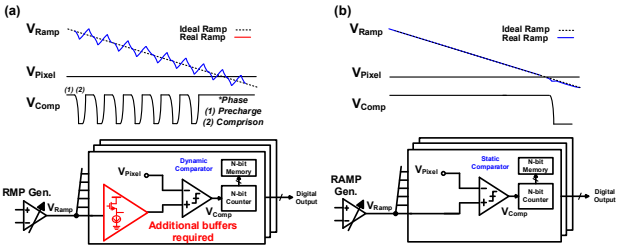

Fig. 1. Kickback noise to global ramp depending on comparator types: (a) dynamic and (b) static comparators.

To address these challenges, we propose an input-signal-based power-gated SS-ADC incorporating a replica comparator with static operation, as shown in Fig. 1(b), to achieve a low kickback noise and enhanced immunity to PVT variations. The proposed SS-ADC architecture features a main comparator that integrates an operational transconductance amplifier (OTA) and a common-source amplifier with a positive-feedback bias sampling (PFBS) technique, a replica comparator for predictive comparison, and a two-step counter. Although the design features two comparators, only one of the main or replica comparators was activated. Consequently, the static power consumption remained comparable to that of a single comparator. In addition, the replica comparator predicts the pixel value in advance, reducing the dynamic power consumption owing to

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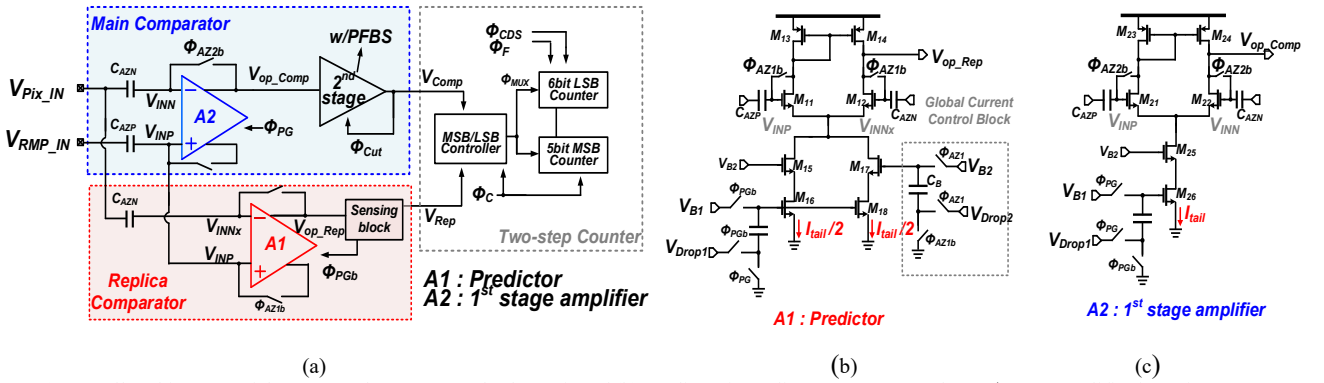


(a) (b) (c)

Fig. 2. (a) Overall architecture of the proposed SS-ADC and schematics of (b) predictor in replica comparator and (c) 1st stage amplifier in main comparator.

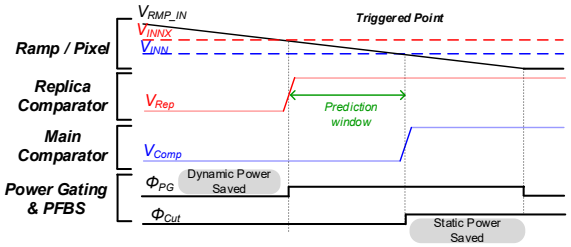
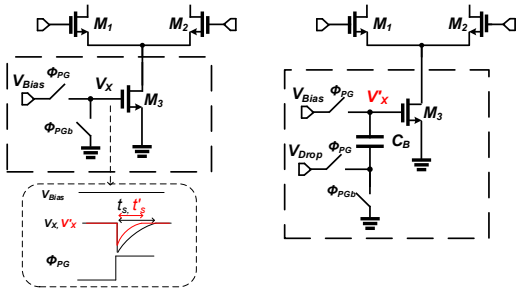


Fig. 3. Simplified operations of the proposed SS-ADC.



(a) (b)

Fig. 4. (a) conventional and (b) proposed power-gating methods.

toggling on the counter by up to 11.2% using the power-gating technique. Additionally, the PFBS technique reduced static power consumption by 21.9%. With the proposed replica comparator, the total power consumption can be reduced by 17.6 %.

II. A PROPOSED LOW-POWER SS-ADC ARCHITECTURE WITH A PIXEL-PREDICTION TECHNIQUE

A. Operations of the proposed SS-ADC

Fig. 2 illustrates the block diagram of the proposed SS-ADC, which consists of a main comparator, replica comparator, and two-step counter (6-bit LSB counter and 5-bit MSB counter). The ramp and pixel voltages (V_{RMP_IN} and V_{PIX_IN}) are applied to the first-stage amplifier of the main comparator A2, and the V_{INP} of A2 is shared with the positive input node A1. The outputs from both comparators are sent to the two-step counter, which consists of an MSB/LSB controller block, D-flip-flop, and MUX.

Fig. 3 shows the simplified operation of the proposed SS-ADC. Unlike [2], which determines the prediction window by the gain difference between the two amplifiers, V_{PIX} is shifted, resulting in better immunity against PVT variations. Additionally, because the LSB counter operates only in the prediction window period, the dynamic power consumption can be reduced until a power-gating signal (Φ_{PG}) is turned on. The higher the illuminance, the slower the comparator flips; therefore, the effect of reducing dynamic power consumption is greater. Additionally, the second stage of the main comparator incorporates the proposed PFBS technique [4], which reduces static power consumption by disconnecting the static current path of the second stage amplifier in A2 after the comparator output (V_{Comp}) is flipped. In this case, the lower the illumination level, the slower the main comparator flips. Thus, the static power consumption effect is more significant.

B. Replica Comparator

As shown in Fig. 2(b) and (c), A1 and A2 had nearly identical structures, except for the global current control block, and produced similar output responses according to the input voltage difference. To generate the prediction window, the static current I_{tail} of A1 is halved by the global current control block, resulting in a higher V_{INNx} than V_{INN} of A2. In the global current control block shown in Fig. 2(b), before the auto-zeroing (AZ) phase, the gate voltage of M_{17} was set to the V_{B2} bias voltage, allowing a current of $I_{tail}/2$. During the AZ1 phase, when the gate voltage of M_{17} floats, a voltage drop occurs at the bottom plate of the C_B, shifting from V_{Drop2} to the ground voltage ($V_{G,\,M17} = V_{B2} - V_{Drop2}$). Because $V_{G,\,M17}$ becomes sufficiently low to turn off M_{17}, the current $I_{tail}/2$ stops flowing through M_{17} and M_{18}. The proposed power-gating technique can mitigate transient noise [5] by continuously preserving the charge amount ($V_{Bx} - V_{Dropx}$).

The sensing block included a NAND-based logic gate that generated $\Phi_{PG,}$ which activated the main comparator to control the on/off states of the currents in A1 and A2. The power-gating technique with Φ_{PG} and Φ_{PGb} can be applied to A1 and A2, respectively. Fig. 4(a) illustrates a commonly used power gating technique that relies on two switches.

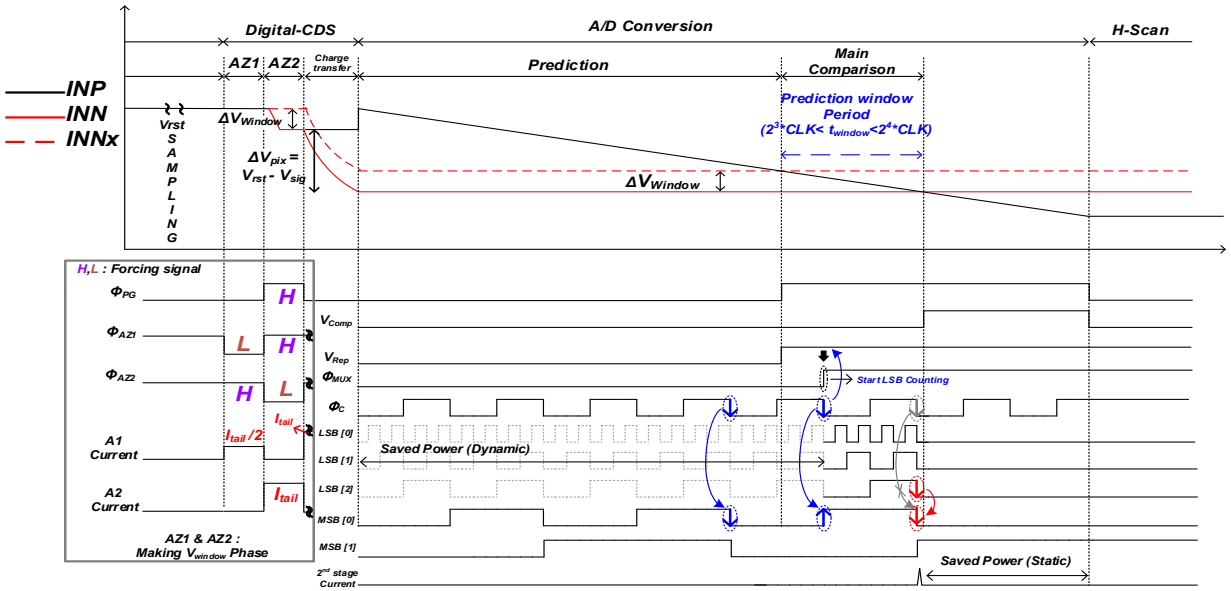


Fig. 5. Overall timing diagram with pixel-signal prediction algorithm.

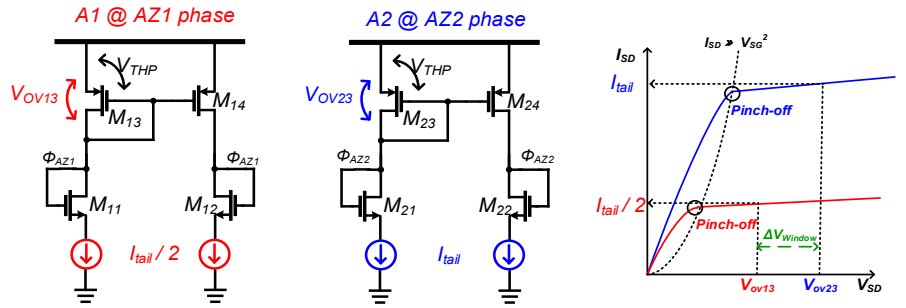


Fig. 6. Determination of prediction window.

However, when Φ_{PG} is turned on and off, the gain voltages of M_3 and V_X can fluctuate by charge redistribution because V_X should be lowered to 0 V. This can result in a transient noise within the column during the A/D conversion period. In contrast, the proposed power-gating method applied to A1 and A2, as shown in Fig. 4(b), can mitigate the transient noise by maintaining a continuous charge through V_{Drop}. The bottom of C_B is connected to V_{Drop}, resulting in less fluctuation on V_X, and settling time, t_s, is reduced from 6.4 μs to 3 ns.

Fig. 5. shows an overall timing diagram of the proposed comparator. In AZ1, the current source in A1 supplies only $I_{tail}/2$ through the global current-control block, and the input transistors of A1 are diode-connected using Φ_{AZ1}. Consequently, during the AZ1 phase, the overdrive voltages (V_{ov_A1}) of M_{13} and M_{14} in A1 are maintained at low levels owing to the reduced current. The autozeroed gate voltages at V_{INNx} and V_{INP} are $V_{DD} - (|V_{ov\_A1} + V_{thp\_M13,M14}|)$, which is equal to V_{INNx}. This global current control block operates only once in the AZ1 phase, and then the C_B stabilizes the fluctuations in V_{B2}. After the AZ1 phase, the diode connections of the input transistors in A1 were released, and the gate voltage of M17 was again set to V_{B2} to allow I_{tail} to flow. In the AZ2 phase, the input transistors in A2 were diode-connected. Because the W/L ratio of the A2 current source is twice that of A1, A2 flows twice as high I_{tail} as A1, leading to higher overdrive voltages M_{23} and M_{24} in A2

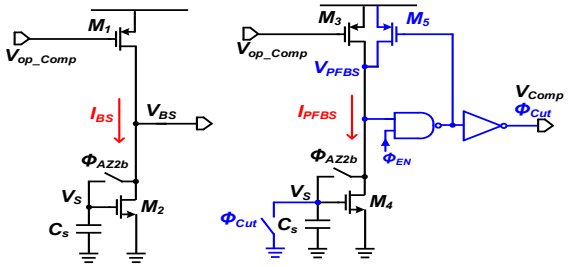


Fig. 7. (a) Column bias sampling schematic and (b) proposed positive feedback bias sampling (PFBS) schematic.

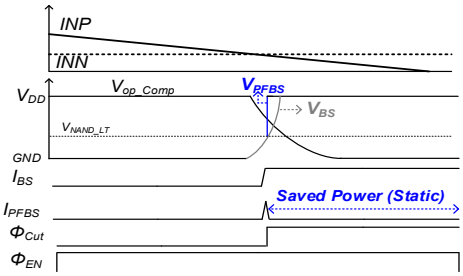


Fig. 8. Low-power operation with the proposed PFBS and CBS.

(V_{ov_A2}) than in V_{ov_A1}. Therefore, V_{INN} and V_{INP} have $V_{DD} - (|V_{ov\_A2} + V_{thp\_M23, M24}|)$ (=V_{INN}), which is lower than that of V_{INNx}. After the AZ1 and AZ2 phases, A1 and A2 flow through the same I_{tail}, resulting in the same gain and generating the prediction window.

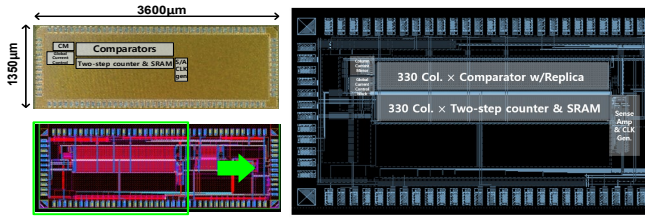


Fig. 9. Layout and Chip Photo.

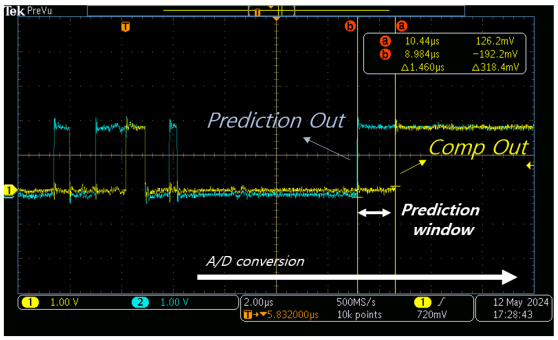


Fig. 11. Measured prediction window at 1/2 I_{tail} (N=2).

C. Prediction Window

In the AZ1 and AZ2 phases, V_{INN} and V_{INNx} are different ($V_{INNx} - V_{INN} = \Delta V_{window}$) because of the different overdrive voltages of the pMOS according to the current change, as shown in Fig. 6. The prediction window, ΔV_{window}, obtained from the large-signal analysis of the current equation according to the saturation state of the MOSFET is expressed as follows:

$$\Delta V_{Window}[V] = \sqrt{\frac{I_{tail}}{K'p(\frac{W_p}{L_p})}} \cdot (1 - \sqrt{\frac{1}{N}}) \qquad (1)$$

Where N is the divisor value obtained by dividing I_{tail} by A1: For example, the current path of A1 in Fig. 2(b) is divided into two paths, where N has a value of 2. K'_p is the process-dependent value of the pMOS, and W_p/L_p is the width and length ratios of M_{13} and M_{14}. After the charge-transfer operation of the pixel is completed, the pixel voltage ($\Delta V_{pix} = V_{rst} - V_{sig}$) is coupled with C_{AZN} to change V_{INN} and V_{INNx}. Depending on the input capacitor and C_{AZN} of A1, the offset of the comparator input may occur, and this can be compensated by adjusting the DC voltage of the ramp signal.

During the prediction phase, only the MSB counter operates. In the subsequent two-stage counter block, the MSB counter operates using a coarse clock (Φ_C) similar to the high-order bits of the LSB counter. When the V_{Rep} signal is generated, the Φ_{MUX} output is aligned with the timing of the LSB counter through a D-flip-flop within the MSB/LSB controller. From that point on, the LSB counter starts toggling and the MSB counter is synchronized with the LSB counter through Φ_{MUX}, resulting in the reduction of the dynamic power consumption of the counter under high lighting conditions.

D. Positive-Feedback Bias Sampling for Low-Power Operations

Fig. 7 shows the popularly used column bias sampling (CBS) technique [6,7] and the proposed PFBS structure for the second stage. The CBS technique samples its own bias to the C_S using a diode connected to M2 and M4 in the AZ2 phase. Each column can be isolated from any fluctuations during the A/D conversion. Fig. 8 shows the operation of the PFBS and CBS when INN approaches INP. The V_{BS} changes along with the output of V_{op_Comp} of A2. Subsequently, even after the V_{BS} flipping process is complete, the current I_{BS} continues to flow through M2, remaining in saturation. This represents an unnecessary power dissipation since the comparison operation has concluded. The proposed Positive-Feedback Bias Sampling (PFBS) technique introduces an additional switch, a NAND gate, and a feedback transistor (M5). The signal Φ_{EN} maintains a high logic level only during the A/D conversion phase. When V_{PFBS} rises sufficiently to activate M5 via the V_{op_Comp} output, the feedback mechanism effectively reduces the current wastage. As V_{PFBS} is fixed to logic H through positive feedback, the voltage sampled at V_S is removed by Φ_{Cut}, which is the output of the inverter; thus, after the output change of the comparator is completed, no more current flows through the I_{PFBS}. The PFBS consumes current only when the output changes; thus, a high gain can be obtained by positive feedback.

(a) (b)

Fig. 10. (a) Histogram of random noise in readout circuits (b) measured images with different input signals.

TABLE I. PREDICTION WINDOW IN TIME COMPARISON.

	N=1.33 (3/4Itail)	N=2 (1/2Itail)	N=4 (1/4Itail)
Simulation [μs]	0.67	1.42	2.55
Measurement [μs]	0.65	1.46	2.51
$1-\sqrt{\frac{1}{N}}$ in (1)	0.134	0.293	0.5

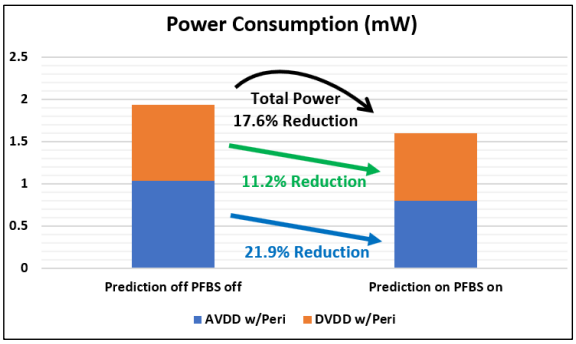


Fig. 12. Power consumption of the proposed SS-ADC (ΔV=0.1V, low illumination condition).

TABLE II. COMPARISON WITH PRIOR WORKS AND SUMMARY.

	This work	JSSC 20 [1]	ISCAS 22 [2] (Sim.)	JSSC 21 [7]	JSSC 18 [8]	Sensors 20 [9]	JSSC 17 [10]
Process (nm)	28	110	110	110	130	90	40
Supply Voltage (V) (Analog / Digital)	1.8 / 1.0	2.5/2.2/1.5	2.8 / 1.5	2.8/1.8	3.3/1.2	2.8/1.5	2.5,2/1.1
Comparator type	Static with power gating	Dynamic	Dynamic, static with power gating	Static	Static with dual gain	Static with two-step	Static with double AZ
Resolution (V × H)	330×240 (without pixels)	640 × 640	640 × 480	1024 × 240	2592 × 2054	960 × 720	N/A
A/D resolution (bit)	11	10	10	11	10	12	12
Power consumption (mW)*	1.6	1.8	1.9	57.2	320	28	-
Power consumption /Col (μW)	4.8	2.8	3.0	55.8	123.5	33	56.5
Frame rates (FPS)	133	44	120	570	120	35	-
1 row conv. tme (μs)	31.3	-	-	-	-	-	56.2
Random noise (μV_{rms})	85.28	-	-	168	-	-	261.5
FoM (fJ/conv-step)**	76.4	97.5	50.3	200	412.7	283	-
FoM (fJ/conv-step)***	74.1	-	-		-	-	83.0

* Pixel amplifier + ADC power consumption, ** FoM = (Power) / (# of pixel × Frame rate × $2^{\text{ADC resolution}}$), *** FoM = (Power/Col × 1 row conv. time) / ($2^{\text{ADC resolution}}$)

III. MEASUREMENT RESULTS

The proposed SS-ADC was fabricated with a 28-nm standard process and a 1.8V, 1.0 V supply voltage and used a pixel-signal-prediction comparator and a two-step counter for digital correlated double sampling circuit in the consideration of an image resolution of 320 × 240, bit depth of 11-bit, and a double data rate of 66.6 MHz at 133 frames/s. Fig. 9 shows the layout and chip photograph of the readout circuits, such as the column ADC, pixel amplifier, and peripheral block without pixels. Fig. 10(a) shows a random noise histogram of the readout circuits, resulting in 85.28μV_{rms}(0.35LSB), and (b) shows the measurement image sweeping the external pixel signals. Because the pixel signal voltages are forced on all column ADCs, the image shows only a monotone screen. The prediction window size should be considered to minimize the number of toggles in the LSB counter. However, an error could occur if the window is too narrow and the LSB counter does not operate. On the other hand, if the window is too wide, as the I_{tail} is significantly reduced during AZ1 phase, the reduced bandwidth lengthens the settling time to generate V_{INNx}, which increases the AZ1 phase time and degrades the frame rate. Therefore, the range of the prediction window over time is as follows:

$$CLK\ Cycle\ of\ the\ Highest\ LSB\ < t_{Window}\ [sec] < CLKcycle\ of\ the\ lowest\ MSB \quad (2)$$

In this study, because the 6-bit LSB counter with 66.6 MHz of F_{CLK} is used, the range of the ideal prediction window is from 961ns to 1.92μs (when N is 2). Fig. 11 presents the measured prediction window, showing a value of 1.46 μs, which falls within the range specified by (2). To evaluate the effect of the divisor N on the prediction window, I_{tail} was adjusted between 1/4 and 3/4 of its nominal value. As summarized in Table I, the prediction window varied according to the changes in N and demonstrated a strong agreement between the simulation and measurement results.

As mentioned earlier, the power reduction effect appears differently depending on the pixel signal (= illumination). Fig. 12 shows the total SS-ADC power consumption with a pixel amplifier compared to the non-PFBS and prediction for a low-light input signal (ΔV=0.1V). The overall power consumption was 1.6mW, with a consumption of 0.297mW by the pixel amplifier; the comparator and pixel amplifier consumed 0.801mW and achieved approximately 21.9% power savings compared to non-PFBS, and 0.798mW by the counter, reducing power consumption by 11.2 %.

Table II compares the proposed SS-ADC with previous low-power CIS readouts [1,2,7-10]. The overall readout power consumption is 1.6 mW, with a power consumption of 0.297 mW by the pixel amplifier; 0.504 mW by the comparator, reducing 27.4% static power consumption by PFBS; and 0.798mW by the counter, reducing 11.2% dynamic power consumption with the prediction. The proposed SS-ADC exhibits an energy efficiency of 76.4 fJ/conv.-step FoM, random noise of 85.28 μV_{rms}, and a total power consumption per column of 4.8 μW. Although the FoM of [2] appears to be superior, it should be noted that this result is based on simulation results.

IV. CONCLUSION

This paper presents a pixel-signal-prediction-based single-slope ADC (SS-ADC) designed for low-power, always-on CMOS image sensors. By utilizing the proposed input-signal-based power-gated SS-ADC, consisting of a main and a replica comparator, a prediction signal can be generated in the comparator without requiring additional power-consuming circuits, resulting in an 11.2% reduction in counter power consumption. Operating in a static mode, the proposed SS-ADC enhances reliability and energy efficiency, culminating in a total power reduction of 17.6% for the SS-ADC owing to decreased static current with PFBS. The measurement results demonstrated the suitability of the proposed SS-ADC for a wide range of low-power applications.

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