A Low-Power CMOS Optoelectronic Receiver Array for LiDAR Sensor Applications

Shinhae Choi[1,2], Yeojin Chon[1,2], and Sung Min Park[1,2,a]
[1]Division of Electronic & Semiconductor Engineering, Ewha Womans University
[2]Graduate Program in Smart Factory, Ewha Womans University
E-mail: rora0414@ewhain.net, wjsdulws7@gmail.com, smpark@ewha.ac.kr

Abstract **- This paper presents a power-efficient receiver topology for short-range LiDAR sensor applications by utilizing a 180-nm CMOS technology. The proposed design includes a fully differential transimpedance amplifier (TIA) with on-chip avalanche photodiodes and a time-to-voltage (T2V) converter. Post-layout simulations reveal that the T2V converter handles the input photocurrents from 40 μA_{pp} to 5.8 mA_{pp} for the detection range as short as 30 centimeters. The single-channel LiDAR receiver consumes 10 mW from a single 1.8-V supply and covers a detection range of 0.3 to 22.8 meters. The whole 4x6 channel optoelectronic receiver array occupies an area of 1.5 x 2.0 mm², including I/O pads.**

Keywords **- APD, LiDAR, Optoelectronic, TIA, T2V.**

I. INTRODUCTION

LiDAR (Light Detection and Ranging) sensors have been widely utilized in various applications, including advanced driver assistance systems (ADAS), remote sensing, navigation systems, and short-range monitoring systems [1-5]. It is well established that many LiDAR systems employ a pulsed Time-of-Flight (ToF) mechanism to calculate the distance to a target. Fig. 1(a) illustrates a block diagram of a conventional short-range LiDAR system, where the transmitter is typically designed as a laser diode driver, enabling the transmission of light pulses toward the target. The reflected light is then captured by the integrated receiver, which consists of an optical photodetector commonly avalanche photodiodes (APDs) that converts the incoming light pulses into electrical current signals. A transimpedance amplifier (TIA) is used to convert these current signals into voltage outputs, which are subsequently amplified by a post-amplifier (PA) and buffered by an output buffer (OB). The buffer isolates the preceding analog front-end (AFE) from the time-to-digital converter (TDC) and generates the final digital codes to estimate the detection range.

Numerous time-to-digital converters have been proposed to precisely measure the time intervals between START and STOP pulses [6-8]. However, many of these TDCs involve complex methods and algorithms, making the circuit design difficult to meet specified requirements.

Additionally, TDCs aim to reduce walk errors that typically occur in the comparators within TDCs. Nevertheless, even state-of-the-art TDCs cannot fully eliminate walk errors due to the inherent finite rise (or fall) times of STOP pulses. In this paper, we propose a simpler receiver architecture for short-range LiDAR applications.

Fig. 1(b) presents the block diagram of the proposed LiDAR receiver, which introduces a fully differential TIA to eliminate the need for a PA and OB, thus achieving lower power consumption. A time-to-voltage (T2V) converter replaces the more complex TDC circuitry. The T2V converter converts the time intervals between START and STOP signals into output voltages and holds peak values until the next reset signal arrives. Simulations show that the T2V converter can process a wide range of input currents (40 μA_{pp} - 5.8 mA_{pp}), indicating that the proposed LiDAR receiver can detect 5.8 mA_{pp} in maximum (i.e., the minimum detection range of 0.3 meters) and 40 μA_{pp} in minimum (which corresponds to 22.8-meter detection range).

This paper is organized as follows. Section II describes the circuit operations of the proposed LiDAR receiver along with the realization of on-chip P^+/N-well/Deep N-well APDs. Section III presents the chip layout and the post-layout simulation results. Then, a conclusion is followed in Section IV.

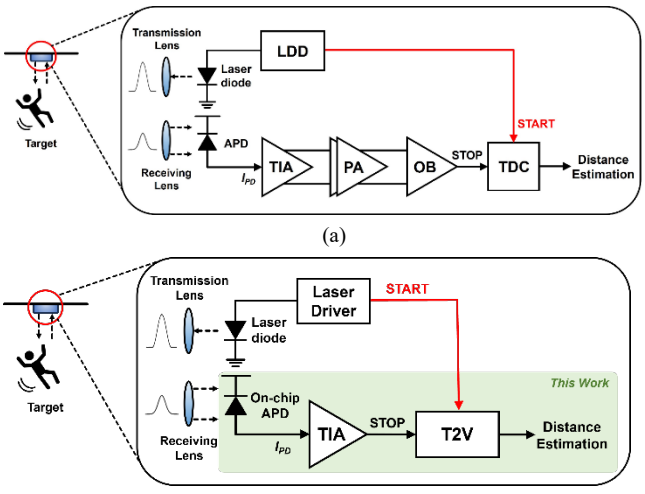


Fig. 1. Block diagrams of (a) a conventional LiDAR sensor, and (b) the proposed LiDAR sensor.

a. Corresponding author; smpark@ewha.ac.kr

Manuscript Received Oct. 24, 2024, Revised Feb. 06, 2025, Accepted Feb. 25, 2025

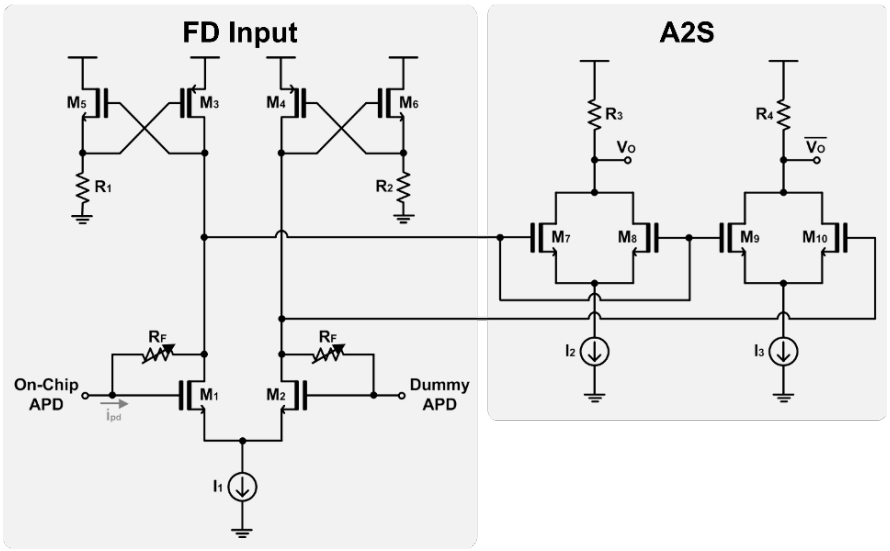


Fig. 2. Schematic diagrams of the proposed FD-TIA with the A2S converter.

II. ARCHITECTURE

A. FD-TIA

Fig. 2(a) illustrates the detailed schematic of the fully differential transimpedance amplifier (FD-TIA), which employs a PMOS load (M_3, M_4) in combination with a cross-coupled NMOS source-follower stage. This configuration enables the output voltages to reach the supply voltage (V_{DD}). The on-chip avalanche photodiode (APD) detects incoming light pulses and converts them into electrical current signals (i_{pd}), which are subsequently fed into the FD-TIA. These current signals are then transformed into voltage outputs at the drain nodes of M_1 and M_2, with the PMOS load facilitating this conversion alongside the support of the cross-coupled NMOS source followers. However, due to the single-ended nature of the input signals, the voltage outputs from the FD input stage may become imbalanced.

B. A2S Converter

In order to counteract this imbalance, an amplitude-to-symmetric (A2S) conversion circuit is incorporated [9]. The A2S converter processes the output voltages from the FD-TIA and works to create more balanced signals by directing the higher output voltage from the drain of M_1 to both M_7 and M_9 simultaneously. This results in more symmetrical output signals, achieving a gain deviation of only 0.6 dB at the drain nodes of M_7 through M_{10}.

In essence, the A2S block ensures that the previously asymmetric output signals are converted into symmetric ones, thereby providing stable input signals for both the A2V and T2V converters. This conversion process is optimized through careful tuning of resistor values and transistor sizes within the A2S circuit. Additionally, the feedback resistor (R_F) commences to function as automatic gain control (AGC) for the input currents larger than 50 μA_{pp}, which thus dynamically adjusts the transimpedance gain to enhance the input dynamic range and improve the effectiveness of the T2V converter's operations.

C. T2V Converter

The T2V converter improves the LiDAR receiver's input dynamic range by converting time-of-flight (ToF) information into corresponding output voltages, making it highly effective for detecting light pulse reflections from objects at different distances. As shown in Fig. 3, the T2V converter comprises a latch, control block, charging circuit, and PDH circuit. In this setup, output signals from the PA are fed directly into the latch comparator, which transforms them into digital pulses. The latch outputs ‘1’ if the pulse exceeds the reference voltage and ‘0’ otherwise. This output, along with the transmitted signal (START), is sent to the control block. Between the START and STOP rising edges, the control block holds the output at ‘0’, driving the charging circuit to generate a triangular waveform. When the STOP pulse is detected, the control block switches the output to ‘1’. The time interval between the START and STOP pulses controls the charging circuit’s rise time, corresponding to the ToF information. Once the output switches to ‘1’, the charging circuit halts and holds the peak value. The charging circuit comprises an operational amplifier, a capacitor, and an NMOS transistor for reset. The PDH circuit holds this output until the next reset signal.

Additionally, the T2V converter ensures accurate distance measurement by converting ToF into proportional voltages. Digital circuits like the latch and control block help reduce walk errors by generating precise STOP pulses. While prior TDC designs measured time intervals with complex algorithms [6-8], this simplified T2V converter offers an easier and more effective alternative. Additionally, the output voltages can be converted into binary codes through a thermometer-to-binary converter, making it suitable for FPGA processing.

D. Chip Layout & Post-Layout Simulation Results

Post-layout simulations were carried out using the model parameters of a standard 180-nm CMOS process. In these simulations, the on-chip APDs were represented by an equivalent electrical lumped model, which included a series resistance of 25 Ω and a parasitic capacitance of 490 fF.

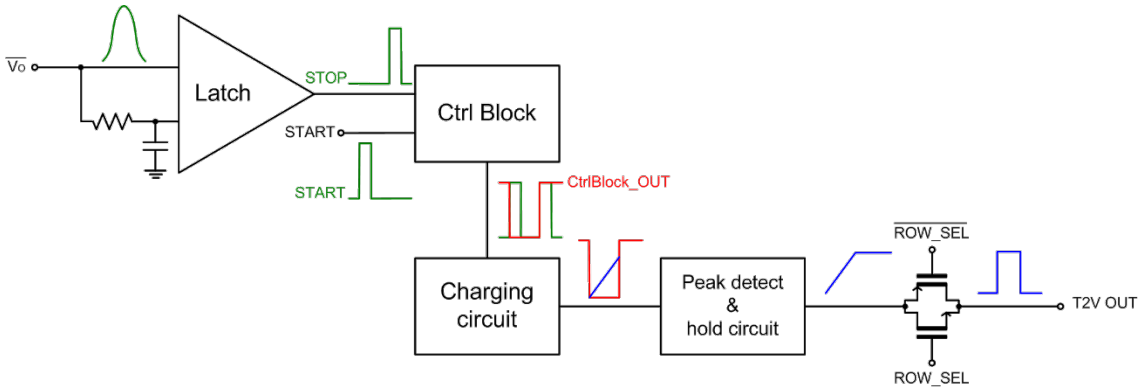
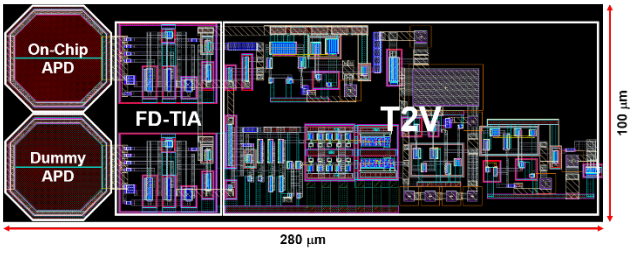


Fig. 3. Block diagram of the T2V converter.

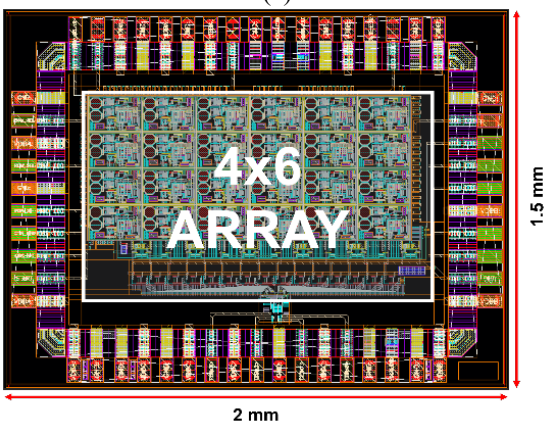
Fig 4 (a) shows the single-cell layout of the proposed LiDAR receiver, which incorporates two on-chip P^+/N-well/Deep N-well APDs and occupies a core area of 100 x 280 μm². DC simulations reveal that the LiDAR receiver consumes 10 mW from a single 1.8-V supply.

Fig. 4 (b) presents the layout of the whole 4 x 6 channel optoelectronic receiver array (ORA) chip that occupies the area of 2.0 x 1.5 mm² and consumes 261 mW in total from a 1.8-V supply.

Fig. 5 depicts the post-layout simulation results of a single-channel LiDAR receiver for varying input currents, indicating that the T2V converter successfully recovers input currents ranging from 40 μA_{pp} to 5.8 mA_{pp}. This corresponds to a dynamic range of 43.2 dB, enabling the detection of targets as close as 30 centimeters. It is evident that the T2V converter effectively handles higher input current levels, demonstrating its ability to operate efficiently across a wide range of input conditions.



(a)



(b)

Fig. 4. Layouts of (a) a single cell LiDAR receiver, and (b) the 4x6 channel ORA.

Fig. 6 illustrates the simulation results of the 4x6 ORA array with the gradually increasing input currents from 1 μA_{pp} to 5.8 mA_{pp}, which demonstrate the sequential output pulse of each column (displayed in different colors) from the 1st to the 4th row of the T2V. Here, the 2nd waveform in each column represents the T2V output that is inversely proportional to the input current, as depicted in Fig. 5. This indicates that the LiDAR receiver can detect the reflected light signals, successfully recovering the images.

Table I summarizes the performance of the proposed 4x6 channel ORA that recovers the time interval with good linearity for the LiDAR sensor applications. Furthermore, it demonstrates low-power and small-area characteristics, which help to facilitate the implementation of multi-channel arrays.

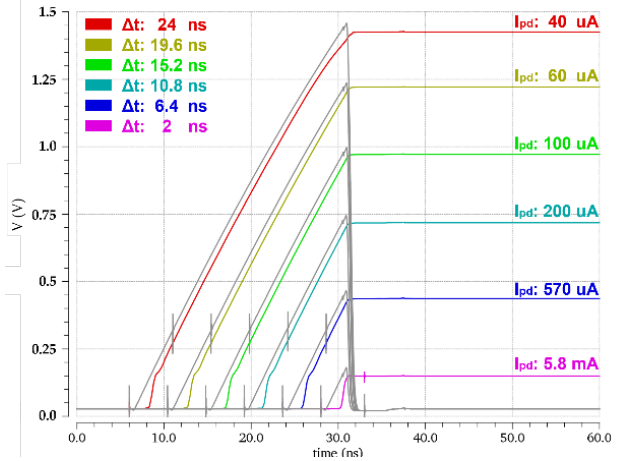


Fig. 5. Simulated pulse response of the proposed T2V where △t represents ToF (time-of-flight).

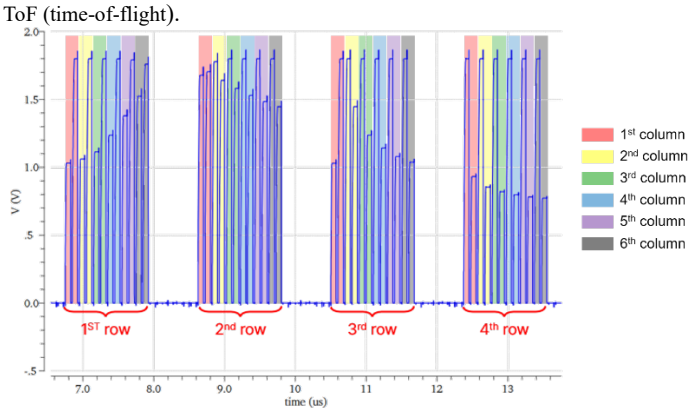


Fig. 6. Simulated results of the 4x6 ORA.

TABLE I. PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED CMOS LASER DIODE DRIVERS.

Parameters		[10]	[11]	[12]	[13]	This work
CMOS technology (nm)		350	180	180	350	180
APD	Type	Off-chip	Off-chip	Off-chip	Off-chip	On-chip
	C_{pd} (pF)	3	2	3	4	0.5
	Responsivity (A/W)	40	-	-	-	4.16
	Wavelength (nm)	905	-	-	905	850
Max. TZ gain (dBΩ)		100	83.5	100	121	81.2
Gain control		No	Yes	Yes	No	Yes
Bandwidth (MHz)		230	89	180	230	842
Min. detectable current (μA_{pp})		1.0	1.3	5	0.6	40
Max. detectable current (mA_{pp})		39$^{\xi}$	2.06	2	30	5.8
Dynamic range (dB)		92	64	52	94	43.2
Power dissipation per channel (mW)		330*	45*	49.3 / 10.5	155*	10
Chip area (mm^2)		4 (Rx 1ch) 10 (TDC)	2.52 (8ch†)	5 (Rx 8ch)	2.89 (Rx 1ch)	3.0 (Rx 24ch)

$^{\xi}$ with a separate TDC chip, *3.3-V V_{DD}, †ch = channel, ‡equivalent circuit model

III. CONCLUSIONS

We have proposed an optoelectronic receiver array chip implemented by using a 180-nm CMOS technology, specifically designed for elder-care LiDAR sensor applications. This approach offers several benefits, including reduced cost, easier integration, and minimized package parasitic. Ultimately, this work has the potential to provide an affordable sensor solution for short-range home-monitoring systems, particularly for safeguarding elderly individuals or dementia patients during emergencies.

ACKNOWLEDGMENT

The EDA tool was supported by the IC Design Education Center.

REFERENCES

[1] T. Raj, F. H. Hashim, A. B. Huddin, M. F. Ibrahim, and A. Hussain, "A Survey on LiDAR Scanning Mechanisms," ***Electronics***, vol. 9, p. 741, 2020.

[2] D. Yoon et al., "Mirrored Current-Conveyor Transimpedance Amplifier for Home Monitoring LiDAR Sensors," ***IEEE Sensors J.***, vol. 21, pp. 5589-5597, 2021.

[3] N. Frøvik, B. A. Malekzai, and K. Øvsthus, "Utilising LiDAR for fall detection," ***Health Technol. Lett.***, vol. 8, pp. 11-17, 2021.

[4] P. Fraccaro, X. Evangelopoulos, and B. Edwards, "Development and Preliminary Evaluation of a Method for Passive, Privacy-Aware Home Care Monitoring Based on 2D LiDAR Data," in ***Artificial Intelligence in Medicine: 18th International Conference on Artificial Intelligence in Medicine,*** AIME 2020, Minneapolis, MN, USA, Aug. 25-28, 2020.

[5] Y.-T. Wang, C.-C. Peng, A. A. Ravankar, and A. Ravankar, "A Single LiDAR-Based Feature Fusion Indoor Localization Algorithm," ***Sensors***, vol. 18, p. 1294, 2018.

[6] V. N. Nguyen, D. N. Duong, Y. Chung, and J. W. Lee, "A Cyclic Vernier Two-Step TDC for High Input Range Time-of-Flight Sensor Using Startup Time Correction Technique," ***Sensors***, vol. 18, p. 3948, 2018.

[7] Y. He and S. M. Park, "A CMOS Integrator-Based Clock-Free Time-to-Digital Converter for Home-Monitoring LiDAR Sensors," ***Sensors***, vol. 22, p. 554, 2022.

[8] M. Liu, H. Liu, X. Li, and Z. Zhu, "A 60-m range 6.16-mW laser-power linear-mode LiDAR system with multiplex ADC/TDC in 65-nm CMOS," ***IEEE Trans. Circuits Syst. I Reg. Pap***., vol. 67, pp. 753-764, 2019.

[9] J. -E. Joo, M. -J. Lee, and S. M. Park, "A CMOS Fully Differential Optoelectronic Receiver for Short-Range LiDAR Sensors," IEEE Sensors J., vol. 23, no. 5, pp. 4930-4939, Mar. 2023

[10] S. Kurtti, J.-P. Jansson, and J. Kostamovaara, "A CMOS Receiver–TDC Chip Set for Accurate Pulsed TOF Laser Ranging," ***IEEE Trans. Instrum. Meas.***, vol. 69, pp. 2208-2217, 2020.

[11] M. Ye, X. Zheng, Y. Li, and Y. Zhao, "A Low-Complexity Hybrid Readout Circuit for Lidar Receiver," ***IEEE Trans. Very Large Scale Integr. (VLSI) Syst.***, vol. 28, pp. 828-832, 2020.

[12] Y. Yang et al., "A Low-Power Multimode Eight-Channel AFE for dToF LiDAR," in ***2024 IEEE Int. Symp. on Circuits and Systems (ISCAS), Singapore***, Singapore, May 19-22, 2024.

[13] A. Baharmast, S. Kurtti, and J. Kostamovaara, "A Wide Dynamic Range Laser Radar Receiver Based on Input Pulse-Shaping Techniques," ***IEEE Trans. Circuits Syst. I Reg. Pap.***, vol. 67, pp. 2566-2577, 2020.

Shinhae Choi received the B.S. degree in electronic and electrical engineering from Ewha Womans University, Korea, in 2023. Her current research interests include silicon photonics, and CMOS optoelectronic integrated circuits and architectures for short-distance optical application systems and sensor interface IC designs.

Yeojin Chon received the B.S. degree in electronic and electrical engineering from Ewha Womans University, Korea, in 2022. Her current research interests include silicon photonics, and CMOS optoelectronic integrated circuits and architectures for short-distance optical application systems and sensor interface IC designs.

Sung Min Park received the B.S. degree in electrical and electronic engineering from KAIST, Korea, in 1993. He received the M.S. degree in electrical engineering from University College London, U.K., in 1994, and the Ph.D. degree in electrical and electronic engineering from Imperial College London, U.K., in May 2000. In 2004, he joined the faculty of the Department of Electronics Engineering at Ewha Womans University, Seoul, Korea, where he is currently a professor.