H-Band 4-Array Frequency-Locked Oscillator ICs Packaged in an Oversized Waveguide Channel

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***Abstract* - This paper presents the design and analysis of a 4-array oscillator module based on InP 250 nm HBT technology, with a focus on spatial power combining. Four identical oscillator ICs were integrated into a 1720 μm extended waveguide, and individual biasing was applied to achieve frequency locking at 262.7 GHz. While locking was successful, power combining through the binary channel could not be achieved due to phase mismatches between oscillator elements. Radiation pattern measurements confirmed out-of-phase locking, and the Total Radiated Power (TRP) reached 6.1 dBm, representing a 6.1 dB increase over a single module. These results highlight both the potential and the challenges of spatial power combining for high-frequency oscillator arrays.**

***Keywords*—millimeter-wave oscillator, waveguide packaging, spatial-power-combining (SPC)**

I. INTRODUCTION

The millimeter-wave (mm-Wave) band is becoming increasingly important as a key frequency resource for next-generation ultra-high-speed wireless communications. As a result, there is growing interest in developing terahertz (THz) oscillators, which serve as essential frequency sources in these high-frequency applications. However, one of the main challenges in high-frequency processes with high f_{max} is the degradation of efficiency, which limits the achievable output power. Researchers are actively exploring different technologies and circuit designs to overcome these limitations and achieve high-power oscillator performance.

A differential Colpitts VCO using 130 nm InP HBT produces a maximum power of 4.7 dBm at 300 GHz [1]. A fixed-frequency oscillator which oscillates at 305.8 GHz and produces 5.3 dBm was designed in differential cross-coupled common-base topology [2]. Another approach involves a second-harmonic oscillator built with 65 nm CMOS HBTs in the triode region, achieving 5.6 dBm at 215 GHz [3]. A notable design is a VCO chip oscillating at 227 GHz, packaged in a WR-3.4 waveguide module, which achieved an output power of 6.4 dBm [4].

To overcome the limitations of the single integrated circuits, several power-combining mechanisms are under investigation. On-chip power combining through transmission lines is a conventional technique. For instance, a four-way Wilkinson power divider and combiner enabled a power amplifier to deliver 16 dBm at 270 GHz [8]. Recent work has focused on array packaging using expanded waveguides. One study demonstrated binary power-combining channels in the W-band, integrating ten-array single-chip thru-line structures [5]. Another effort achieved a 3 dB insertion loss in the WR-3.4 band by mounting four separated thru-line chips inside a 1720μm expanded waveguide channel [6]. Optimizing the edge cells of a ten-array circuit on a single chip ensured a flat 3 dB insertion loss across the WR-3.4 band [7]. (Table I)

TABLE I. Comparison of Various Power Combining Mechanisms

Ref	Substrate	# of array	Freq band	Circuit	Antenna type	Power combining mechanism
[5]	Duroid 5880	10	W	Thru-line	Tapered slot	Binary channel, flange
[6]	InP	4	H	Thru-line	Dipole	Binary channel, flange
[7]	InP	10	H	Thru-line	Dipole	Binary channel, flange
This work	InP 250 nm HBT	4	H	Core-only oscillator	Dipole	Free-space radiation

This paper presents an exploration of oscillator arrays integrated within metallic waveguides to achieve high output power at THz frequencies. Using Teledyne′s 250 nm InP HBT process, oscillator circuits were designed and successfully packaged. An E-plane extended waveguide configuration was employed, revealing variations in frequency locking and output power depending on the use of a buffer and whether individual or merged chips were implemented.

II. SINGLE OSCILLATOR MODULE

A. Oscillator Design

The circuit is designed using Teledyne′s InP 250nm HBT process, which offers f_T=350 GHz and f_{max}=500 GHz. For the oscillator design, a cross-coupled common-base topology, widely used for H-band oscillators, is implemented (Fig. 1(a)). Despite using identical IC designs, variations between individual chips result in differences in oscillation frequency. To facilitate proper frequency locking across the cells, the buffer amplifier is intentionally excluded in this design.

As shown in the load-pull plots of power and frequency

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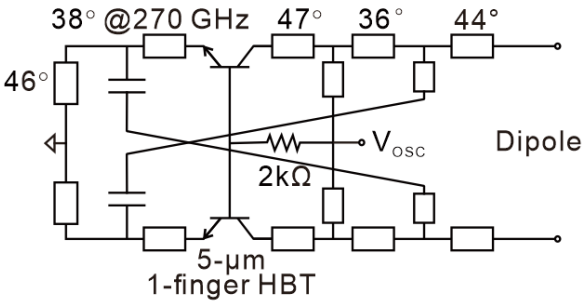

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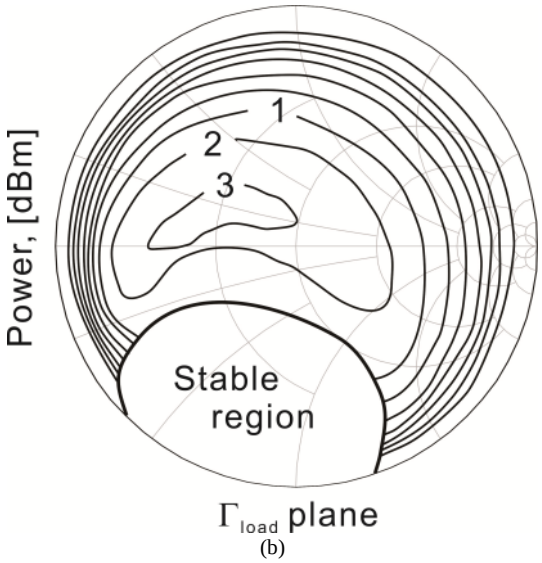

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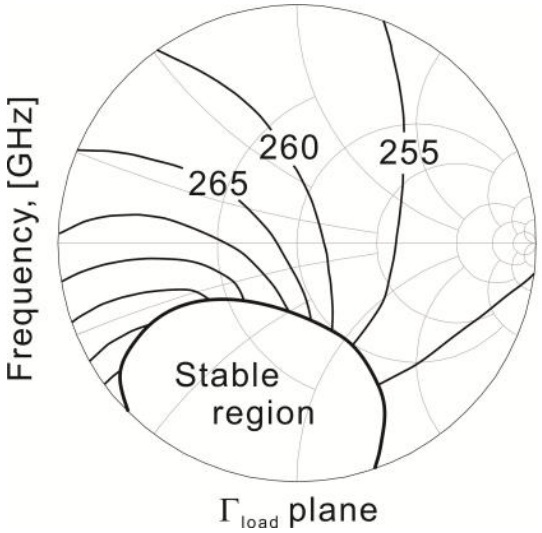

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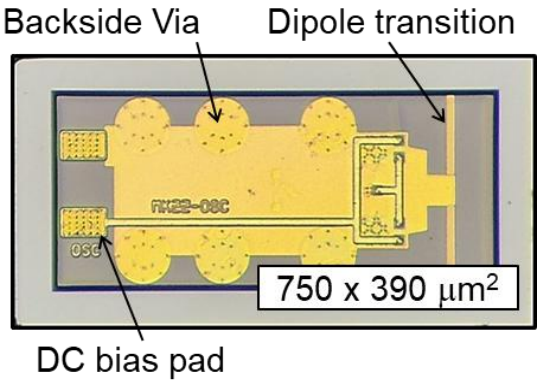
Fig. 1. Oscillator core design for waveguide packaging: (a) Circuit schematic, simulated load-pull on the Γ_{load} plane, (b) Output power, and (c) Oscillation frequency

(Fig. 1(b), (c)), the oscillation frequency is highly sensitive to output impedance. This sensitivity reflects the influence of the dipole′s environment on the oscillator core and suggests that the array configuration can improve locking performance. Including a buffer amplifier would increase isolation between the oscillator core and the output stage, limiting frequency shifts to approximately 5 GHz on the



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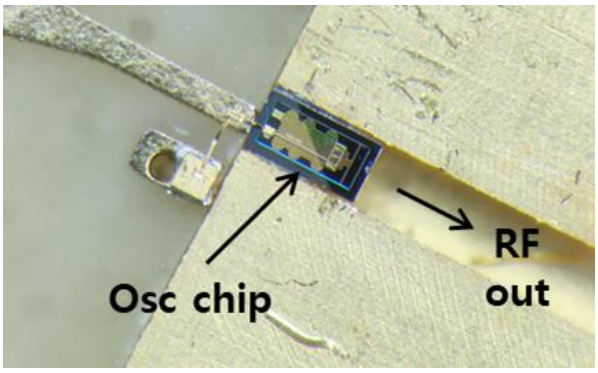

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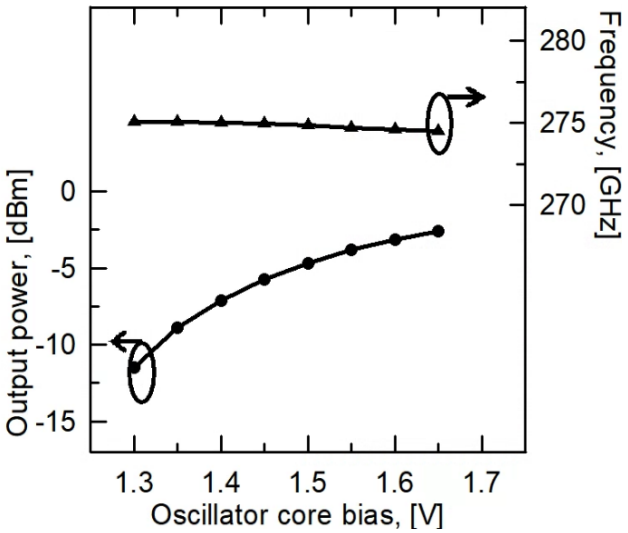

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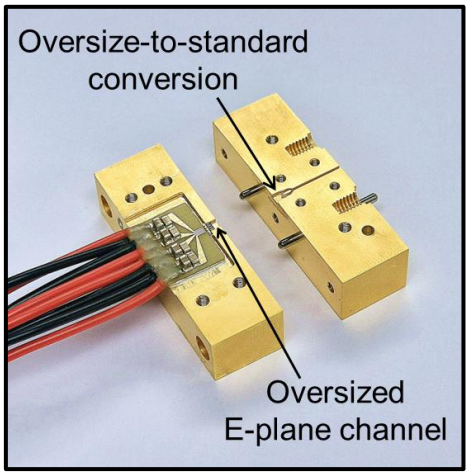
Fig. 2. (a) Photograph of the fabricated oscillator chip, (b) Single oscillator IC packaged inside a standard WR-3.4 waveguide, and (c) Measured output power and oscillation frequency of the single oscillator module with collector bias variation

Smith chart. However, this would impair locking across the array, which is why the buffer amplifier is removed in the final design.

The primary objective is not to achieve frequency tuning but to demonstrate stable operation at a single frequency with enhanced output power through the array configuration. To keep the design simple, varactor tuning components are omitted. The differential output of the oscillator circuit is coupled to a dipole transition to enable packaging inside a waveguide along the E-plane.



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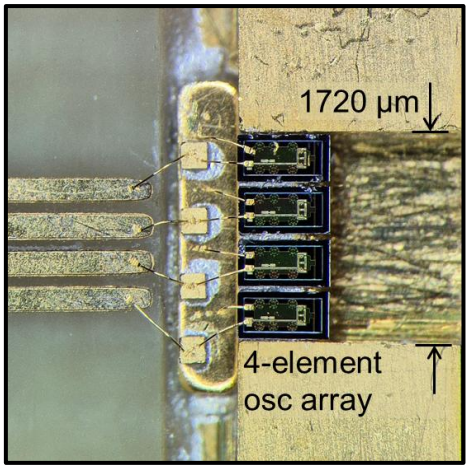

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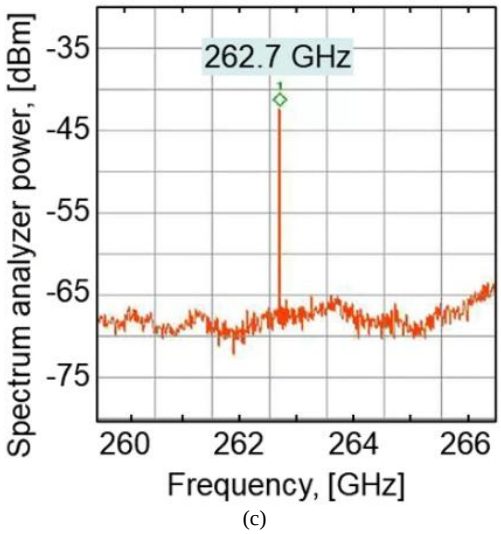

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Fig. 3. (a) Photograph of the 4-array oscillator module, (b) Four oscillator ICs packaged inside an oversized waveguide channel and (c) Frequency spectrum indicating each oscillator

B. Single Oscillator Module Performance

The fabricated chip, shown in Fig. 2, measures 750 μm in length and 390 μm in width. To prevent damage, 20 μm air gaps are provided on both sides, allowing the chip to fit easily into a standard WR-3.4 waveguide with a width of 430 μm. Fig. 2(b) shows the oscillator chip mounted in the waveguide, where it radiates signals through the dipole antenna. The left-side DC bias pad is wire-bonded to the DC line of an external FR-4 circuit to supply bias.

One challenge during assembly is electrostatic discharge (ESD), which can easily damage the circuit. To prevent this, a series of 120 pF, 10 nF, and 1 μF capacitors are mounted on the FR-4 substrate to enhance stability. The performance of the oscillator module is presented in Fig. 2(c), demonstrating an output power of -3 dBm at 1.6 V and 12 mA. With a higher bias of 1.9 V, the output power increases to 0 dBm. The oscillation frequency is centered around 275 GHz, with minimal variation across different bias levels.

III. 4-ARRAY OSCILLATOR MODULE

A. Flange Test Using Binary Channel

In [8], a 10-array thru-line was implemented in the WR-10 band, and in [5], a 4-array thru-line was integrated in the WR-3.4 band. Both studies successfully measured a 3 dB loss using binary power combiners/dividers in extended waveguides. However, when it comes to active circuits such as oscillators, integrating them into extended waveguides presents challenges. Performance variations between chips prevent the formation of a uniform field within the extended channel, which hinders proper power combining.

For this study, we packaged four identical oscillator IC chips, each designed identically, into a 1720 μm extended waveguide, as shown in Fig. 3, to conduct spatial power-combining experiments. When packaging the array oscillator, it is essential to apply individual bias voltages to each cell to enable frequency tuning, as the oscillation frequencies of the cells differ slightly. If a common bias is applied across all cells, frequency locking cannot be achieved, and mixing occurs, resulting in multiple frequencies appearing on the spectrum analyzer.

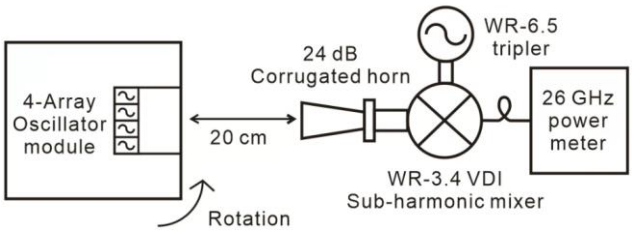
The output spectrum, with each cell′s bias voltage finely tuned to oscillate at a single frequency, is shown in Fig. 3(c). The individual biases range from 1.78 V to 1.86 V, and under these conditions, the array locks at 262.7 GHz, confirming successful frequency synchronization.

B. Total Radiated Power (TRP) Measurement

Despite achieving frequency locking, power combining through the binary channel was unsuccessful. As a follow-up, we conducted an experiment to derive the Total Radiated Power (TRP) by measuring the radiation pattern after removing the binary channel. Using E-plane and H-plane patterns, TRP can be calculated [9].

The measurement setup, illustrated in Fig. 4(a), involved using a power meter operating at 26 GHz and a VDI WR-3.4 subharmonic mixer (SHM) placed 20 cm from the source. The local oscillator (LO) for the mixer was supplied via a VDI WR-6.5 tripler, and a corrugated horn antenna with 24 dB gain was attached at the input of the SHM.

The simulated E-plane radiation pattern is shown in Fig. 4(b). When all cells are in phase, the simulation predicts a



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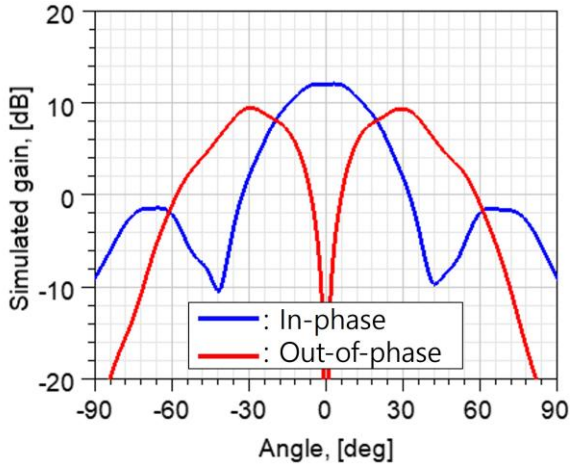

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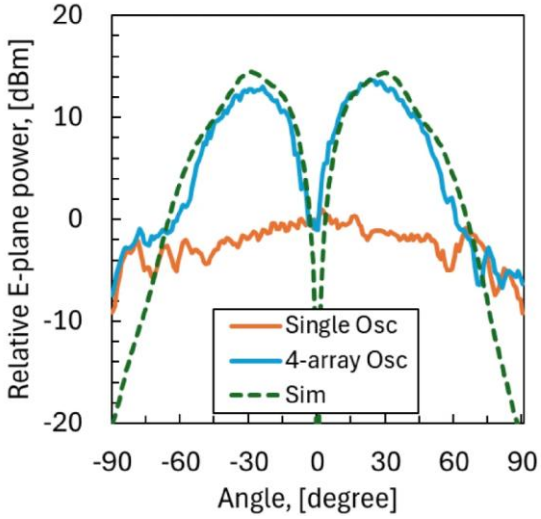

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Fig. 4. (a) Measurement setup for the pattern and radiated power, (b) Simulated E-plane pattern of the 4-element oscillator locked in-phase and out-of-phase, and (c) Measured E-plane pattern of the singe and 4-array oscillator module

gain of 12 dB at the center. However, when the cells are out of phase, a null appears at the center. The measured E-plane pattern, presented in Fig. 4(c), confirms that the null at the center indicates the four oscillator elements are locked in an out-of-phase state.

Additionally, the power level from the four-array module was significantly higher than that of a single module. The TRP, calculated from the measured pattern and Equivalent Isotropic Radiated Power (EIRP), was 6.1 dBm, representing an approximately 6.1 dB increase—four times the power of a single module.

IV. CONCLUSION

Four oscillator ICs were integrated into an oversized waveguide with a 1720 μm width, achieving frequency locking at 262.7 GHz through individual bias tuning. However, power combining through the binary channel was unsuccessful due to phase misalignment. Measured radiation patterns confirm that each of the four oscillator elements is locked out of phase with a null at the center. Despite this, the 4-array module achieved a TRP of 6.1 dBm, four times higher than that of a single module. Further research is underway to achieve in-phase locking of each oscillator element using injection-locked oscillators, with the goal of enabling power combining through the binary channel.

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REFERENCES

[1] D. Kim and S. Jeon, “A 300-GHz high-power high-efficiency voltage-controlled oscillator with low power variation,” IEEE Microw. Wireless Compon. Lett., vol. 30, no. 5, pp. 496–499, May. 2020.

[2] J. Yun, D. Yoon, H. Kim, and J. -S. Reih, “300-GHz InP HBT oscillators based on common-base cross-coupled topology,” IEEE Trans. Microw. Theory Techn., vol. 62, no. 12, pp. 3053–3064, Dec. 2014.

[3] R. Kananizadeh and O. Momeni, "High-power and high-efficiency millimeter-wave harmonic oscillator design, exploiting harmonic positive feedback in CMOS," IEEE Trans. Microw. Theory Techn., vol. 65, no. 10, pp. 3922-3936, Oct. 2017.

[4] J. Jeong, Y. Jeon, and Y. Jang, "H-band high-power and high-efficiency voltage-controlled oscillator IC and waveguide module," IEEE Trans. Terahertz Sci. Technol., vol. 14, no. 2, pp. 238-247, Mar. 2024.

[5] C. Yi, K. Kim, H. J. Kim, and M. Kim, "W-band waveguide module design for power combining of linear microstrip array," IEEE Microw. Wireless Compon. Lett., vol. 31, no. 6, pp. 569-571, Jun. 2021.

[6] J. Lee, et. al., "WR-3.4 overmoded waveguide module for the packaging of a linear integrated-circuit array," Electronics, vol. 11, no. 13, pp. 2091, Jul. 2022.

[7] Y. Koh, S. Jeon, and M. Kim, “WR-3.4 multi-mode waveguide module with single-chip-integrated array circuits," Electronics Letters, vol. 60, no. 8, Apr. 2024.

[8] A. S. Ahmed, et. al., "A compact H-band power amplifier with high output power," Proc. IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Jun. 2021.

[9] R. Han and E. Afshari, “A CMOS High-Power Broadband 260-GHz Radiator Array for Spectroscopy,” IEEE J. Solid-State Circuits, vol. 48, no. 12, pp. 3090–3104, Dec. 2013.

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