Optimizing CML-CMOS Converter Through Sizing Transistors for Producing 50% Duty Square Wave

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***Abstract* - The current-mode logic (CML) circuits are widely used in several ICs for its low power dissipation and high speed performance. As the analog and digital mixed ICs are widely used, this implies great advantage of CML circuits. A drawback of the CML circuit is its less robustness of noises than static CMOS circuits because of its small signal swing. Thus, combined application of CML and static CMOS circuits in a single IC is inevitable, and also the CML-CMOS converter is important to combine them together in a chip. In this paper, by sizing transistors of a comparator, the CML-CMOS converter accomplishes the rail-to-rail output signal with 50.14% duty cycle. Rising/falling time of the output signal are lessened by 87.3~90% compared with input CML signal. D-Q delay of the comparator is optimized by 216~239ps.**

***Keywords*—CML-CMOS converter, Comparator, Duty, IC, Square wave, VLSI**

I. INTRODUCTION

Recently, wide usage of VLSI chips emphasizes the importance of the ideal square wave generation. Most of ICs use CLK signal to operate their logic. Improving CLK generator performance is a big issue [1]. Since clock signal toggles all times, it is very important to make it dissipate little power. Many researches have been focusing on the issue [2]. In the case of VCSEL driver, square-waved current should be also applied to their proper functioning [3].

With improvement of fabrication of ICs process, the power dissipation of the chips becomes critical issue of designing a IC [4]. For lowering power consumption of VLSI chips, current-mode logic (CML) is widely used. Its small swing and low voltage level of signal can yield lower power dissipation than static CMOS circuits. This implies that CML circuits have the great advantages to be inserted in mixed signal circuits [5]. The conventional method can be applied in high speed drive IC [6, 7]. However, CML circuit is less robust to several environmental noise because of its small swing, so designing a single chip only with CML circuits is not a good choice.

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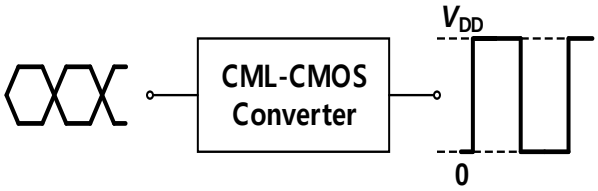


Fig. 1. CML signal and output through the CML-CMOS converter.

To combinate CML circuit and static CMOS circuit, CML-CMOS converter is necessary. Role of the CML-CMOS converter is to make input CML signal swing rail-to-rail, so that the static CMOS circuit easily accept the signal. CML-CMOS converter can be made of a simple comparator [8]. The positive feedback of a comparator is utilized to spread input voltage swing rail-to-rail as Fig. 1. In addition, spreading CML signal can overcome less noise robustness of CML circuits.

In this paper, main consideration of the design is square-waved output signal with 50% duty cycle. By sizing transistors, optimized CML-CMOS converter is proposed. To make sure that the output signal close to ideal wave, rising/falling time simulation is held. D-Q delay of the comparator is also a consideration of this paper for faster performance. In Section II, details of the circuit structure are considered. Simulation tests and results are in Section III. At last, the conclusion of the research is covered in Section IV.

II. DESIGN METHODOLOGY

A. Comparator

The circuit figure of a comparator used in this paper is in Fig. 2. The comparator accepts two inputs, V_p and V_m. Between the input signals, the comparator senses the signal that has bigger magnitude and if V_p is bigger than V_m, transmits high voltage, V_{DD}, as the output signal. In a case of bigger V_m, the comparator drops the output signal to low voltage level. The proposed comparator circuit consists of two driving NMOSs, cross coupled current source loads, and three current mirrors. The proposed structure makes a positive feedback to make sure that the output signal is formed rail-to-rail.

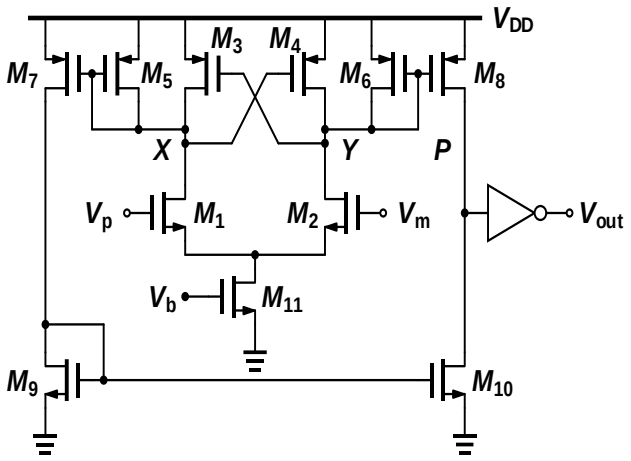


Fig. 2. A comparator circuit structure.

The specific procedure of the operation is as following: If V_p increases, the drain current of M_1 goes up. The current difference makes voltage of node X, V_X, decreases. Then M_4 produces more current from V_{DD} to node Y, and voltage of node Y, V_Y, increases. Contrariwise, M_3 produces less current from V_{DD} to node X due to the mentioned operation, and then V_X goes down. As a result, a positive feedback occurs and the difference between V_X and V_Y increases until V_Y reaches V_{DD}. Due to the positive feedback, M_3 is turned off and only M_5 makes a current path from V_{DD} to ground through M_1 and M_{11}. As M_5 and M_7 form a current mirror, the same current flows through M_7 and M_9. M_9 and M_{10} also form a current mirror, so M_{10} makes a current path from node P to ground. On the other hand, since V_Y reaches V_{DD}, M_6 and M_8 are turned off. Then no current flows from V_{DD} to node P. Then voltage of node P, V_P, decreases and reaches ground voltage. In conclusion, through the inverter, V_{out} goes high.

Contrary, if V_m increases, the opposite operation occurs. V_X increases and reaches V_{DD}, then turns off M_4, M_5, and M_7. M_6 makes the only path from V_{DD} to ground though M_2 and M_{11}. Due to several current mirrors, no current flows through M_{10}, then the input port of the inverter does not have path to the ground. Instead, M_8 makes a path from V_{DD} to node P. As a result, V_P increases and V_{out} is dropped to the low voltage level. In short, little difference of V_p and V_m makes the extreme change of V_{out}. Through the procedure, small swing of the input CML signal is amplified to rail-to-rail output.

Since making output signal in 50% duty is the main purpose of this paper, sizing transistors in the comparator is held, especially the devices directly connected to node P. As NMOS transistors, M_9 and M_{10}, have bigger W/L ratio, pull down speed of node P gets faster, and then duty would decrease. On the other hand, as PMOS transistors, M_3~M_8, have bigger W/L ratio, pull up speed of node P becomes faster, and then duty would increase. However, due to parasitic capacitances of the transistors, total delay would increase as transistors are scaled up.

More inverters can be added at the output of the comparator as a buffer. The buffer makes output wave sharper because of its regenerative property. As a trade-off, inserting a buffer can make input-output delay bigger due to the delay of the inverters.

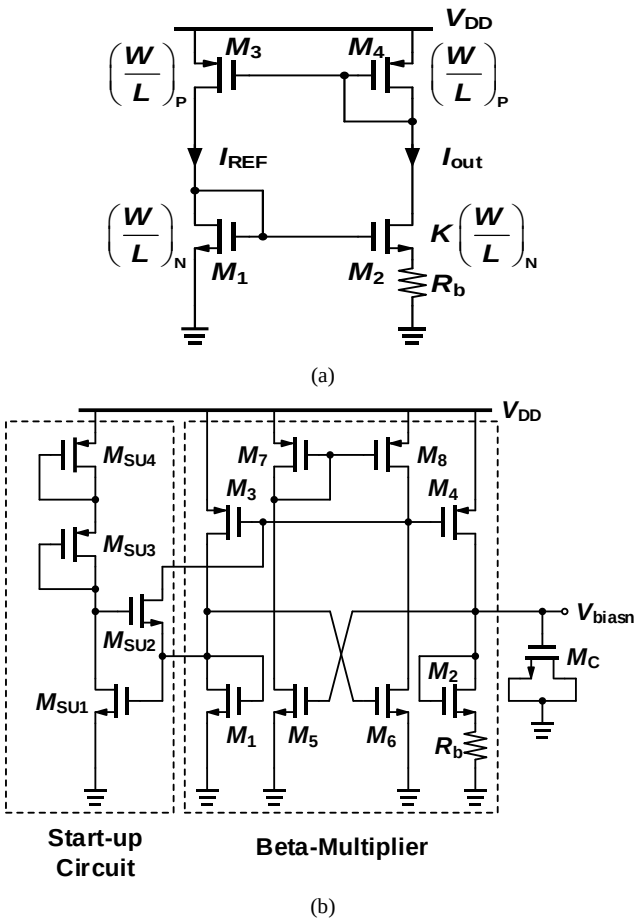


Fig. 3. (a) A simple beta-multiplier; (b) modified beta-multiplier

B. Beta-multiplier

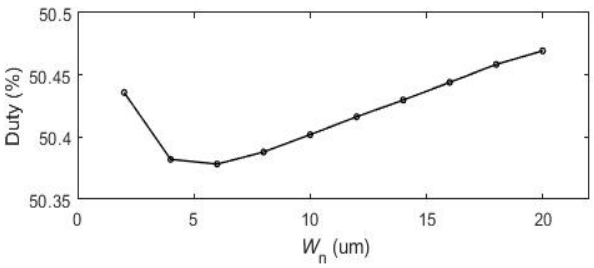
For proper operation of a comparator, the current source, M_{11} in Fig. 2, should produce steady and stable current to the circuit. If the current through M_{11} varies as input varies, the differential movements of V_X and V_Y can be slowed or, extremely, corrupted. The corruption can result malfunctioning of total the operation, so we should design a stable bias circuit, a beta-multiplier.

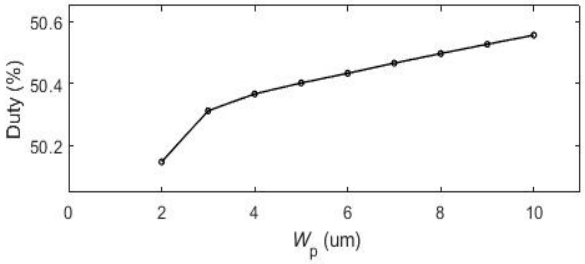
A simple beta-multiplier structure is in Fig. 3. (a). The beta-multiplier consists of two current mirrors and a resistor [9]. Two current mirrors are mirroring their current each other so that constant current can flow through the circuit. A resistor R_b is inserted in source of M_2 to choose certain current level. M_1 and M_2 have same gate voltage level, so following equations can be derived.

$$V_{GS1} = V_{GS2} + I_{out}R_b \tag{1}$$

$$\sqrt{\frac{2I_{REF}}{\mu_n C_{ox}(W/L)_N}} + V_{TH1}$$

$$= \sqrt{\frac{2I_{out}}{\mu_n C_{ox}K(W/L)_N}} + V_{TH2} + I_{out}R_b \tag{2}$$





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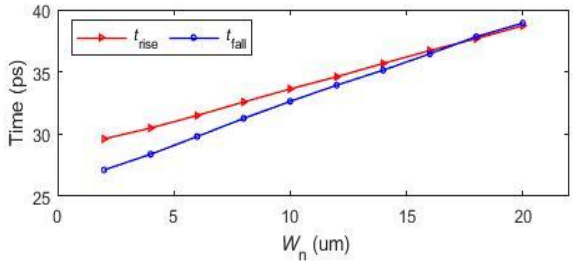

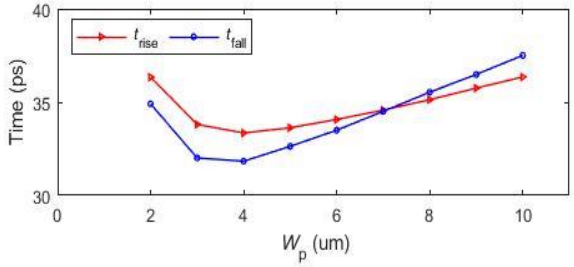

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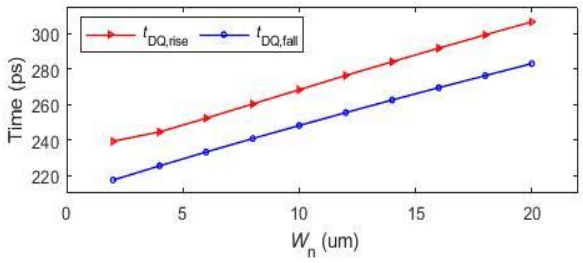

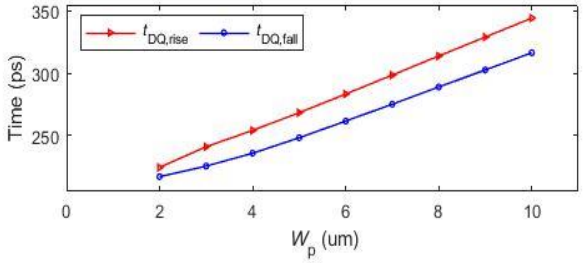

(c)

Fig. 4. (a) Duty, (b) rising/falling time, and (c) D-Q delay of the output signal of the CML/CMOS converter sweeping width of the NMOSs or PMOSs. (Default NMOS width is 10um and PMOS width is 5um.)

For simplicity of calculation, the body effect and the channel-length modulation are neglected. Due to the PMOS current mirror, M_3 and M_4, I_{REF} and I_{out} have same magnitude. So I_{out} can be derived as following:

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R_b^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (3)$$

I_{out} can be chosen by sizing not only W/L of the NMOS, but also the resistance R_b. In this paper, an external resistor is used for R_b.

However, in practice, I_{out} varies as V_{DD} changes due to the channel-length modulation. For stable current reference, the variation should be diminished. A simple differential amplifier is inserted in the circuit to solve this problem [10]. The amplifier makes output impedance of M_2 larger and stabilizes drain voltage of M_1 and M_2 in a certain level. Then the dependency of I_{out} on V_{DD} gets weaker.

Though supply voltage is turned on, entire circuit would not be turned on. The reason of this is that no current flows through the circuit before the supply voltage is turned on, so gate voltage of M_3 and M_4 follows V_{DD}, then M_3 and M_4 are not turned on. To solve the problem, the start-up circuit is necessary. A small NMOS M_{SU2} makes a current path from gate of M_3 and M_4 to drain of M_1 so that M_3 and M_4 can be turned on. The start-up circuit should be turned off after the beta-multiplier is turned on. M_{SU3} and M_{SU4} can be replaced to a small capacitor to prevent steady current through the start-up circuit.

In order to stabilize the circuit, MOSCAP M_C should be added in the output of the reference.

III. RESULTS AND DISCUSSIONS

The proposed circuit is simulated in TSMC 180nm CM process. The current source of a comparator is biased at 409uA. Input CML signal has 200MHz, 1.2V common-mode level, 400mV peak-to-peak, and 300ps rising/falling time. All transistors have same length, 200nm. Except current source of the comparator, every NMOS in the comparator is identical, but two NMOS transistors in node P in Fig. 2 have 2 fingers. In other words, M_9 and M_{10} have double width of M_1 and M_2. Every PMOS is identical. In this paper, duty, rising/falling time, and D-Q delay of output signal of the CML/CMOS converter are plotted, sweeping NMOS or PMOS width.

In Fig. 4. (a), when width of NMOS, W_n, is short, duty and W_n are inverse proportional. When W_n is 6um, duty is optimized at 50.37%. Fig. 4. (b) and (c) show that rising/falling time and D-Q delay are proportional to W_n. With small W_n, the rising/falling time has best value of 29.6ps and 27.1ps, respectively. Optimized D-Q delay is 239ps and 217ps for rising and falling, respectively.

Fig. 4. (a) shows that the duty of the output signal is proportional to W_p. Optimized value of the duty is 50.14%. According to Fig. 4. (b), when W_p is small, rising/falling time are inverse proportional to W_p. The rising/falling time have

optimized value of 33.3ps and 31.8ps respectively when W_p equals 4um. According to Fig. 4. (c), D-Q delay is proportional to the W_p in every region. The best value of D-Q delay is 224ps for rising and 216ps for falling.

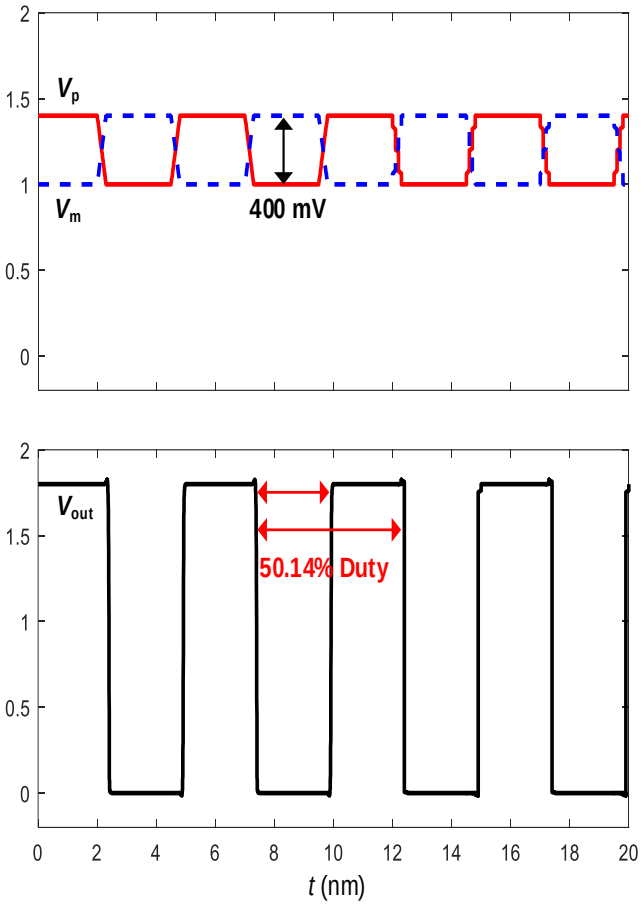

Fig. 5. The transient response of the optimized CML-CMOS converter.

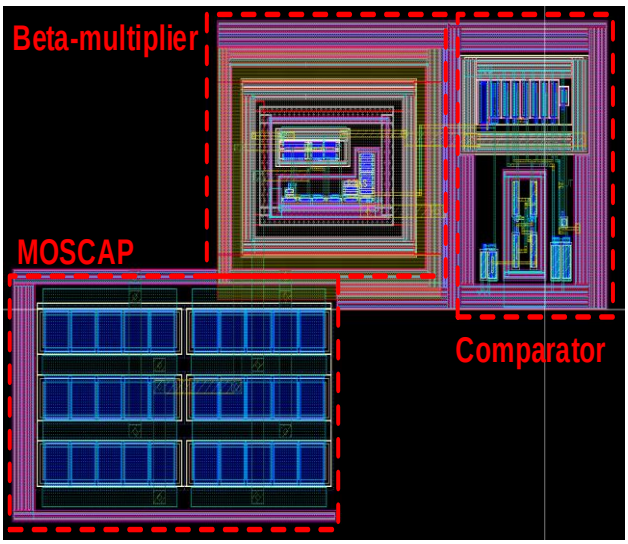

Fig. 6. A layout structure of the CML-CMOS converter.

TABLE I. A summary of the simulations

Parameter	This paper
CMOS Technology (nm)	180
CML signal frequency (MHz)	200
CML signal t_{rise}, t_{fall} (ps)	300
Optimized duty (%)	50.14
Optimized t_{rise} (ps)	29.6
Optimized t_{fall} (ps)	27.1
Optimized $t_{DQ,rise}$ (ps)	224
Optimized $t_{DQ,fall}$ (ps)	216

The parasitic capacitances of the transistors proportionally increase as the dimensions of the devices get bigger. Due to the dependency of parasitic capacitances on the dimension of the transistors, the delays of the circuit increase as the dimension of devices gets larger. Fig. 4. (b) shows the dependency of the rising/falling time on the size of the transistors.

Fig. 5 is the simulated transient response of the optimized CML-CMOS converter. The differential CML input signals have 400mV peak-to-peak, 250MHz, and 300ps rising/falling time. The converter amplitudes the input signals to rail-to-rail output signal with 50.14% duty. The rising/falling time is also optimized. A summary of the simulations is in Table I.

Fig. 6 is a layout structure of the CML-CMOS converter. The input driving transistors of the comparator are designed in common-centroid structure to minimize an effect of process variations. To equalize the current through current mirrors in the circuit, every current mirror is also designed in common-centroid. Since latch-up problem in the fabrication process is critical, all of the pairs of transistors have guard rings. Since a long metal path makes additional parasitic capacitances and resistances in the circuit, the layout is carefully designed to minimize an area of metal layers. The comparator has $30\times40um^2$ size. The beta-multiplier has $40\times35um^2$ size. The MOSCAP takes up an area of $61\times30um^2$. Total area of the CML-CMOS converter is $121\times74um^2$.

IV. CONCLUSION

To make an ideal-close square wave, CML-CMOS converter is proposed in this paper. The analog comparator is widely used to perform this role. Because of the positive feedback of the comparator, the small swing input signal can be widened to rail-to-rail signal. To make the output signal closer to ideal, sizing transistors should be held carefully. Several simulations in this paper give an advice to this decision. In terms of the duty, it is best when W_n is 6um and W_p is 2um. To minimize rising/falling time, W_n should be minimized and W_p is preferred to be 4um. Both W_n and W_p

should be minimized with regard to D-Q delay. Depending on what the designer wants to optimize for the top priority, most optimized values of dimensions of the transistors have to be chosen.

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