Design of a 520-624-GHz Amplifier-Frequency-Doubler Chain in 250-nm InP HBT Technology

Myeongjae Kim[1], Minseok Choi, Giyeong Nam, Wooyong Keum and Jae-Sung Rieh[a]
Department of Electrical Engineering, Korea University
E-mail : [1]2020171021@korea.ac.kr

***Abstract* - In this study, an Amplifier-Frequency-Doubler Chain (AFDC) operating around 600 GHz has been designed based on 250-nm InP HBT technology. It consists of a 300-GHz drive amplifier followed by a 600-GHz frequency doubler. The drive amplifier adopts a four-stage cascode topology, in which a staggering matching scheme is used to achieve a wide bandwidth. Additionally, to saturate the subsequent frequency doubler, load-pull matching is adopted for the output matching of the amplifier. The frequency doubler is based on a push-push topology followed by an output matching network that helps to suppress the undesired fundamental and odd-order harmonics. The integrated AFDC exhibited a simulated peak output power of -8.4 dBm, with a 3-dB bandwidth of 104 GHz (520-624 GHz), or a fractional bandwidth of 20.7% at 0-dBm input power. The simulated total DC power consumption is 282.6 mW. The layout size is 1137 × 464 μm², including probing pads.**

***Keywords*—250-nm InP HBT, Frequency multiplier, Terahertz band**

I. INTRODUCTION

The terahertz band (0.1-10 THz) attracts interest as a solution to realize ultra-high-speed communication systems and high-resolution radar systems [1], [2]. A high-performance signal source is essential to implement terahertz systems. In particular, wideband characteristics are highly desired for some key applications, such as high data rate wireless communication transceivers with a wide channel bandwidth and high resolution FMCW radar systems with a wide chirp bandwidth [3].

The widely adopted approaches for implementing a terahertz source are oscillator [4-7] and amplifier multiplier chain (AMC) [8, 9]. On-chip oscillators benefit from the fact that they do not require additional off-chip signal source unless signal locking needs to be employed. On the other hand, AMCs can implement relatively wideband sources, making them more suitable for achieving high-resolution radar systems. For these reasons, a terahertz source using an AMC is an attractive approach for various applications that require wideband operation.

a. Corresponding author; jsrieh@korea.ac.kr

Manuscript Received Oct. 11, 2024, Revised Nov. 18, 2024, Accepted Dec. 24, 2024

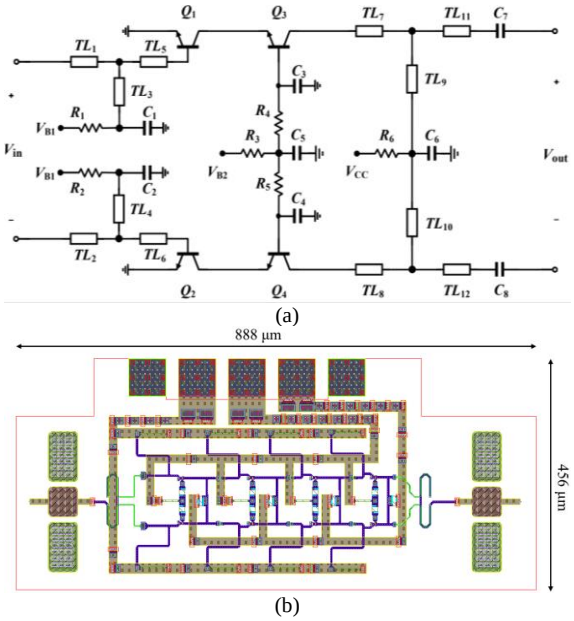


Fig. 1. (a) Schematic of the unit cell and (b) layout of the 300-GHz drive amplifier.

As for the semiconductor technology to implement the circuits, it is true that the performance of Si-based technologies, such as CMOS or SiGe BiCMOS, has been significantly improved in recent years, making Si-based terahertz circuits feasible options. However, compound semiconductor technologies including HBT and HEMT technologies are still more viable candidates for terahertz applications owing to the higher device operation speed. In this work, a 250-nm InP HBT technology that exhibits f_{max} of 850 GHz and 4.5-V common-emitter (CE) breakdown voltage (BV_{CEO}) has been adopted [10, 11]. allowing for amplifier design in the 300-GHz band as required in this work.

The rest of this work is organized as follows. In Section II and III, the design and analysis the 300-GHz drive amplifier and 600-GHz frequency doubler, respectively, will be presented. The design and analysis of the integrated 600-GHz AFDC will be discussed in Section IV. Finally, Section V concludes this study.

II. 300-GHZ DRIVE AMPLIFIER

Fig. 1 shows the schematic of the unit cell and the layout

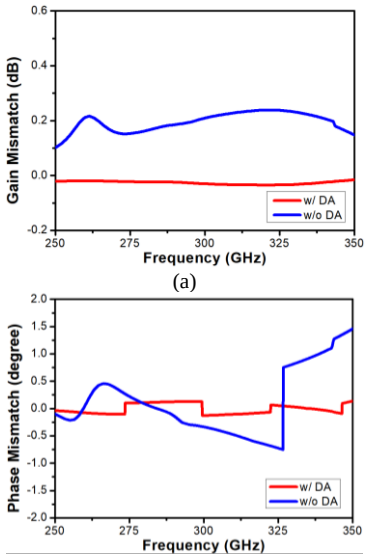


Fig. 2. Simulation results of Marchand balun with and without drive amplifier: (a) gain mismatch and (b) phase mismatch.

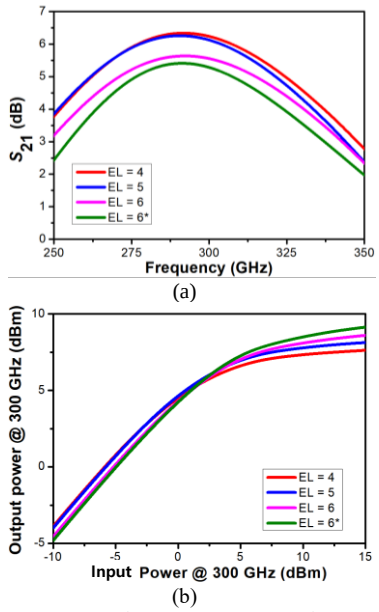


Fig. 3. Simulation results of the unit stage amplifier: (a) small-signal gain and (b) output power vs. input power for amplifiers at 300 GHz for various emitter length (EL).
* : load-pull matched output stage.

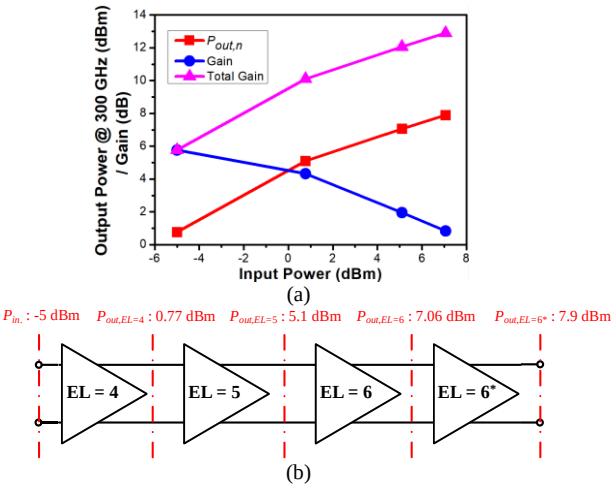


Fig. 4. Analysis based on harmonic balance simulation results of the 300-GHz drive amplifier: (a) output power and large signal gain vs. input power, and (b) power level which is obtained using a differential power probe component.
* : load-pull matched output stage.

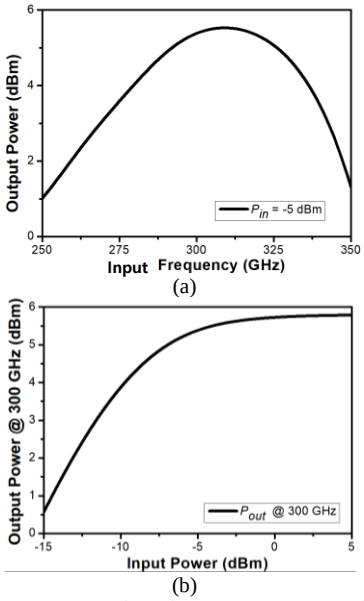


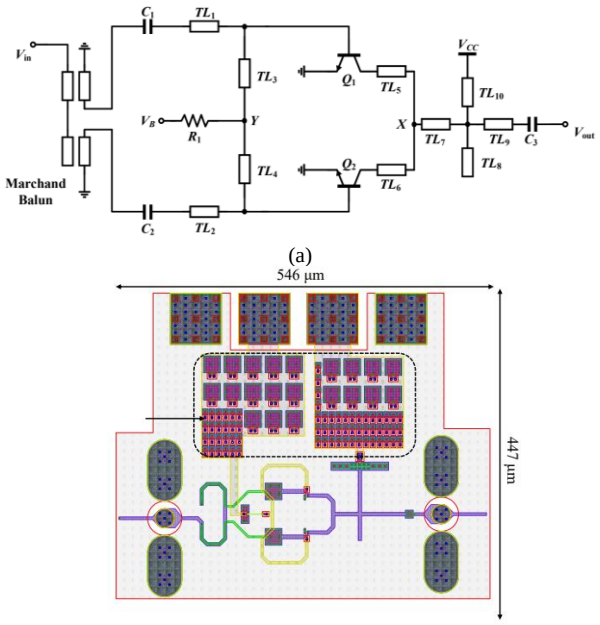
Fig. 5. Simulation results of the four-stage drive amplifier: (a) output power vs. input frequency with -5-dBm input power, and (b) output power vs. input power at 300 GHz.

of the designed 300-GHz four-stage drive amplifier. The layout size is 888 × 456 μm^2. A staggering scheme is adopted to achieve a wide 3-dB bandwidth, although it lowers the maximum gain. With this scheme, stages 1 and 2 are conjugately matched at 280 GHz, while stages 2 and 3, as well as stages 3 and 4, are conjugately matched at 320 GHz. To maximize the gain and compensate for the side effects of the staggering scheme, a cascode topology is adopted, which exhibits higher MAG than other configurations [12].

Resistors R_1, R_2 and R_3 are added to apply a stable DC voltage to the bases of the Q_1 to Q_4. Resistor R_6 is added to apply a stable DC voltage to the collector of the Q_3 to Q_4. Resistors R_4 and R_5 are added for stability. To apply V_{B1} to the transistors and match the input, TL_1 to TL_6 are employed. TL_7 to TL_{12} are used to provide stable V_{CC} and output matching. As shown in Fig. 1 (b), bypass capacitors are added to the base and drain bias lines, to enforce a virtual ground at the end of the short stub. A base bias V_{B1} of 1.1 V, V_{B2} of 2.8 V and a collector bias V_{CC} of 3.9 V are applied.

To facilitate a single-ended measurement, a Marchand balun was included at the input and output of the differential amplifier. The differential structure inherently suppresses the common-mode signal. As shown in Fig. 2, when only the Marchand balun is simulated with S-parameters, there is a gain difference of 0.2 dB and a phase difference of 0.34° at 300 GHz. However, after passing through the drive amplifier, the gain mismatch is compensated, and the phase difference is reduced to 0.12°.

A tapered scheme is adopted for device size selection to optimize the gain and output power of the amplifier. An



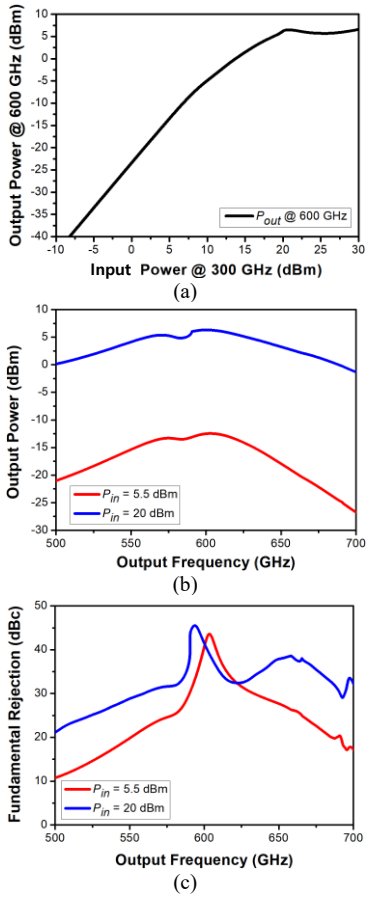
(a)

(b)

Fig. 6. (a) Schematic and (b) layout of the 600-GHz frequency doubler.

analysis based on harmonic balance simulation was performed for optimization, using Keysight Advanced Design System (ADS). In the simulation, the power was obtained using a differential power probe component. Fig. 3 (a) and (b) show the gain and output power of the unit stage amplifier, respectively, where both the input and output are matched for EL=4, 5, and 6. For the load-pull matched case, EL=6 was selected. Each case exhibits gains of 6.2 dB, 6.1 dB, 5.6 dB, and 5.3 dB at 300 GHz with corresponding output powers of 7.3 dBm, 7.8 dBm, 8.1 dBm, and 8.5 dBm, respectively, at an input of 10 dBm. With an input power of -5 dBm, each case exhibits output powers of 0.77 dBm, 0.71 dBm, 0.15 dBm, and -0.04 dBm at 300 GHz, respectively. The simulated results indicate that the EL=4 case shows the highest gain but the lowest saturated output power, while the EL=6 load-pull matched case shows the lowest gain but the highest saturated output power. As shown in Fig. 3, the output power and the gain of the amplifier are determined by input power level and emitter length. Consequently, the emitter length (EL) of each stage is selected based on the expected input power level. For this purpose, the emitter length of the first stage is set to 4 μm to amplify the input signal, which is assumed to be below 0 dBm. The EL for the second stage is set to 5 μm, and for the third and final stages, it is set to 6 μm. Additionally, the output stage of the drive amplifier is load-pull matched to optimize saturated output power.

To ensure that the load-pull matched last stage operates in saturation, the preceding stages are designed to amplify the signal to the desired power level. For instance, consider that an input power of -5 dBm is applied to the first stage of the drive amplifier. As shown in Fig. 3 (b), the first stage amplifies the signal up to 0.77 dBm, which is then fed into the second stage. The output power of the second stage is 5.1 dBm, and the signal is further amplified to 7.1 dBm by the third stage. The load-pull matched last stage amplifies the 7.1 dBm input power to 7.9 dBm. Note that the gain per stage



(a)

(b)

(c)

Fig. 7. Simulation results of the 600-GHz frequency doubler: (a) output power vs. input power, (b) output power vs. output frequency, and (c) fundamental rejection vs. output frequency.

is degraded toward latter stages as the transistors are increasingly saturated with the higher input power entering each stage. An Analysis of the output power of the drive amplifier is summarized in Fig. 4. The simulation results of the four-stage drive amplifier are shown in Fig. 5. In the simulation, the power was obtained using a grounded power probe component. For an input power of -5 dBm, the amplifier exhibits an 80.7 GHz (264.3 – 345 GHz) 3-dB bandwidth and a peak output power of 5.5 dBm at 308 GHz. Note that this output power is slightly lower than the expected 7.9 dBm with the fully differential configuration, which is due to the mode conversion by the Marchand baluns located at the input and output ports of the amplifier.

III. 600-GHZ FREQEUNCY DOUBLER

Fig. 6 shows the schematic and layout of the designed 600-GHz frequency doubler. The layout size is 546 × 447 μm^2. The frequency doubler consists of a doubler core and a second harmonic output stage, adopting a push-push structure to suppress the fundamental and odd-mode harmonics. Additionally, the even harmonics other than the second harmonic at the common collector node of Q_1 and Q_2 are filtered out with the output stage matched for the second harmonic.

The EL of the device is set to 6 μm, with a base bias of 0.7 V and a collector bias of 1.1 V applied. A resistor R_1 is added to apply a stable DC voltage to the bases of the Q_1 and Q_2.

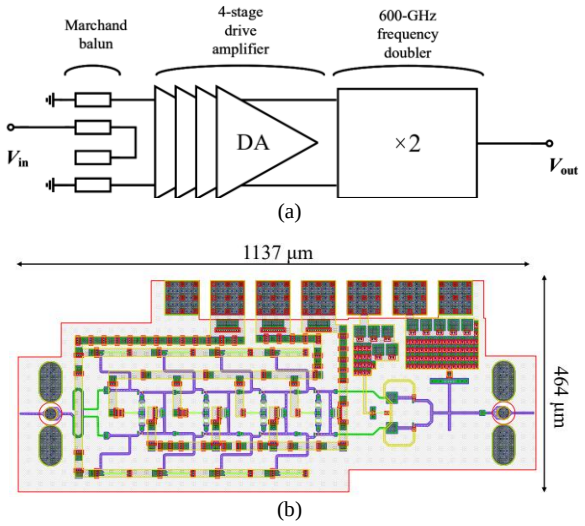


Fig. 8. 600-GHz Amplifier-Frequency-Doubler Chain (AFDC) designed in this work: (a) block diagram, and (b) layout.

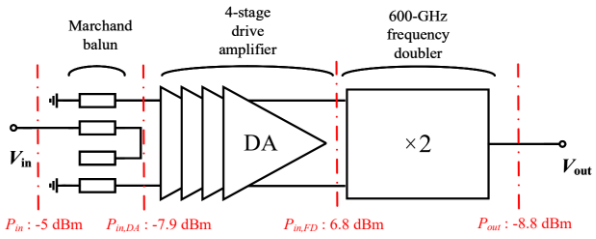


Fig. 9. Simulation results of power level power level obtained using a power probe component.

By implementing TL3 and TL4, the virtual ground node Y in differential mode is converted into an open circuit when viewed from the bases of the Q_1 and Q_2. In terms of common-mode signal, in contrast, the virtual open node Y is converted into short circuit when viewed from the bases of the Q_1 and Q_2. To apply V_{CC} to the collectors and simultaneously match the output, TL_5 to TL_{10} are used to configure the output stage. To convert single-ended signal to differential signal, a Marchand balun is placed at the input of the doubler. As shown in Fig. 5 (b), bypass capacitors of two sizes are added to the base and drain bias line, to enforce a virtual ground at the end of the short stub.

A harmonic balance simulation was performed for the analysis, using a grounded power probe to obtain power. Fig. 7 (a) shows the simulated output power of the circuit with the input power variation. The frequency doubler exhibits a saturated output power of 6.3 dBm, indicating that it requires at least 20 dBm of input power at the input port. As shown in Fig. 7 (b), which shows the output power as a function of frequency, the 3-dB bandwidth of the frequency doubler is 85.8 GHz (549.2 – 635 GHz) at an input power of 5.5 dBm. With this condition, a peak output power of -12.5 dBm was obtained at 603 GHz under the saturation condition. With a higher input power level of 20-dBm, the doubler exhibits a 108.2 GHz (541– 649.2 GHz) 3-dB bandwidth and a peak output power of 6.3 dBm at 600 GHz. Fig. 7 (c) shows the simulated fundamental rejection of the circuit as a function of frequency. The fundamental rejection is larger than 19.6 dBc throughout the entire 3-dB bandwidth.

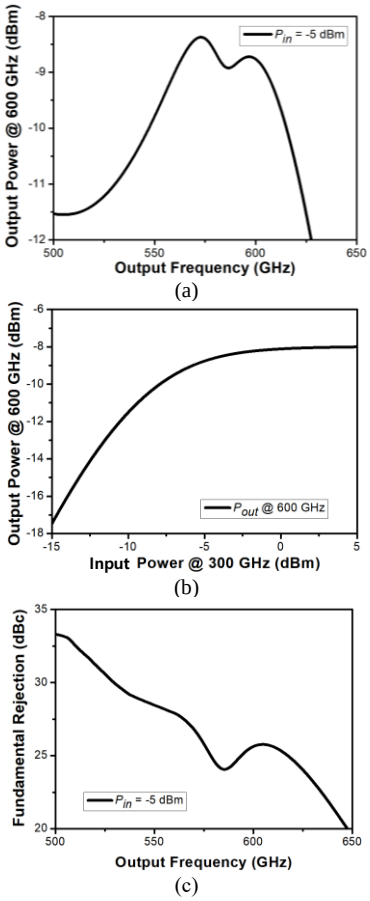


Fig. 10. Simulation results of the 600-GHz Amplifier-Frequency-Doubler Chain (AFDC): (a) output power vs. output frequency with -5-dBm input power, (b) output power vs. input power at 300 GHz, and (c) fundamental rejection vs. output frequency.

IV. 600-GHZ AMPLIFIER FREQUENCY DOUBLER CHAIN

The drive amplifier and the frequency doubler described above are integrated to realize an Amplifier-Frequency-Doubler Chain (AFDC), which upconverts the input signal from 300 GHz to 600 GHz. Fig. 8(a) shows the block diagram of the AFDC, which also includes a Marchand balun located at the input for single-end to differential conversion for test purpose. The inclusion of the Marchand balun may cause phase mismatch, amplitude mismatch, and loss, which can be compensated by the drive amplifier that follows as discussed earlier with Fig. 2.

Fig. 9 shows the power level at various points of the integrated AFDC obtained with harmonic balance simulation. An input signal of -5 dBm is applied to the Marchand balun, where it is converted to a differential signal with a finite loss. The power level of the signal at the drive amplifier input is -7.9 dBm, simulated using a differential power probe. The signal is then amplified by the amplifier up to 6.8 dBm and upconverted to the second harmonic by the push-push structure of the frequency doubler. The final single-ended output power is -8.8 dBm at 600 GHz by simulation.

Fig. 10 shows the simulated output power and fundamental rejection of the AFDC. For a -5 dBm input

TABLE I. Performance Comparison of 600-GHz Amplifier-Multiplier-Chain.

	*This work	[8]	[9]
Technology	250-nm InP HBT	35-nm mHEMT	65-nm CMOS
Multiplication factor	×2	×6	×30
3-dB BW (GHz)	520 - 624	553 - 612	582 - 612
**Frequency (GHz)	573	576	*600
Peak P_{out} (dBm)	-8.4	-8	*-12.8
P_{DC} (mW)	282.6	-	378
Chip size (mm^2)	1137 × 464	1750 × 500	1360 × 460

* : Simulated results.
** : Frequency at peak P_{out}.

signal, the AFDC exhibits a 3-dB bandwidth of 104 GHz (520–624 GHz) with a -8.4 dBm peak output power at 573 GHz. The fundamental rejection is larger than 24 dBc throughout the entire 3-dB bandwidth. The saturated output power is -8.8 dBm at 600 GHz. Corresponding DC power consumption is 282.6 mW. Compared to the previously simulated saturated output power of 6.3 dBm for the individual frequency doubler, the output power is slightly lower. This is due to the actual input power delivered to the frequency doubler being smaller than the assumed input power of 20 dBm in the previous case. Table I summarizes the results of the recently reported Amplifier-Multiplier-Chain around 600 GHz. The proposed AFDC exhibits the widest bandwidth among the chipsets.

V. CONCLUSION

In this study, a 600-GHz AFDC has been designed based on a 250-nm InP HBT technology. The AFDC exhibits 104 GHz 3-dB bandwidth with a peak output power of -8.4 dBm at 573 GHz. As for the saturated output power, -8.8 dBm was obtained at 600 GHz by simulation, with A DC power consumption of 282.6 mW. Individual frequency doubler and drive amplifier were also designed and characterized. The designed AFDC is expected to be applied for various THz applications that require with bandwidth.

ACKNOWLEDGMENT

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean government (NRF-2021R1A2C3009096). The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

REFERENCES

[1] J.-S. Rieh and SpringerLink, *Introduction to Terahertz Electronics*, 1st 2021. ed. Cham: Springer International Publishing : Imprint: Springer (in English), 2021.

[2] G.-S. Park, M. Tani, J.-S. Rieh, and S.-y. Pak, *Advances in terahertz source technologies*, First edition. ed. Singapore: Jenny Stanford Publishing (in English), 2024.

[3] B. R. Mahafza, *Radar systems analysis and design using MATLAB*, Fourth edition. ed. Boca Raton: Chapman & Hall/CRC (in English), 2022.

[4] L. Gao and C. H. Chan, "A 0.68–0.72-THz 2-D Scalable Radiator Array With –3-dBm Radiated Power and 27.3-dBm EIRP in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 10, pp. 3114-3124, 2022-10-01 2022, doi: 10.1109/jssc.2022.3178721.

[5] L. Gao and C. H. Chan, "A 144-Element Beam-Steerable Source Array With 9.1-dBm Radiated Power and 30.8-dBm Lensless EIPR at 675 GHz," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 2, pp. 375-387, 2024-02-01 2024, doi: 10.1109/jssc.2023.3308095.

[6] H. Son, J. Kim, K. Song, D. Kim, J. Yoo, and J.-S. Rieh, "600-GHz High-Power Signal Sources Based on 250-nm InP HBT Technology," *IEEE Transactions on Terahertz Science and Technology*, vol. 12, no. 6, pp. 648-657, 2022-11-01 2022, doi: 10.1109/tthz.2022.3202045.

[7] H. Son, J. Yoo, D. Kim, and J.-S. Rieh, "A 700 GHz Integrated Signal Source Based on 130 nm InP HBT Technology," *IEEE Transactions on Terahertz Science and Technology*, vol. 13, no. 6, pp. 654-658, 2023-11-01 2023, doi: 10.1109/tthz.2023.3319607.

[8] U. J. Lewark, T. Zwick, A. Tessmann, H. Massler, A. Leuther, and I. Kallfass, "Active 600GHz frequency multiplier-by-Six S-MMICs for submillimeter-wave generation," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014-06-01 2014: IEEE, pp. 1-3, doi: 10.1109/mwsym.2014.6848294.

[9] B. Khamaisi, S. Jameson, and E. Socher, "A 0.58–0.61THz single on-chip antenna transceiver based on active X30 LO chain on 65nm CMOS," in *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, 2016-10-01 2016, vol. 5: IEEE, pp. 97-100, doi: 10.1109/eumic.2016.7777499.

[10] Z. Griffith, M. Urteaga, and P. Rowell, "220-GHz High-Efficiency Power Amplifiers in 250-nm and 130-nm InP HBT Technologies Having 14.4-25.0% PAE and 40-60 mW P_{out}," in *2024 IEEE/MTT-S International Microwave Symposium - IMS 2024*, 2024-06-16 2024: IEEE, pp. 966-969, doi: 10.1109/ims40175.2024.10600322.

[11] M. Urteaga *et al.*, "InP HBT Integrated Circuit Technology for Terahertz Frequencies," in *2010 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2010-10-01 2010: IEEE, pp. 1-4, doi: 10.1109/csics.2010.5619675.

[12] J. Kim, S. Jeon, M. Kim, M. Urteaga, and J. Jeong, "H-Band Power Amplifier Integrated Circuits Using 250-nm InP HBT Technology," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 2, pp. 215-222, 2015-03-01 2015, doi: 10.1109/tthz.2014.2387259.

Myeong Jae Kim received the B.S. degree in electronic engineering from Korea University, Seoul, South Korea, in 2024, where he is currently pursuing the Ph.D. degree at the School of Electrical Engineering. His current research interests include frequency multipliers and wireless transceivers for terahertz radar.

Min Seok Choi received the B.S. degree in electronic engineering from Korea University, Seoul, South Korea, in 2024, where he is currently pursuing the Ph.D. degree at the School of Electrical Engineering. His current research interests include mm-wave and sub-THz integrated circuits for radar systems.

Gi Yeong Nam received the B.S. degree and in electrical engineering from Dongguk University, Seoul, South Korea, in 2023. He is currently pursuing the M.S. degree in electrical and electronics engineering at Korea University, Seoul, South Korea. His research interest includes THz signal sources and oscillators.

Wooyong Keum received the B.S. degree in electronic engineering from Korea University, Seoul, South Korea, in 2021, where he is currently pursuing the Ph.D. degree at the School of Electrical Engineering. His current research interests include frequency synthesizers and wireless transceivers for terahertz radar.

Jae Sung Rieh received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1991 and 1995, respectively, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 1999. In 1999, he joined IBM Semiconductor R & D Center, where he was responsible for the development of high frequency SiGe HBT technologies. Since 2004, he has been with the School of Electrical Engineering, Korea University, Seoul, Korea, where he is currently a Professor. In 2012 and 2018, he was a visiting scholar at Submillimeter Wave Advanced Technology team (SWAT) in JPL, Pasadena, USA, and at High Speed Electronics Lab (HSEL) in UCLA, Los Angeles, USA, respectively. His major research interest lies in the mm-wave and terahertz devices and circuits. Prof. Rieh was a recipient of IBM Faculty Award (2004) and a co-recipient of IEEE EDS George E. Smith Awards (2002 and 2006) and IEEE Microwave and Wireless Component Letters Tatsuo Itoh Best Paper Award (2013). He has served as an Associate Editor of the IEEE Microwave and Wireless Components Letters (2006-2009) and the IEEE Transactions on Microwave Theory and Techniques (2010- 2013). He is the author of a book, “Introduction to Terahertz Electronics (Springer, 2021)” and a co-editor of a book, “Advances in Terahertz Source Technologies (Jenny Stanford Publishing, 2024)”