An Inductor-Less 28-Gb/s NRZ Optical Receiver Analog Front-End Optimization Using BAG in 28-nm CMOS

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Abstract **- This paper presents an optimized design methodology for an inductor-less 28-Gb/s NRZ optical receiver (ORx) analog front-end (AFE) using the Berkeley Analog Generator (BAG) in 28-nm CMOS technology. With the increasing demand for high-speed data transmission in optical inter-connects, achieving an optimal balance between gain, band-width, and noise in transimpedance amplifiers (TIAs) remains challenging. To address this challenge, optimization to maximize signal-to-noise ratio (SNR) is performed using BAG. Measured results of the ORx AFE demonstrate an input sensitivity of −8.5-dBm average optical power at 28-Gb/s, PRBS-7. This work highlights the potential of the BAG-based design framework for integration into advanced optical communication systems, facilitating future developments in high-speed optical inter-connects.**

Keywords**—Optical receiver (ORx), transimpedance amplifier (TIA), inductor-less, berkeley analog generator (BAG)**

I. INTRODUCTION

The rapid expansion of applications such as artificial intelligence, machine learning, the internet of things, cloud services, and mobile services has led to exponential growth in data traffic. As a result, data centers now require faster interconnect solutions. However, traditional electrical interconnects (EIs) are now limited in bandwidth and long-distance transmission. To overcome these challenges, optical interconnects (OIs) have been introduced. OIs offer higher bandwidth, reduced electromagnetic interference, and improved long-distance data efficiency compared to EIs, making them essential in this transition. Initially used for long-distance communication between data centers, OIs are now also being employed for short distance communication, less than 100-m within data centers. As the required bandwidth increases, the transmission distance of OIs is becoming progressively shorter [1].

As shown in Fig. 1, a typical OI consists of an optical transmitter (OTx), an optical fiber, and an optical receiver (ORx). OTx converts electrical data to optical signals and ORx converts the received optical signals back to electrical data. Generally, the analog front-end (AFE) of ORx comprises a photodiode (PD), a transimpedance amplifier (TIA), a main amplifier (MA), and, optionally, an equalizer. The PD converts the optical signal into a current signal. The TIA then converts this current signal into a voltage signal. The equalizer is used to enhance insufficient bandwidth. The MA amplifies the signal to the desired level, enabling the decision circuit that follows the AFE to make accurate decisions. Among these blocks, the TIA is the main circuit determining the sensitivity of the ORx. Additionally, it has a trade-off relationship between gain, bandwidth, and noise performance, making it challenging to achieve high gain, high bandwidth, and low noise simultaneously. The Berkeley Analog Generator (BAG) [2]-[4], a Python framework, offers an effective approach to address these challenges. By automating the design process, BAG enables post-layout simulations of numerous cases that consider parasitic elements. In this paper, we focus on maximizing the signal-to-noise ratio (SNR) using the proposed design methodology with BAG.

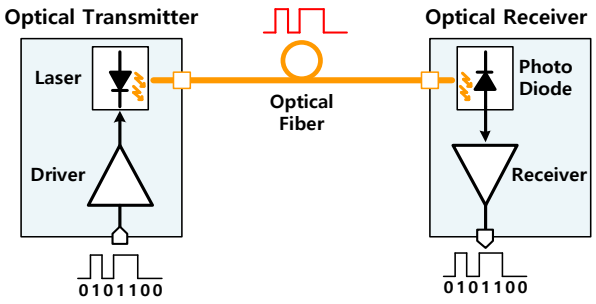

Fig. 1. Typical optical interconnect.

This paper is organized as follows. Section II describes the methodology for optimizing the ORx AFE using BAG. Section III details the optimized inductor-less ORx AFE. Section IV presents the measurement results, and Section V concludes this paper.

II. DESIGN METHODOLOGY FOR ORX AFE

Fig. 2 (a) shows the schematic of a single-stage inverter-based shunt-feedback TIA (SF-TIA). An inverter-based SF-TIA has a simple structure with minimal headroom issues and does not require an additional biasing circuit. By using the transconductance of both NMOS and PMOS, it achieves high

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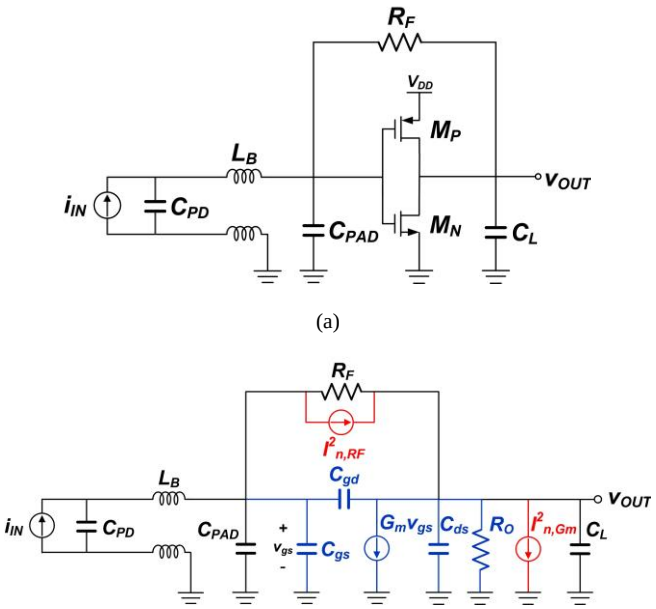


Fig. 2. Single-stage shunt-feedback inverter-based TIA (a) schematic and (b) small signal model.

linearity and a large transconductance with low power consumption.

Considering C_{gd} (miller effect) ([5] and [6]), the transimpedance is expressed as

$$Z_T(\mathrm{s}) = \frac{V_{out}(s)}{i_{in}(s)} = -R_T \cdot \frac{1 - s/\omega_z}{1 + s/(Q\omega_0) + s^2/\omega_0^2} \tag{1}$$

$$R_T = \frac{A_0 R_F - R_o}{1 + A_0} \approx R_F, \quad A_0 = G_m R_o \gg 1 \tag{2}$$

$$\omega_z = \frac{G_m - 1/R_F}{C_{gd}} \tag{3}$$

$$\omega_0 = \sqrt{\frac{1 + A_0}{R_F R_o \left(C_T C_{gd} + C_{out} C_{gd} + C_{out} C_T\right)}} \tag{4}$$

$$Q = \frac{\sqrt{(1 + A_0) R_F R_o \left(C_T C_{gd} + C_{out} C_{gd} + C_{out} C_T\right)}}{R_F\left[C_T + (1 + A_0) C_{gd}\right] + R_o (C_T + C_{out})} \tag{5}$$

where R_T is the transimpedance gain, $C_T = C_{PD} + C_{PAD} + C_{gs}$, and $C_{out} = C_L + C_{ds}$. The zero created by C_{gd} is generally at a higher frequency than ω_0 [6]. Therefore, with the Butterworth transfer function ($Q = 1/\sqrt{2}$), the 3-dB bandwidth follows as shown in [7]

$$BW_{3dB} = \frac{\omega_0}{2\pi} \sqrt{\sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1} + \left(1 - \frac{1}{2Q^2}\right)} = \frac{\omega_0}{2\pi} \tag{6}$$

The wire-bond inductance (L_b) sequentially charges the C_{PD} and $C_{PAD} + C_{gs}$ which improves the rise time compared to when capacitors are charged simultaneously (i.e., without

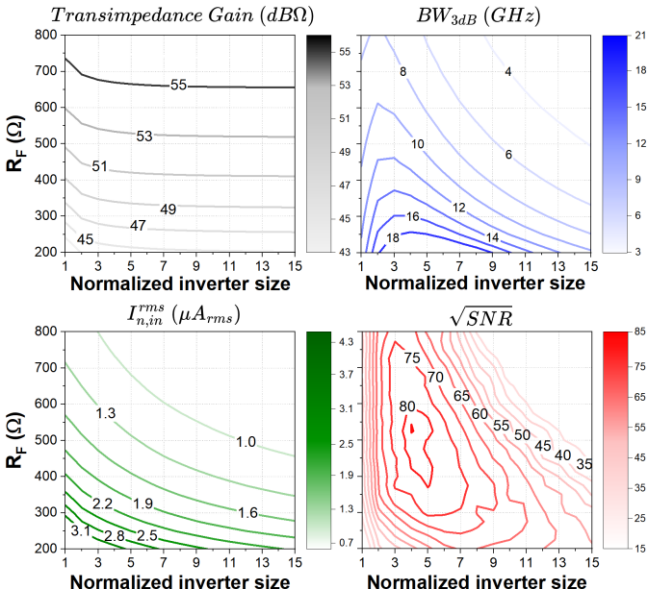


Fig. 3. the contour plot of the transimpedance gain, bandwidth, input-referred rms noise, and $\sqrt{SNR}$ with respect to inverter size and R_F of SF-TIA (C_{PAD}, $L_B = 400\ pH$, $C_L = 40\ F$) using BAG.

L_b). This results in the enhanced bandwidth [7]. In this work, based on previous bonding experience, optimization is performed with 400-pH.

The input-referred noise current power spectral density (PSD) of SF-TIA is expressed as [7]

$$I^2_{n,in,SF\text{-}TIA}(f) = I^2_{n,in,R_F}(f) + I^2_{n,in,Gm}(f) \approx \underbrace{\frac{4kT}{R_F}}_{I^2_{n,in,R_F}} + \underbrace{\frac{4kT\Gamma}{G_m R_F{}^2} + 4kT\Gamma\frac{(2\pi C_T)^2}{G_m} f^2}_{I^2_{n,in,Gm}} \tag{7}$$

From (4) and (7), increasing R_F reduces the white noise from both the resistor and the FET, which leads to a reduction in the input-referred noise current PSD, but it also results in a narrower bandwidth. The input-referred rms noise current, which is directly related to sensitivity, is expressed as [7]

$$i^{rms}_{n,in,SF\text{-}TIA} = \frac{v^{rms}_{n,SF\text{-}TIA}}{R_T} = \frac{1}{R_T}\sqrt{\int_0^\infty |Z_T(f)|^2\, I^2_{n,in,SF\text{-}TIA}(f)\, df} \tag{8}$$

where $v^{rms}_{n,SF\text{-}TIA}$ is the rms output noise. The value of $v^{rms}_{n,SF\text{-}TIA}$ is derived by integrating the noise voltage PSD referred to the output and subsequently taking its square root. Finally, the input-referred rms noise current is calculated by dividing the rms output noise by the transimpedance gain.

The SNR is calculated as [6]

$$SNR = \frac{\left(V_{tap(0)} - \sum_{n\neq 0}^{\infty} V_{tap(n)}\right)^2}{\overline{v^2_{n,out}}} \tag{9}$$

where the numerator is the worst-case eye height for a single bit response (225-μA_{pp} current pulse) and the denominator is the power of the output noise.

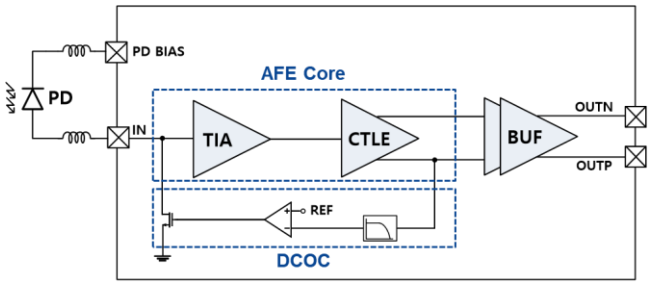


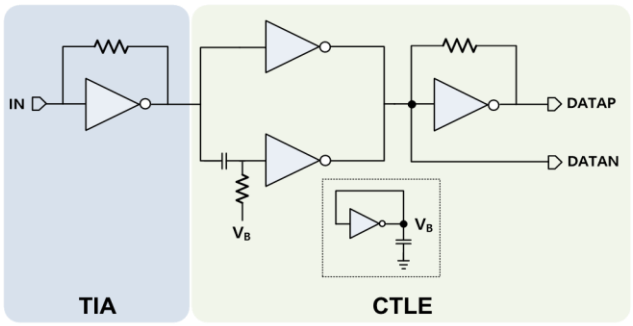
Fig. 4. Block diagram of the inductor-less ORx AFE.

Fig. 3 shows the contour plot of the transimpedance gain, bandwidth, input-referred rms noise, and SNR, obtained from post-layout simulations, varying with inverter size and R_F of SF-TIA using BAG. A normalized inverter size of 1 corresponds to an NMOS width of 4-μm and a PMOS width of 10-μm. As discussed in (2), the transimpedance gain is determined by the value of R_F. The relationship between inverter size and bandwidth shows that as the inverter size increases, the intrinsic gain (G_mR_o) remains constant, but the increased capacitance reduces the bandwidth of the TIA. As discussed in (7) and (8), increasing R_F reduces the input-referred noise rms current while simultaneously decreasing bandwidth. Notably, there are optimal points for gain, bandwidth, and noise, but they do not align. This highlights the trade-offs between these metrics. Therefore, the design is optimized to maximize the SNR, achieving a peak value of 83 at R_F = 550-Ω and normalized invert size of 4. However, the transimpedance gain of less than 60-dBΩ from a single-stage SF-TIA is insufficient. In the next section, we will further discuss the ORx AFE, which achieves higher transimpedance gain and SNR. Previous research [6] extracted various parameters through post-layout simulation of the unit cell-based layout and scaled them according to device size. Numerical analysis-based optimization was then performed. However, as circuit complexity increases, it becomes challenging to account for all parasitic components, making precise numerical analysis more difficult.

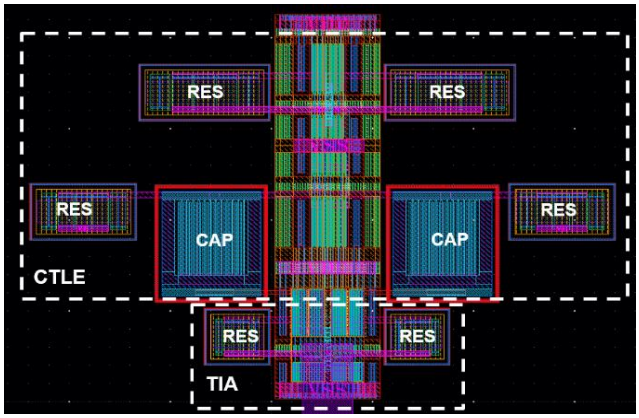
III. INDUCTOR-LESS ORX AFE OPTIMIZATION

On-chip inductors are used for high-performance TIAs [8]-[11]; however, they incur a high area cost. For multi-channel integration on the same die, minimizing chip area is crucial. In this paper, an inductor-less ORx AFE is implemented and optimized using the BAG. Fig. 4 shows the block diagram of the inductor-less ORx AFE. The AFE consists of a TIA, a continuous-time linear equalizer (CTLE), a DC offset cancelation (DCOC) loop, and an output buffer (BUF) for measurement. The current signal fed into the TIA contains a DC current, which limits the operating range of the circuit. To address this, the DCOC loop is employed to eliminate the unwanted DC current. The DCOC consists of a low-pass filter with 1.4-MHz cut-off frequency, an operational amplifier, and a transistor for the DC current sink. The AFE core, including the TIA and CTLE, is optimized using the BAG. The AFE core and BUF are all implemented using inverters.

Fig. 5 shows the detailed schematic and BAG layout of the AFE core. The TIA stage uses a single-stage SF-TIA. The



(a)



(b)

Fig. 5. AFE core (a) schematic (b) BAG layout.

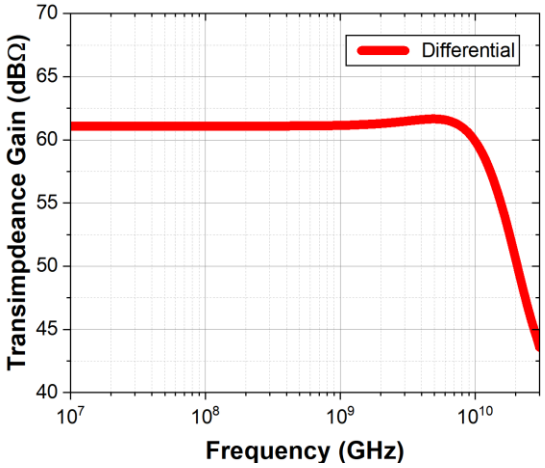


Fig. 6. Simulated AC response.

CTLE stage is implemented in a transadmittance-transimpedance (TAS-TIS) configuration. The low-frequency gain is provided through an inverter-type transconductor. The high-frequency gain is provided in a parallel path with high-pass filter and a transconductor which is biased by a diode-connected inverter. The output current of transconductors is converted back to voltage by the following TIS stage. To enhance matching, passive elements such as resistors and capacitors are arranged in a parallel layout. To enable the parametric sweep process in layout, all inverter size and resistance values within the TIA core are parameterized using the BAG. By performing a sweep of these parameters, a total of 972 layouts are generated, and post-layout simulations are conducted. The optimization is performed in a direction that maximizes the SNR

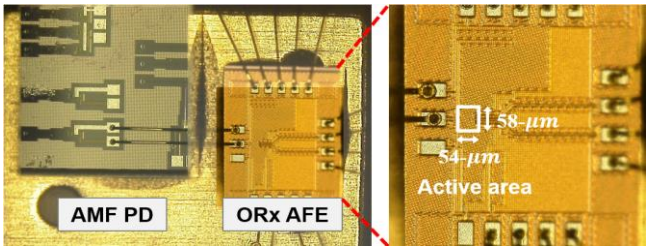


Fig. 7. Chip micrograph.

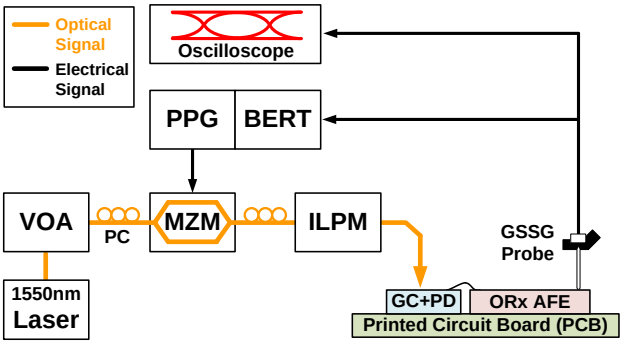


Fig. 8. Measurement setup.

of the DATAP and DATAN nodes, achieving a value of 110.8 at the data rate of 28-Gb/s. All simulations consider the PD model, PAD capacitance, wire-bonding inductance (400-pH), DCOC, and the BUF following the AFE core.

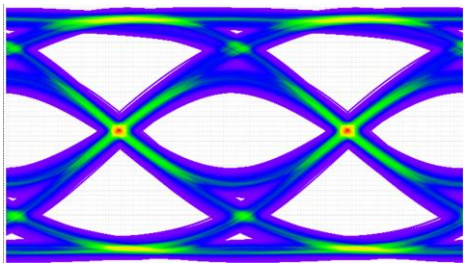
Fig. 6 shows the post-layout simulated AC response. Including the 50-Ω termination, the differential transimpedance gain and −3-dB bandwidth are achieved to be 61-dBΩ and 12.3-GHz, respectively.

IV. MEASUREMENT RESULTS

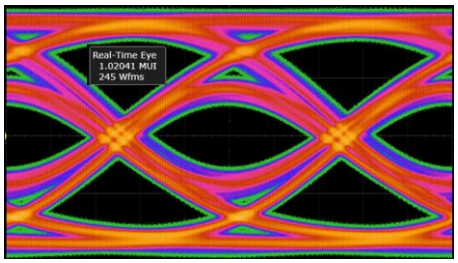
Fig. 7 shows the micrograph of the PD and the ORx AFE chip. The PD provided by the process design kit of Advanced Micro Foundry (AMF) process is used. The ORx AFE chip is fabricated using 28-nm CMOS technology. The total chip size is 1-mm × 0.78-mm. The ORx AFE occupies an area of 0.029-mm^2, while the active area excluding the filter of the DCOC loop is 0.0031-mm^2. The PD has a 0.9-A/W responsivity and an optical-to-electrical bandwidth of 23-GHz. Both dies are mounted on an FR4 PCB.

Fig. 8 shows the measurement setup. Optical measurements are performed using a tunable laser source operating at a wavelength of 1550-nm. The laser passes through a variable optical attenuator (VOA) and is then fed into a 40-Gb/s commercial Mach-Zehnder modulator (MZM). The RF input of the MZM is driven by a pulse pattern generator (PPG). Optical power is monitored by an in-line power monitor (ILPM) before reaching the PD. The grating coupler (GC) exhibits a coupling loss of 6-dB. The differential output of the ORx AFE is probed using an on-wafer GSSG probe. The electrical signals are captured by an oscilloscope and bit error rate (BER) is measured by the BER tester (BERT) module of the PPG.

Fig. 9 compares the simulated and measured 28-Gb/s eye diagram, demonstrating the effectiveness of the BAG-based design framework. The close match between simulation and measurement validates the accuracy of the proposed



(a)



(b)

Fig. 9. Eye diagram of ORx AFE for 28-Gb/s, PRBS-7 modulation data: (a) simulation and (b) measurement.

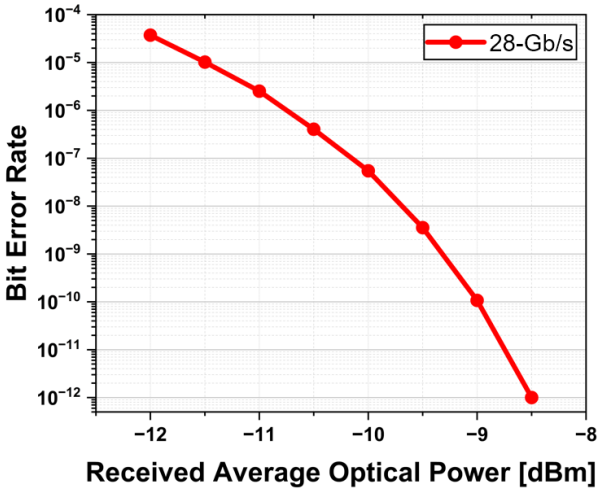


Fig. 10. Measured BER curve of ORx AFE for 28-Gb/s, PRBS-7 modulation data.

Fig. 11. Single-ended output voltage noise.

methodology for high-speed optical receiver design.

Fig. 10 shows the BER curve measured for 28-Gb/s, PRBS-7 modulation data, while varying the average optical power using the VOA. The BER less than 10^{-12} is achieved at the average optical power of −8.5-dBm. At this point, including the BUF, the ORx AFE consumes 34.8-mW from 1.2-V supply voltage, resulting in an energy efficiency of 1.24-pJ/bit.

Fig. 11 shows the single-ended output voltage noise distribution measured using an oscilloscope in the absence of an input signal [9], [12]. In the differential topology, the output voltages are anti-correlated, making the differential rms noise voltage twice the single-ended noise voltage [13]. After de-embedding the oscilloscope noise of 0.64-mV_{rms}, the input-referred rms noise current of the ORx AFE is

$$i_{n,in,rms} = \frac{2\times\sqrt{(1.28\ \text{mV})^2 - (0.64\ \text{mV})^2}}{10^{\left(\frac{61\ \text{dB}}{20}\right)}} = 1.99\ \mu\text{A}_{rms} \quad (10)$$

where the transimpedance gain of 61-dB is obtained from simulation result. Then, the average input-referred noise current density is given by

$$I_{n,in}^{\text{avg}} = \frac{i_{n,in,rms}}{\sqrt{\text{BW}}} = 17.9\ \text{pA}/\sqrt{\text{Hz}} \quad (11)$$

where the bandwidth of 12.3-GHz is obtained from simulation result.

TABLE I. Comparison of inductor-less optical receivers

	[14]	[15]	[16]	[17]	**This Work**
Process (nm)	28	28	65	40	28
Data rate (Gb/s)	17	25	25	25	28
Data pattern	$2^{31}-1$	-	$2^{7}-1$	$2^{15}-1$	$2^{7}-1$
Optical sensitivity @10^{-12}(dBm)	−4.3	−6.8	−0.2 *	−10.8	−8.5
Power efficiency (pJ/bit)	-	0.17	1.23	1.13	1.24 **
Total area (mm^2)	0.0025	0.0018	0.0056	0.007	0.029

* Optical modulation amplitude
** Including BUF power consumption

Table I compares the performance of our inductor-less ORx AFE with previously reported results. As shown in the table, this work achieves the highest data rate and best optical sensitivity at this rate.

V. CONCLUSION

This work demonstrates an optimized inductor-less 28-Gb/s NRZ optical receiver AFE in 28-nm CMOS technology. The design process carefully balances the trade-offs between gain, bandwidth, and noise to maximize the SNR through the proposed design methodology using the BAG. The ORx AFE achieves the optical sensitivity of −8.5 dBm at 28-Gb/s. This study highlights the potential of BAG-based design frameworks for high-speed optical interconnects.

ACKNOWLEDGMENT

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