Low-Noise EEG Sensor and Neural Stimulator: For Motion and Stimulation Artifact Removal

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***Abstract* – This work aims to develop a neural interface system that enables electroencephalogram (EEG) measurement in wearable equipment and eliminates stimulation artifacts by processing in miniaturized neural stimulation modules. The ASIC implements a 4-channel analog-front-end (AFE) with a high input-Z buffer, 2nd order oversampling delta-sigma ADC, stimulation noise cancellation digital processors, and digitally controlled neural stimulators into the chip. The simplified stimulation artifact rejection algorithm implemented on the digital block allows users to acquire pure neural signals while stimulating. The 3 mm x 1 mm IC chips were fabricated through the TSMC 65 nm LP process.**

***Keywords* – biopotential recording, neural recording, stimulation artifact, motion artifact, electroencephalography**

I. INTRODUCTION

Acquiring neural signals in a daily-life environment is an important research topic for biomedical engineers due to its usefulness. The daily-life electroencephalography (EEG) can fulfill the clinical needs for non-invasive monitoring of chronic diseases such as epilepsy [1], neurodegenerative disease, and depression disorders, and needs for other applications such as brain-machine interfaces and neuroscience research. For this reason, it has been researched to modify pre-existing clinical EEG systems to reduce the cumbersomeness of bio-potential recordings: development of dry or non-contact active electrodes to apply a more convenient user interface, miniaturized sizes, and extremely low noise for recording small amplitude biopotential.

Recently, the improvements in neural signal processing technique based on deep neural network and adaptive algorithm enables the quick and accurate classification/ interpretation of neural signals, and it provides the vision of the future applicability related to the daily-life EEG acquisition system. In addition, as research about the neural stimulator proceeds, the idea of a closed-loop neural interface by integrating the acquisition system, signal processor, and neural stimulator becomes a clear goal [2][3][4].

Designing an integrated system of daily-life EEG recorders and stimulators is a still challenging project, and many of the difficulties come from the artifact issues. The unstable electrode-tissue interface, especially in dry and non-contact cases, generates large motion artifacts that saturate the neural recorder and distort the signal. Moreover, in the integrated system, the stimulation artifacts also become a big issue. A large input perturbation is given to the neural recorder when the stimulator generates the output. The stimulation artifact causes a similar problem of saturating the neural recorder and missing the neural signals.

For decades, strategies for removing motion/stimulation artifacts have been researched and reported [5]. These artifacts cannot be easily removed by frequency filters, as the frequency spectra of users' everyday physical activities and the electrophysiological signals of the human body overlap. Modifying electrodes could provide a more stabilized electrode-tissue interface, and ASICs for recording EEG were introduced by boosting the input impedance and monitoring the interface changes to compensate for the artifact components [6]. Decomposition methods and algorithms (wavelet, ICA, PCA, etc.) to detect and remove motion/stimulation artifacts were reported as well. However, the post-recording process with heavy computational costs becomes an obstacle when applying the system in real-time environments.

This work aims to design a recorder and a neural stimulator that can satisfy the requirements for daily-life use. To record 4-channel EEG through the dry-contact interface, a high input impedance buffer and a low-noise oversampling delta-sigma ADC are integrated into one recorder channel [7]. An analog buffer at each channel is reset to the reference voltage in a short time (~1ms, short time considering the bandwidth of EEG) when the recorder generates saturated output so that it can prevent the loss of signal information and record the desired signal. Moreover, since the magnitude of the EEG motion artifact depends on the voltage across the input of the

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recording analog front-end and the skin contact, the reset reference voltage of the buffer can be controlled and adjusted by the magnitude of the motion artifact. [8]

On-chip digital block with a stimulation artifact removal algorithm is implemented to realize real-time signal processing. The IIR adaptive filter scheme and the simplified algorithm reduced the area and power consumption of the digital block [9] and allowed users to acquire pure neural signals while stimulating at a low cost. In bio-application charge mismatch during stimulation could induce tissue damage and corrosion of stimulation electrodes. The H-bridge structure is used to realize a charge-balanced biphasic stimulator.

II. DESIGN METHODOLOGY

A. EEG Recording AFE and ADC-Direct Neural Recording

The diagram of the EEG measurement module is shown in Fig. 1. Due to the high input impedance of the analog-front-end (AFE) buffer, EEG can be recorded without large signal attenuation. Also, by shielding the input node with the output of the buffer (i.e., active shielding), power line interference such as 50/60Hz noise is significantly reduced. Input is biased with a certain DC voltage level, and a digital DC servo loop is designed to prevent saturation of output and stabilize the overall system for using ADC output. The overall chip has 4-channel recording, which can improve the post-processing and analysis effect of the EEG paradigm signal.

The buffer in the AFE is designed to enable EEG recording without signal attenuation even with high electrode-skin interface impedance (ESI) and its variation. Active shielding by buffer minimizes the parasitic capacitance and can boost the input impedance. By utilizing this, very small fine EEG signals can be received through the analog front end.

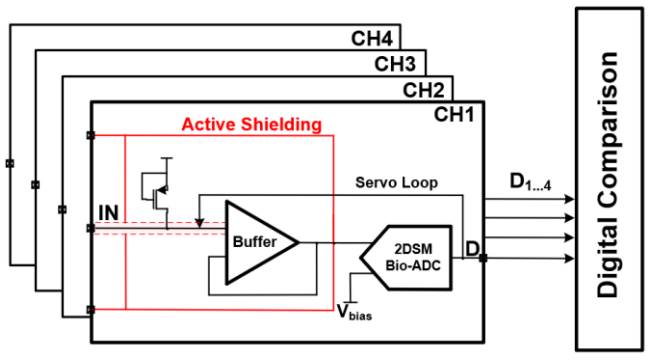


Fig. 1. Entire block diagram of the EEG measurement module.

The block diagram of neural recording Bio-ADC is shown in Fig. 2. The signal is integrated using the 2nd-order open-loop Gm-C integrator. The current reuse schematic is used in the amplifier of the integrator for high energy efficiency. Then, the dynamic comparator determines the value D which is the output sign of the comparison results by using the integrated signal. The system uses 2nd-order Delta-Sigma modulation ($\Delta^2\Sigma$) ADC, enabling ADC-direct neural recording without a separate amplification process. Chopper stabilization and oversampling perform noise-shaping, which improves the signal-to-noise ratio (SNR) by eliminating low-frequency noise such as flicker (1/f) noise. In addition, with the help of digital auto-ranging and prediction block, ADC output quickly follows the input signal when it fluctuates significantly due to large artifacts.

For example, if the ADC output sign is changed three times continuously, it increases the resolution of ADC. Taking these advantages of ADC, the overall system implements a digital DC servo loop that resets the input DC point back to the original bias point when a large artifact beyond a certain specific threshold is detected. The resolution of the input ADC can be controlled for up to 8 bits depending on the amount of change in the signal.

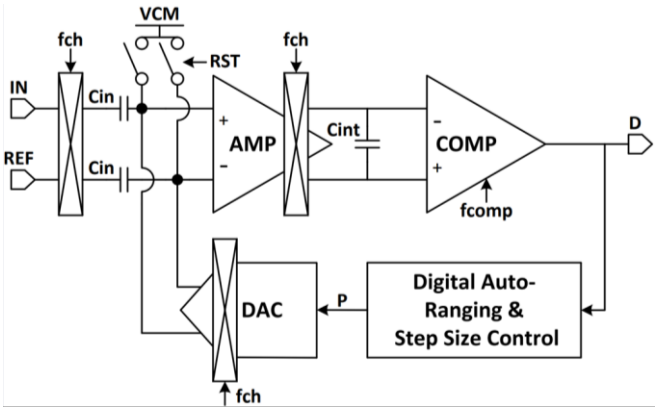


Fig. 2. Entire circuit diagram of neural recording Bio-ADC.

B. Stimulation Artifact Removal Algorithm

Basic assumptions behind the operation of the algorithm are as follows: 1) Neural signals can be removed by averaging throughout the time axis. (Fig 3); 2) Stimulation artifacts are identical, for at least a short period; 3) Stimulation artifacts contaminate neural signals in simple addition-based operation. The block diagram of the stimulation artifact removal algorithm is shown in Fig 4.

After reset, all parameters are set to the initial value. Parameters are changed using the SPI interface. During the operation, the stimulation artifact removal block (SARB) keeps checking whether stimulation occurs. If it recognizes stimulation, the stimulation artifact (SA) flag is turned on and maintained till the termination logic is conducted. While the SA flag is on, SARB keeps updating the artifact template for each sample. If the number of updated samples reaches the designated value, the termination logic operates and starts to wait for the next SA flag.

C. Charge-Balanced Stimulator

To prevent tissue damage and corrosion of electrodes, it is important to ensure the charge balance during stimulation. The stimulator uses an H-bridge structure to accomplish this design goal [10]. The H-bridge stimulator uses the same current source for both cathodic and anodic phases. Therefore, it easily makes charge-balanced biphasic stimulation.

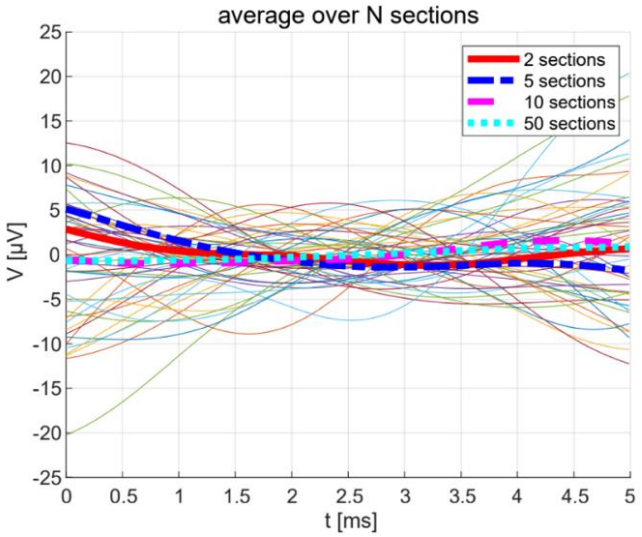


Fig 3. Change of neural signal data during template generation. The neural signal goes to zero when more time sections are averaged.

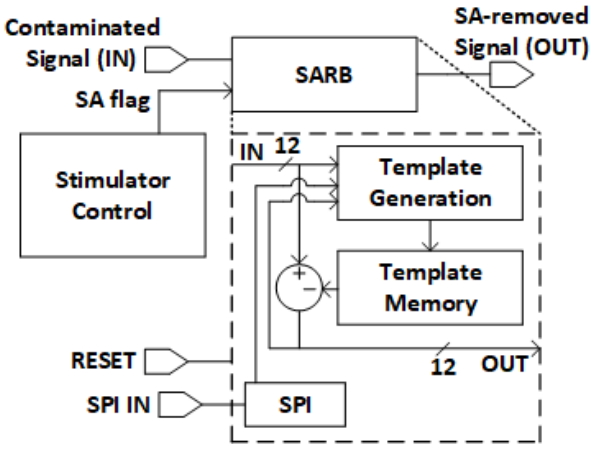


Fig. 4. Block diagram of stimulation artifact removal algorithm.

III. RESULTS AND DISCUSSIONS

The suggested design was implemented as IC chips. The layout picture is displayed in Fig. 5. The semiconductor chips were fabricated through the TSMC 65nm LP process and the functional profiles were measured through the following process.

A. EEG Recording AFE and ADC-Direct Neural Recording: simulations and measurements

Fig. 6 shows the simulation results of the IC that the designed circuit can measure the aimed biopotential signal. The surrogate signal whose magnitude and frequency spectrum mimic EEG is applied on the IC input and the ADC provides the output with the intended DC settling profile.

Fig. 7 shows the experiment setup and measured output signal of the buffer. In the experiment, AFE records the input signal well with negligible signal attenuation. Fig. 8 shows the ADC output results through the IC chip. It can record sub-mV EEG magnitude signals well.

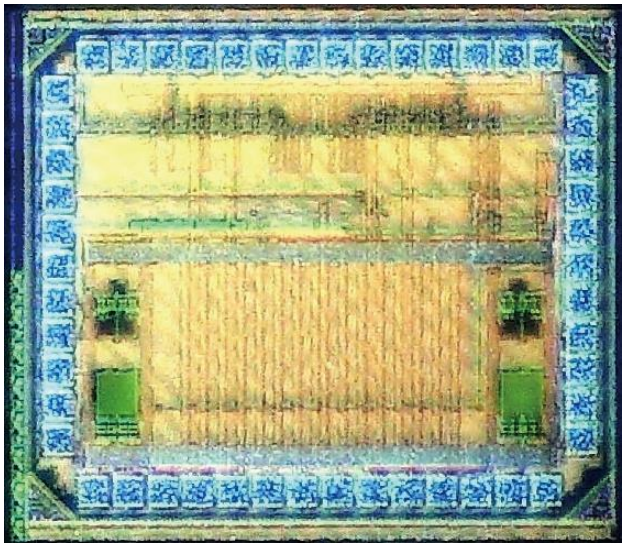


Fig. 5. Layout picture of neural stimulator with SARB.

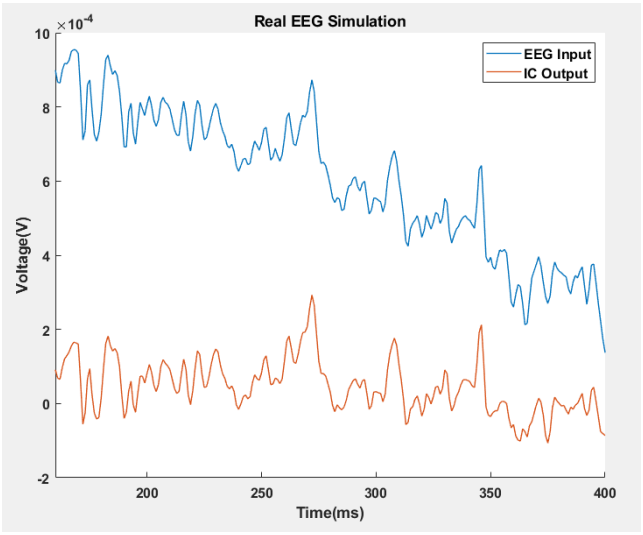
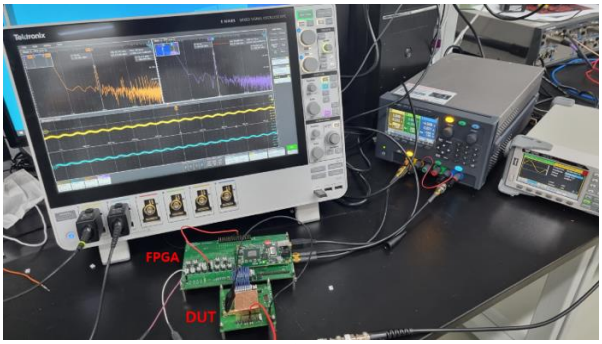
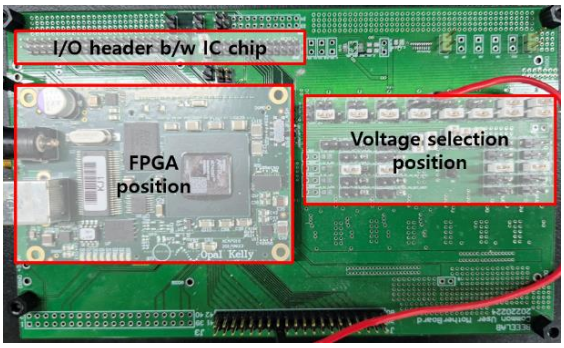
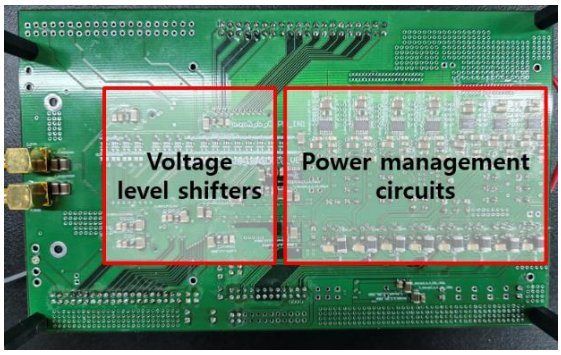


Fig 6. Simulation results when an EEG-like signal is applied on IC input (blue). ADC shows a well-recorded output signal (orange).

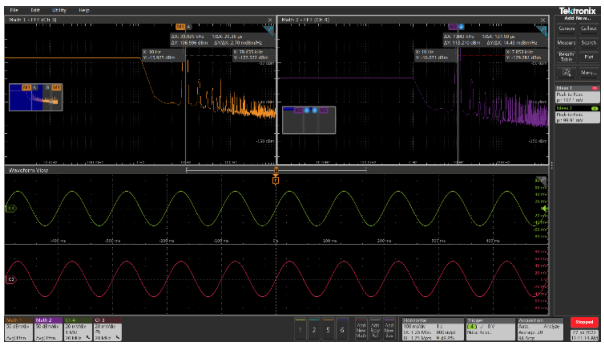


(a)



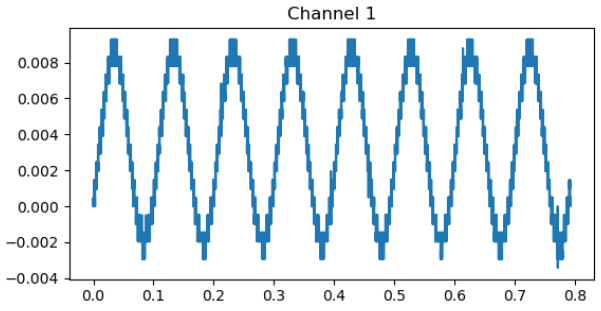


(b)

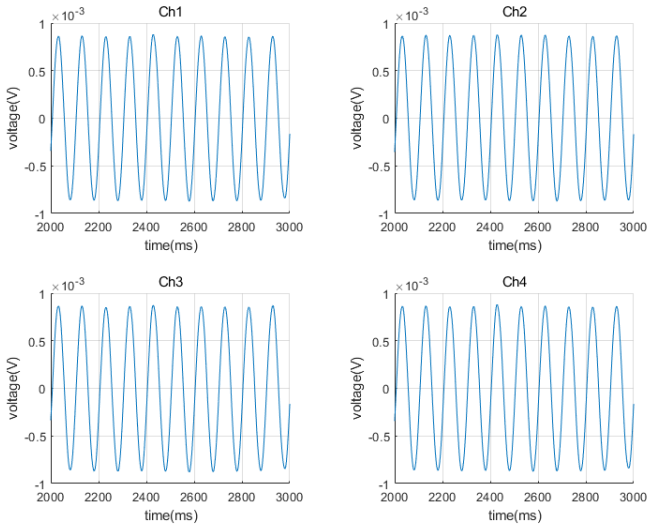


(c)

Fig 7. (a) Experiment setup for IC chip test measurement, (b) Test PCB board with FPGA, I/O header for communication with IC, voltage level shifter, and power management circuits, and (c) Input signal (green: time | orange: FFT) is recorded through the buffer and the output signal is shown (red: time | purple: FFT).



(a)



(b)

Fig 8. Output results when small signal is inserted into IC input: (a) <mV range signal can be recorded through overall IC in real-time and (b) 60Hz PLI noise is removed by postprocessing, then integrated buffer and ADC circuit can measure EEG-like magnitude signal with very low noise.

B. Neural Stimulation and the Artifact Removal

Fig. 9 shows the stimulation artifact removal result. Brain signal and stimulation artifact were recorded simultaneously by integrated ADC of the IC. Power line noise is removed by a 60Hz notch filter using MATLAB. Comparing before and after the stimulation artifact removal, clearly shows that an integrated stimulation artifact removal module can remove artifacts and recover neural signals.

Fig. 10 shows the Fourier transform of the notch-filtered raw signal, the artifact template, and the recovered neural signal. The FFT of the template shows an undesired distortion and it appears at the FFT of the recovered signal. If this distortion is higher than the neural signal floor, the processed IC cannot be used to recover the neural signal. However, the size of the distortion is less than -120dB which is smaller than the noise floor of the signal band (10~50Hz). Therefore, it can be ignored.

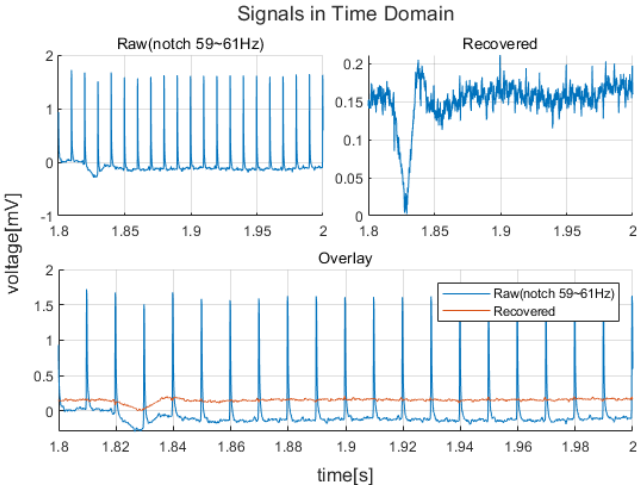


Fig. 9. Time domain signal plot of the recorded neural signal. The top left and right show the raw signal and the artifact-removed signal each. The bottom shows an overlay plot of the top two signals.

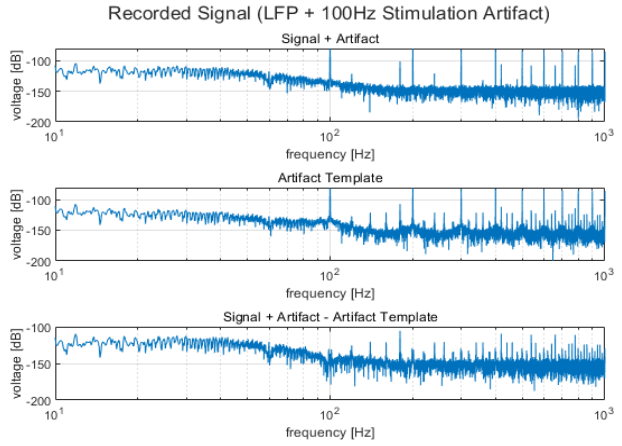


Fig 10. Frequency domain signal plot. From top to bottom, each shows the recorded neural signal, the generated artifact template, and the artifact-removed signal.

TABLE I. Performance Comparison

Performance	This work	[11]	[12]
Process	65nm CMOS	Sub-μ CMOS	65nm CMOS
Supply voltage (V)	1 / 2	5.25	1.2 / 2.5
Artifact suppression (dB)	45	100	60
Input referred noise (nV/√Hz)	237.2	144.6	126.9(3)
Artifact rejection delay	< 1s (1)	-(2)	< 2s

(1) At 100Hz stimulation frequency
(2) Conducted on external device
(3) Calculated from table in [12]

IV. CONCLUSION

In this work, circuit systems for bio-potential recording in daily life were designed, implemented, and tested: the 4-channel EEG-recording AFE with the low-noise buffer and the 2nd-order delta-sigma modulating Bio-ADC, and the digitally controlled neural stimulator with the stimulation artifact removal module by the artifact template method. Through the TSMC 65nm LP process, mm^2 scale IC chips are fabricated. Table I summarizes the key features compared with the performance of the prior arts. The result shows that the low-noise EEG recording AFE and ADC can read EEG-magnitude μV level signals well. The stimulation artifact removal method using artifact-template estimation by averaging method could effectively reduce artifacts from the recorded LPF. While electrical stimulations were given, the artifact profiles could be removed in the time and frequency domain.

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