A 2.5 GHz, 87-fs Step, Temperature-and-Voltage-Tolerant 6-bit Digital-to-Time Converter in 28nm CMOS

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Abstract **- This paper presents a temperature-and-voltage-tolerant 2.5GHz 6-bit digital-to-time converter (DTC) with an 87-fs resolution. The capacitor-DAC (CDAC) based DTC can achieve high resolution and linearity, but typical DTC structures suffer from performance degradation due to temperature and voltage variations. To address this issue, we implement a replica feedback loop consisting of a regulated constant-slope DTC, which effectively maintains the delay of the DTC even as temperature and voltage conditions fluctuate. Additionally, an on-chip histogram counter accurately measures on-chip delays. The proposed DTC in this paper is fabricated in a 28-nm CMOS process, with the core occupying an area of 0.0129 mm². It operates at 2.5 GHz with a 0.9 V supply voltage, consuming only 0.82 mW. Measured results demonstrate that the full-scale range changes for 125 °C temperature variation and for 200mV supply variation are reduced by 7.2x and 1.9x, respectively.**

Keywords**—Digital-to-time converter (DTC), capacitor-DAC (CDAC), replica feedback loop**

I. INTRODUCTION

A digital-to-time converter (DTC) is utilized in applications such as a fractional-N all-digital PLL, a clock-data recovery (CDR) in the serial-link receiver, and a time-interleaved ADC (TIADC). DTCs can be implemented in many different ways, but when fine resolution below gate delay is required, a signal-superposition-based phase interpolator DTC [1-3] or a switched-capacitor based DTC [4-7] is commonly used. In particular, the switched capacitor-based DTC utilizing constant-slope discharging in [6] demonstrated excellent linearity with fine resolution by adjusting the initial voltage on a local capacitor using a linear capacitor-DAC (CDAC) and charge sharing. A drawback, however, is that the full-scale range of this DTC is susceptible to supply and temperature because the discharge current and the threshold comparator in [7] are subject to supply and temperature variations.

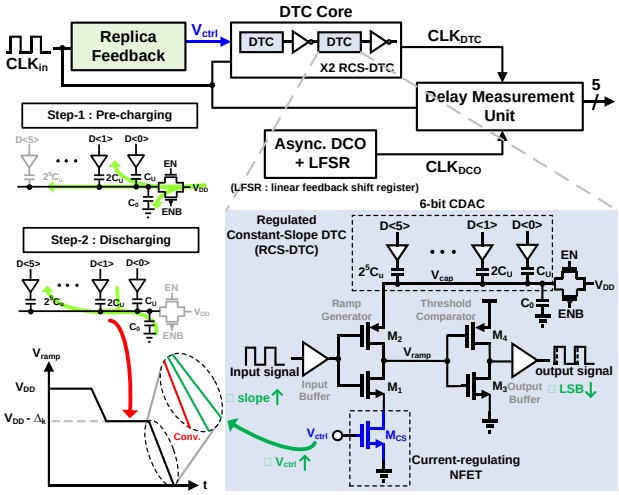

Fig. 1. Block diagram of core and architecture of the proposed DTC.

In applications such as the timing-skew calibration in TIADCs or the CDR in wireline receivers, it is critical to keep the DTC's delay constant over temperature or supply variation. To address this challenge, this work proposes an improved DTC in which a replica feedback loop regulates the full-scale range of the DTC, thereby maintaining the delay of the DTC over temperature and voltage variation. Measured performance validates that the full-scale range changes for 125°C temperature variation and for 200mV supply variation reduce by 7.2x and 1.9x, respectively, when compared to the case without using the proposed technique.

The rest of this paper is organized as follows: In Section II, the implementation of the proposed DTC, replica feedback loop, and delay measurement circuit is discussed. In Section III, measurement results are presented, and Section IV concludes the paper.

II. DESIGN METHODOLOGY

A. Proposed DTC

The architecture of the proposed DTC is shown in Fig. 1. The input clock (CLKIN) drives both the DTC core and the

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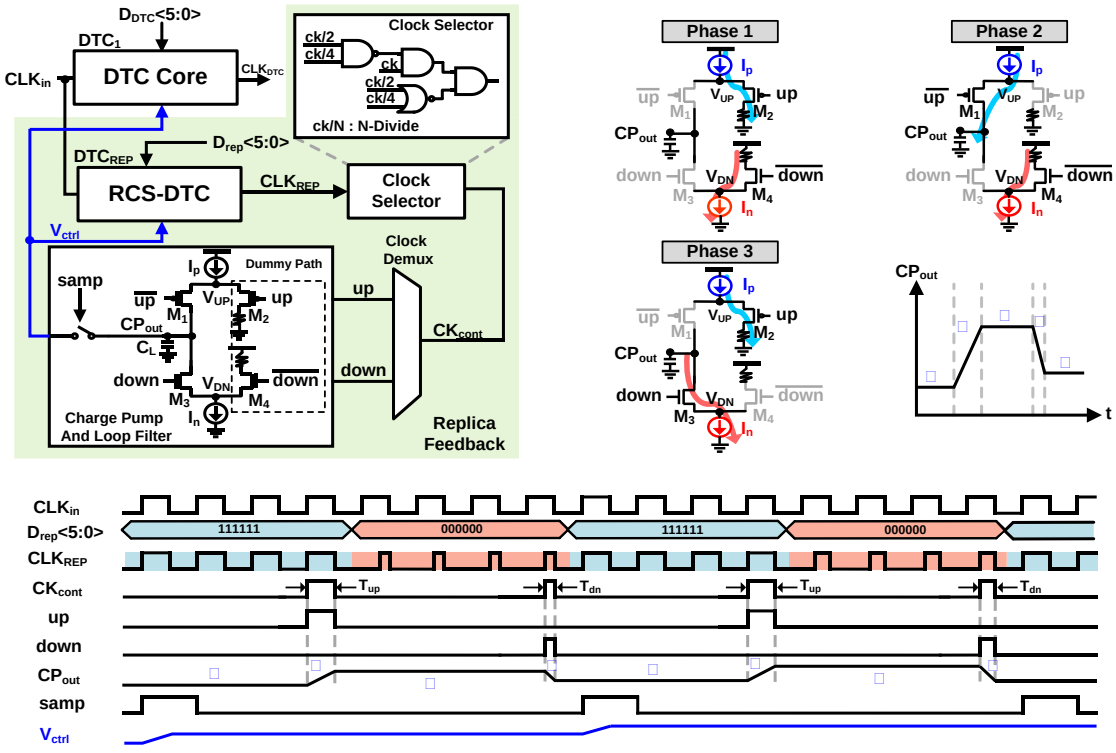


Fig. 2. The details of the replica feedback block and the corresponding timing diagram.

replica feedback block. The delay between the DTC output (CLK_{DTC}) and the input clock (CLK_{IN}) is measured by the histogram-based delay measurement unit. The DTC core is a two cascaded regulated-constant-slope DTCs (RCS-DTCs). The RCS-DTC consists of an input and output buffer, a 6-bit CDAC, a ramp generator, and a threshold comparator.

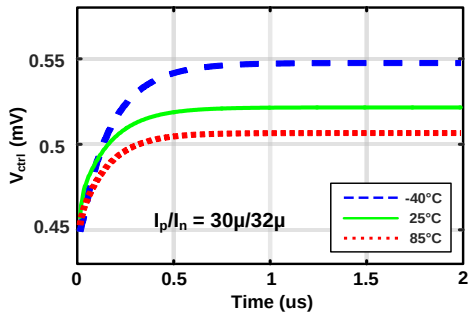
A key difference, when compared to the previous constant-slope DTC in [7], is that the current-regulating transistor M_{CS} is added in the discharge path of the ramp generator, where the gate voltage V_{ctrl} of M_{CS} is driven by the replica feedback block. The programmable delay is realized in two steps: pre-charging the V_{CAP} node and discharging the V_{RAMP} node.

As illustrated in Fig. 1, during the pre-charging, the transmission gate is on (EN=1) and the capacitors in CDAC with D<k>=1 are reset with zero voltage while those with D<k>=0 are pre-charged to V_{DD}. During the discharging, the transmission gate is turned off and all CDAC inputs are zeroed. The total charge is shared including newly activated capacitors, creating a voltage drop Δ_k at V_{CAP} node which is transferred to V_{RAMP} when the input clock is low. When the input clock signal is high, V_{RAMP} is discharged from V_{DD} - Δ_k where the discharging current is determined by V_{ctrl}. Therefore, the delay depends both on the CDAC input and V_{ctrl}. One limitation of this approach is that the delay programmability is applied only to the rising edge of the output clock. In applications, where the pulse width should be invariant to the digital input of the DTC (e.g., sampling clock generation of high-speed TIADCs), this can be a serious issue. To resolve this issue, our DTC core simply uses two cascaded RCS-DTCs, each contributing the same amount of delay for the edges to maintain a 50% duty cycle at CLK_{DTC}.

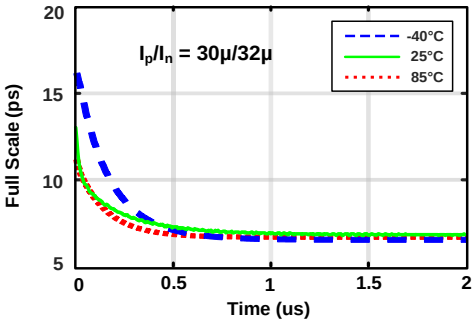
B. Replica feedback loop structure

Fig. 2 reveals the details of the replica feedback block along with the timing diagram. It consists of a replica RCS-DTC (DTC_{REP}), which is nominally identical to the RCS-DTC in the actual DTC (DTC_1), a clock selector, a clock demultiplexer, a charge pump, and a sampled loop filter that generates V_{ctrl} to close the feedback loop. The central idea here is to create a self-referenced feedback loop such that the time difference between minimum and maximum delay, which is the full-scale of the DTC_{REP}, is constant over voltage or temperature variation, and the resulting V_{ctrl} is forwarded to the DTC_1, being used with arbitrary input D_{DTC}<5:0>. To accomplish this goal, the DTC_{REP} input D_{REP}<5:0> toggles between decimal 0 and 63 at every four CLK_{in} cycles, and the output CLK_{CONT} is sent to the clock demultiplexer where the CLK_{CONT} is routed to the "up" pulse when D_{REP}=63 and to "down" pulse when D_{REP}=0.

The charge pump operates in three phases: In phase 1, M_2 and M_4 are turned on with both "up" and "down" being low. As current flows through dummy paths, CP_{out} remains unchanged. In phase 2, M_1 is turned on with "up" being high. As a result, the current I_p charges the loop-filter capacitor C_L and CP_{out} rises. In phase 3, M_3 is turned on with "down" being high, and the I_n discharges C_L so that CP_{out} drops. The role of the dummy path in phases 2 and 3 is to keep the I_n and I_p alive even when not being used. With the dummy path, V_{DN} and V_{UP} stay nearly unchanged, which reduces unwanted charge sharing that could cause errors in V_{ctrl} when transitioning from phase 1 to 3 and from phase 1 to 2.



(a)



(b)

Fig. 3. Simulation results of (a) V_{ctrl} and (b) the full-scale of the DTC for three different temperatures.

The actual output V_{ctrl} is sampled at the beginning of phase 1 when V_{ctrl} is fully settled after charge-discharge process is completed. When the loop is locked and V_{ctrl} reaches the final value, ΔV_{ctrl} =0 should hold, i.e., $I_n \cdot T_{dn} = I_p \cdot T_{up}$. Therefore, by using ratioed currents for I_n and I_p, the full-scale of the DTC can be kept constant even when the temperature or supply voltage changes. The simulated waveforms at the top of Fig. 3 show the V_{ctrl} and the full scale of the DTC for three different temperatures when I_p/I_n=30μA/32μA is used. It is evident that the full-scale delays converge to the same value with respective V_{ctrl} values.

In practice, process-induced mismatches create discrepancies between the DTC_{REP} and DTC_1, which can degrade the ability to maintain a constant full-scale. To address this issue, the sizes of M_1 and M_{CS} in Fig.1 were designed to be sufficiently large, minimizing the impact of mismatches. Additionally, future designs could implement a calibration block by connecting a transistor array in parallel with the M_{CS} of DTC_1, enabling fine-tuning to further reduce mismatch effects.

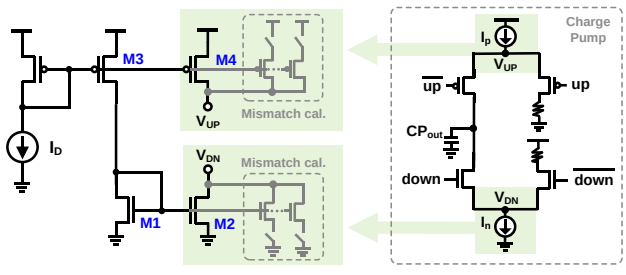


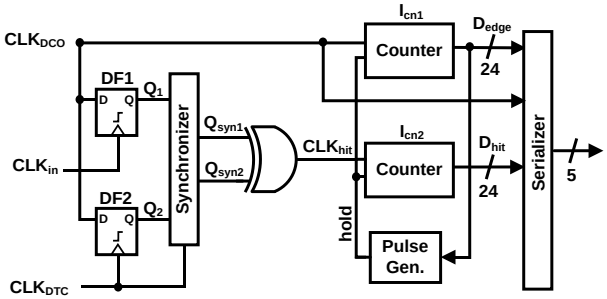
Fig. 4. Architecture of the charge pump current source.

Similarly, the full-scale of the DTC depends on the ratio of I_p to I_n, making the I_p/I_n ratio critical. Fig. 4 illustrates the architecture of the charge pump current source. In this design, the I_p/I_n ratio is defined by the transistor size ratios, specifically the ratios of M1:M2 and M3:M4. Because the transistor sizes determine the I_p/I_n ratio, it remains stable against temperature variations, thereby ensuring the full-scale stability of the DTC.

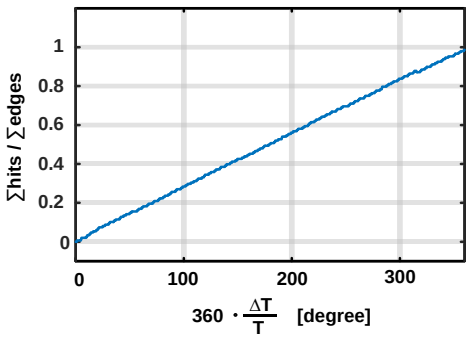
However, achieving the desired I_p/I_n ratio can be challenging due to mismatches between M1 and M2 or M3 and M4. Although not implemented in this study, Fig. 4 demonstrates how a calibration block could be incorporated to address these mismatches. By performing a one-time foreground calibration, the desired DTC full-scale can be achieved.

C. On-chip delay measurement

Fig. 5 displays the delay measurement unit used in this work, which is inspired by the code density test (CDT) technique in [8]. An on-chip digitally-controlled oscillator (DCO) generates an asynchronous clock (CLK_{DCO}), and the delay is calculated by counting the total number of CLK_{DCO}



(a)



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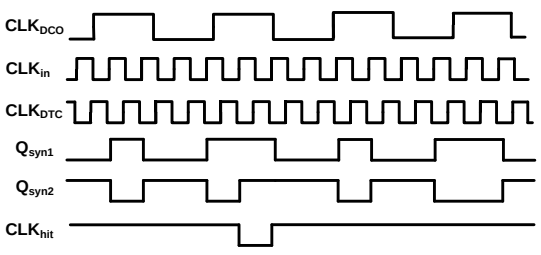

(c)

Fig. 5. (a) Architecture, (b) simulation result of the delay measurement unit, and (c) the corresponding timing diagram.

TABLE I. Performance summary and comparison table

	JSSC' 16 [1]	ASSCC' 17 [7]	CICC' 18 [9]	VLSI'21 [10]	This Work
Method	Edge interpolator	Constant slope (CDAC)	Two step Counter	Constant slope	Regulated Constant slope
Process (nm)	28	28	65	28	28
Supply (V)	1.1	1	1.05	0.9	0.8-0.1
Resolution (fs)	244	103	330	1020	87
Number of bits	11	5	7+10	9	6
DNL (fs)	305	36	1000	550	279
INL (fs)	1200	75	1650	700	294
Range (ps)	500	3.2	5310	530	5.6
Range Sensitivity	Self-aligned	PVT Sensitive	Self-aligned	Voltage Insensitive	VT Insensitive
Power (mw)	19.8 @2GHz	0.015 @40MHz	10 @100MHz	0.036 @50MHz	0.41** @2.5GHz
FoM* (fJ)	23.8	8.5	31.07	0.95	8.17

FoM*=Power ∗ INL / (Freq ∗ Range). **Only one RCS-DTC is considered

edges hitting the time between the edges of CLK_{in} and CLK_{DTC}. To measure this, CLK_{DCO} edges are first sampled by two flip-flops (DF1, DF2) clocked at CLK_{in} and CLK_{DTC}, respectively, and then a clock synchronizer composed of three flip-flops resamples the outputs Q_1 and Q_2 to reduce potential metastability error. Since glitches in the XOR gate output can introduce errors in D_{hit}, a resampling process is required to ensure stable operation. The synchronized clocks are compared through the XOR gate whose output toggles the 24-bit edge counter I_{cn2}. By comparing the D_{edge} and D_{hit}, normalized delay can be computed. The simulated output shown in Fig. 5 confirms that such a measurement can accurately estimate the delay between CLK_{in} and CLK_{DTC}. When compared to the measurement circuit in [8], our delay measurement does not use the return-to-zero block because it needs to measure the delay between only rising edges, not both edges.

III. MEASUREMENT RESULTS

The design is fabricated in a 28-nm CMOS process with an active area of 0.0129 mm^2, as illustrated in Fig. 6. As shown in Fig. 7, the replica feedback, which includes a replica RCS-DTC, consumes 1.64 mW when operating at 2.5 Gs/s. In practical applications such as TIADCs, the power consumption from the replica loop is amortized because it can be shared across many DTCs. The main DTC consumes only 0.82 mW. The resolution and full scale of the DTC, measured by the on-chip CDT, are 87-fs and 5.6 ps, respectively. The peak DNL and INL are 279 fs and 294 fs, respectively. The linearity degradation is attributed to the nonlinearity of the on-chip binary CDAC, which can be easily improved by using segmented CDAC.

Fig. 8 shows the measured full-scale variation versus supply and temperature change. The graphs show that the Δ*Fullscale/Fullscale* is reduced from 24.47% to 12.63% for a 200 mV supply change and from 45.21% to 6.32% for a 125°C temperature change, respectively. Table I summarizes the comparison with state-of-the-arts, showing this work is the only >GHz DTC achieving sub-100 fs resolution with PVT tolerance and superior power efficiency.

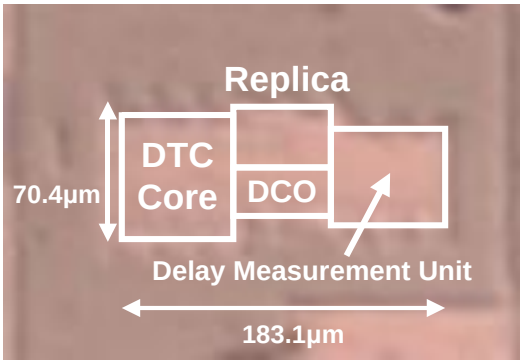

Fig. 6. Chip microphotograph.

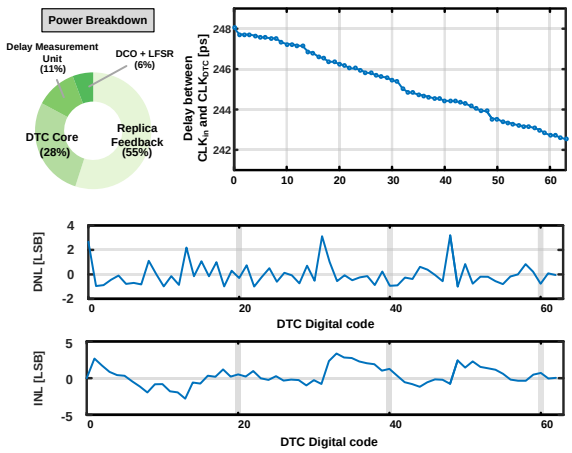

Fig. 7. Power breakdown and measured DTC linearity.

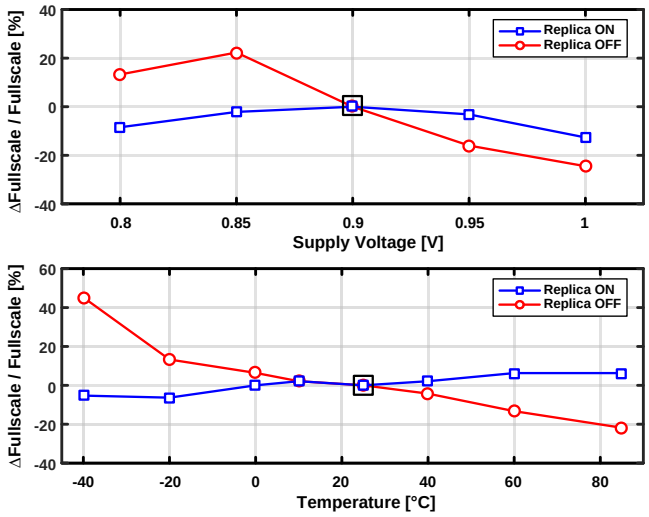

Fig. 8. Measured full scale variation versus supply and temperature change.

IV. CONCLUSION

This paper presents a 2.5 GHz 6-bit DTC achieving 87-fs resolution with tolerance to temperature and voltage variations. The proposed DTC architecture, consisting of a regulated constant-slope DTC and a replica feedback loop, effectively maintains the full-scale range. The replica feedback system ensures stable operation by regulating the discharge current through control voltage, significantly reducing full scale variations from 24.47% to 12.63% for a 200 mV supply variation and from 45.21% to 6.32% for a 125°C temperature change. These results demonstrate the efficiency of the proposed DTC, suggesting it could be utilized in applications that require stable delay performance over VT variations.

ACKNOWLEDGMENT

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