# Design of NRZ/PAM-3/PAM-4 Tri-Mode Single-Ended Transmitter for Next-Generation Memory Interfaces

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***Abstract*—This paper presents a single-ended voltage-mode transmitter for next-generation memory interfaces, supporting three signaling modes: non-return-to-zero (NRZ), three-level pulse amplitude modulation (PAM-3), and four-level pulse amplitude modulation (PAM-4). Utilizing the same output driver, the tri-mode transmitter effectively reduces the development cycle and associated costs for intellectual property (IP) development. Firstly, based on the mode selection signal, two mode selectors determine which data are passed to the tri-mode driver, outputting the data in either NRZ, PAM-3, or PAM-4 signaling. Secondly, 2-tap feed-forward equalizers (FFE) are separately applied to the three modes, compensating for signal distortions caused by losses in signal transmission through the channel based on different FFE encodings. A seven-step four-point ZQ calibration with offset cancellation is implemented to improve the level separation mismatch ratio. Designed using 65-nm CMOS technology, the transmitter achieved data rates of 16-Gb/s in NRZ mode, 24-Gb/s in PAM-3 mode, and 32-Gb/s in PAM-4 mode.**

***Keywords*—Feed-forward equalizer (FFE), level separation mismatch ratio (RLM), transmitter, tri-mode ZQ calibration**

## I. Introduction

With various technological advancements, the demand for high-bandwidth memory interfaces has been rapidly increasing in applications such as cloud servers, WiFi, automobiles, smartphones, and others. One way to increase the transfer bandwidth of memory interfaces is to increase the number of parallel I/O pins [1], which is adopted in high-bandwidth memory (HBM). Although this method can expand bandwidth, it also leads to increased hardware costs. Another method to increase bandwidth is to increase the data transmission speed per pin. However, as the transmission speed increases, the impact of channel attenuation also intensifies, limiting bandwidth improvement. To address this issue, alternative approaches adopting multi-level signaling, such as pulse amplitude modulation (PAM), have been recently introduced [2], [3].

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Four-level PAM(PAM-4) signaling can increase data transmission speed because it transmits 2 bits in one unit interval (UI) symbol; GDDR6X memory [4] recently achieved a transmission speed of 22 Gb/s/pin using PAM-4 signaling. However, the eye height of PAM-4 signals is only one-third of the non-return-to-zero (NRZ) signals; this leads to a deterioration in bit error rate (BER). To cope with this issue, three-level PAM (PAM-3) signaling has been adopted for next-generation memory interfaces. PAM-3 signals can transmit about 1.58 ($\log_2 3$) bits during a 1-UI symbol, thereby offering 1.58 times the bandwidth improvement compared to NRZ signals, with the eye height at half of the NRZ signals; thus, PAM-3 signaling achieves a lower BER than PAM-4 signaling. Recent GDDR7 memory [5] has achieved a transmission speed of 37 Gb/s/pin and a 20% improvement in energy efficiency over GDDR6 using PAM-3 signaling.

To support various memory standards, various studies have been reported on multi-mode memory interfaces, such as NRZ/PAM-4 [6], [7] and NRZ/PAM-3 [8] dual-mode configurations. However, while NRZ, PAM-3, and PAM-4 are all utilized in memory interfaces, a memory interface that supports all three modes has not yet been developed.

This paper presents a tri-mode transmitter (TX) that supports NRZ, PAM-3, and PAM-4 signaling modes. Compared to previous dual-mode transmitters, this tri-mode approach significantly reduces development time and costs, increases development efficiency, and offers the flexibility to meet the requirements of diverse memory interfaces.

The rest of this paper is structured as follows: Section II explores the design of the existing dual-mode transmitter. Section III provides a detailed description of the proposed tri-mode transmitter. Section IV shows the simulation results, and Section V concludes the paper.

## II. Previous Dual-Mode Transmitter

As aforementioned, there have been various dual-mode designs for memory interfaces, such as NRZ/PAM-4 [6], [7] and NRZ/PAM-3 [8] TXs. An NRZ/PAM-4 dual-mode TX implemented in [6] uses 60 basic source-series terminated (SST) driver units, as shown in Fig.1(a). In [7], an N-over-N driver comprising three pull-up (PU) drivers and two pull-down (PD) drivers, as shown in Fig.1(b), is used to implement NRZ/PAM-4 dual-mode. Each PU and PD driver is structured with 5-bit binary segmentation to control impedance independently. In [8], the driver outputs

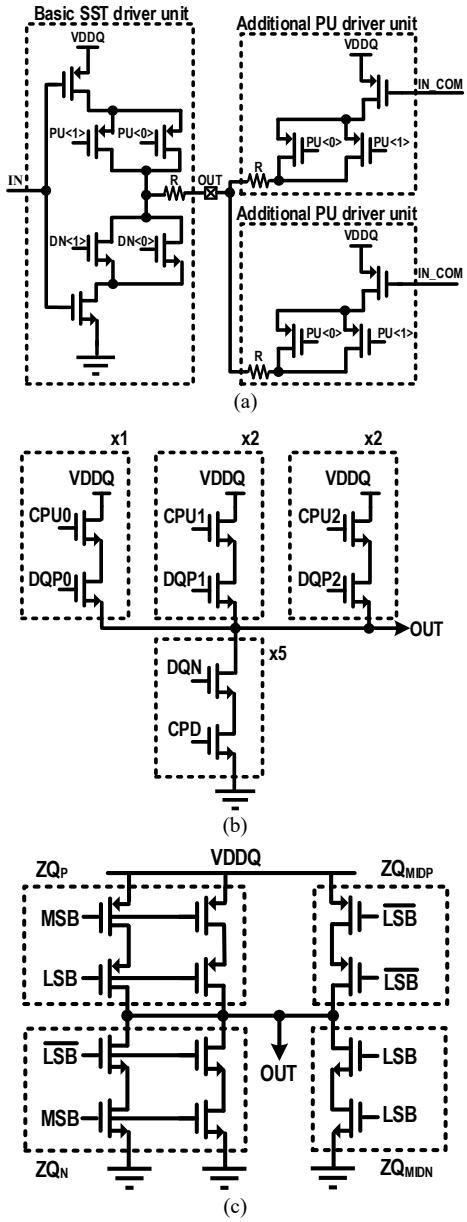



Fig. 1. Previous (a) NRZ/PAM-4 [6], (b) NRZ/PAM-4 [7] and (c) NRZ/PAM-3 [8] dual-mode drivers.

an NRZ/PAM-3 signal by using a combination of the most significant bit (MSB) and least significant bit (LSB) signals, as shown in Fig. 1(c).

In multi-level signaling, such as PAM-3 and PAM-4, a level separation mismatch ratio (RLM) performance is important to achieve a good BER. To improve RLM, additional PU driver units are used in [6], achieving 98% RLM. A five-step, three-point ZQ calibration is employed to improve the RLM to 99% in [7]. The two-point PAM-3 ZQ calibration used in [8] enhances the RLM to 98.5%.

## III. Proposed Tri-Mode Transmitter

Fig. 2 presents the complete block diagram of the proposed tri-mode NRZ/PAM-3/PAM-4 transmitter. The 64-bit pseudo-random binary sequence (PRBS) generator produces parallel PRBS data as input data for the NRZ and PAM-4 modes. The three parallel input data for PAM-3 mode are generated by three 16-bit PRBS generators. The data from these PRBS generators are sent to the serializers. The serialized data are transmitted to the encoder for encoding. After encoding, the first data selection determines whether the data entering the 2:1 serializer are NRZ, PAM-3, or PAM-4 data. Following the 2:1 SER, a second data selection is performed to determine the data that enter the tri-mode driver and a 2-tap feed-forward equalizer (FFE) driver. The PU and PD drivers of the tri-mode driver and the 2-tap FFE driver consist of serially connected NMOS transistors and passive resistors. A four-point ZQ calibration helps the tri-mode driver achieve the correct output impedance and improve the RLM of PAM-3 and PAM-4 signals.

### *A. Tri-Mode Driver*

As illustrated in Fig. 3, we introduce a tri-mode driver that incorporates six PU drivers and six PD drivers to achieve high linearity and impedance matching. Each PU driver and PD driver consists of an NMOS transistor in series with a passive resistor, which is more tolerant of impedance variation caused by changes in output level [9] and makes output impedance matching with the channel easier. The value of the passive resistor (R) is set to 150 Ω. Using ZQ calibration, the total on-resistance ($R_{ON}$) of the NMOS transistor and the passive resistor in each PU and PD driver is adjusted to 300 Ω.

Figs. 4(a) and (b) respectively illustrate how the tri-mode driver generates four signal levels (+3, +2, +1, and +0) for PAM-4 and three signal levels (High, Middle, and Low) for PAM-3, respectively. These signal levels are determined by the activated PU and PD drivers, as well as the receiver (RX) termination. The output levels of the tri-mode driver can be expressed as follows:

$$V_{OUT} = \frac{R_{PD}//R_{RX}}{R_{PU}+R_{PD}//R_{RX}} \cdot V_{DDQ} \quad (1)$$

where $V_{DDQ}$ is the supply voltage of the driver, $R_{PD}$ and $R_{PU}$ represent the total impedances of the activated PD and PU drivers respectively, and $R_{RX}$ is the resistance of RX termination.

For PAM-4 signaling, at the '+0 level', the total impedance of the pull-down section is 50 Ω. At the '+1 level', the pull-up section has an impedance of 150 Ω, while the pull-down section has 75 Ω. At the '+2 level', the pull-up section is 75 Ω, and the pull-down section is 150 Ω. At the '+3 level', the pull-up section is 50Ω. For PAM-3 signaling, the High level is the same as the '+3 level' in PAM-4, the Low level corresponds to the '+0 level' in PAM-4, and the Middle level has equal impedances of 100 Ω for both PU and PD sections. For NRZ signaling, the High and Low levels are generated similarly to the '+3 level' and '+0 level' in PAM-4, respectively. Due to the variation in impedance with changes in the drain-source voltage ($V_{DS}$), the impedance of NMOS transistors differs at each output level. ZQ calibration is used to correct the impedance errors caused by $V_{DS}$ variations, thereby achieving high RLM.

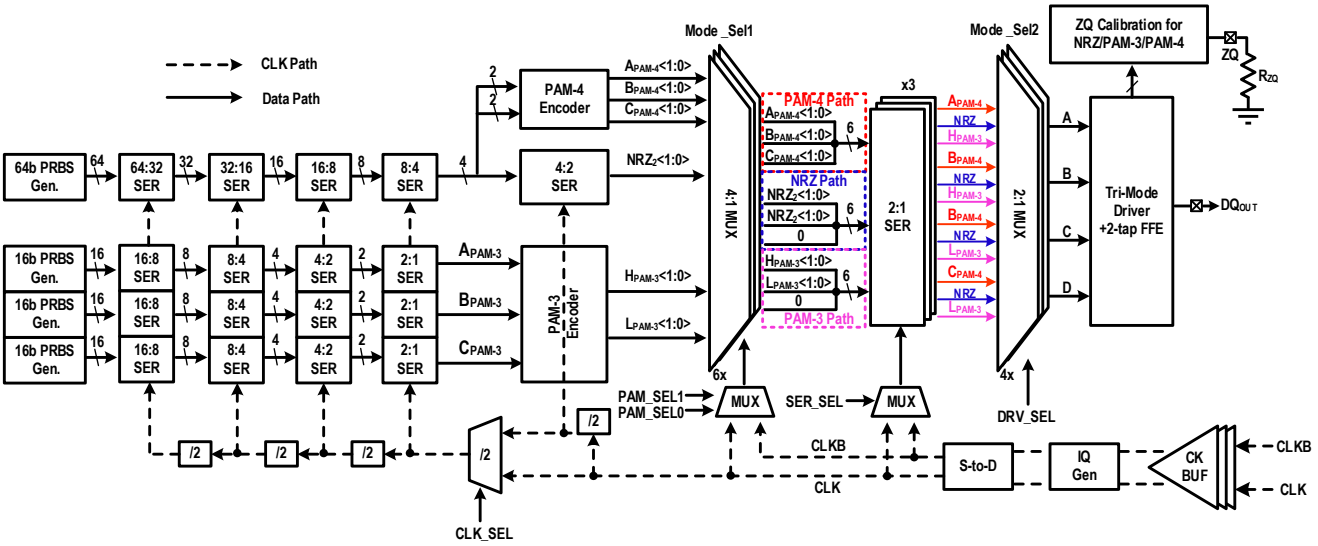



Fig. 2. Tri-mode NRZ/PAM-3/PAM-4 transmitter architecture.

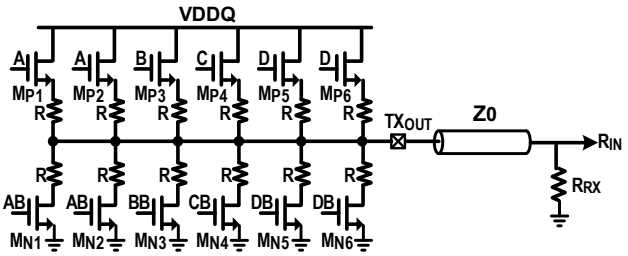


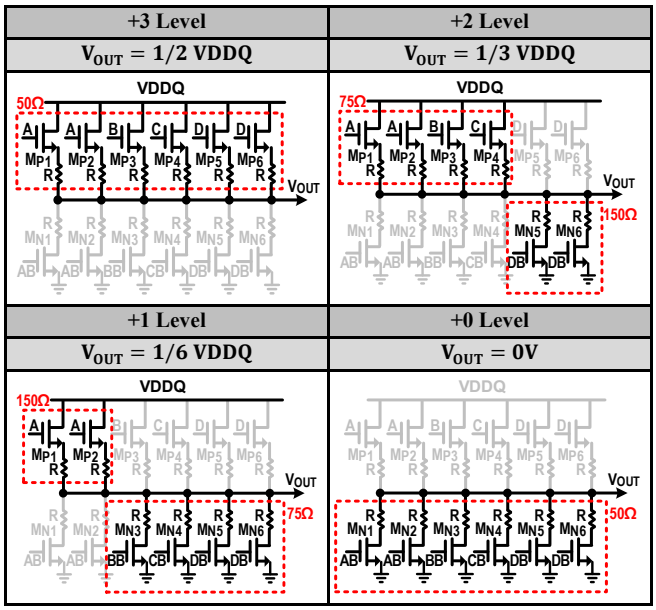

Fig. 3. Schematic of the proposed tri-mode driver.

Fig. 5 shows the detailed circuit implementation of the tri-mode driver. The PU and PD drivers are each controlled by 4-bit binary ZQ codes, which are generated by the ZQ calibration process. These codes activate and deactivate NMOS transistors to achieve impedance matching at each output level.

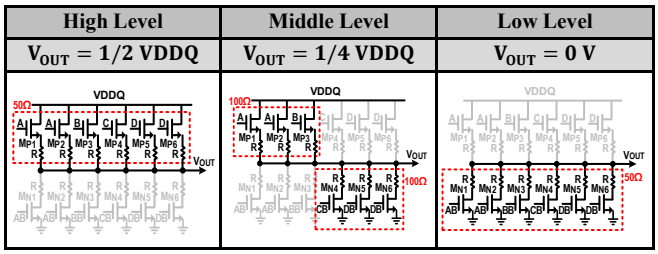
### *B. PAM-4 and PAM-3 Encoder, Two Mode Selectors, and 2:1 Serializer*

Fig. 6 illustrates the PAM-4 encoder, which generates three output data: $A_{PAM-4}$, $B_{PAM-4}$ and $C_{PAM-4}$, by encoding the MSB and LSB. The input data for the encoder is provided by the frontend serializers. TABLE I shows the encoding table for the PAM-3 signal. In PAM-3 signals, each UI can convey 1.5 bits, meaning a two-UI symbol can transmit 3 bits of data. The three-bit full-rate data $A_{PAM-3}$, $B_{PAM-3}$, and $C_{PAM-3}$ generated by the serializer are encoded into four output data: $H_O$, $L_O$ (odd data), and $H_E$, $L_E$ (even data). These four output data determine the High, Low, or Middle levels, resulting in eight transition cases.

The encoded data enters the two-mode selectors. The first mode selector consists of six 4:1 multiplexers (MUXs), determining which data enters the 2:1 serializer. The second mode selector comprises four 2:1 MUXs, selecting the data that is fed into the tri-mode driver. Additionally, after the first data selector, true single-phase clock D flip-flops are used to sample the output signals, ensuring the timing margin for the 2:1 serializer and




(a)




(b)

Fig. 4. (a) PAM-4 and (b) PAM-3 operations of proposed tri-mode driver.

reducing data-dependent jitter (DDJ). A clock phase selector is also used to correct the clock phase for sampling the output when the device mismatch and process, voltage, and temperature (PVT) variations occur.

### *C. 2-Tap FFE*

In high-speed links, channel loss and inter-symbol interference (ISI) distort the transmitted data, deteriorating BER. To correctly recover the data, the tri-mode driver employs a 2-tap feed-forward equalizer (FFE) structure, as

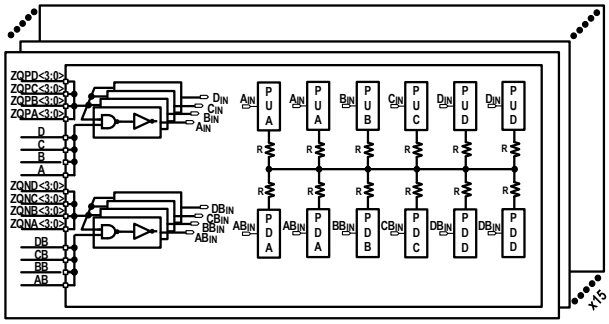



Fig. 5. Detailed implementation of the tri-mode driver.

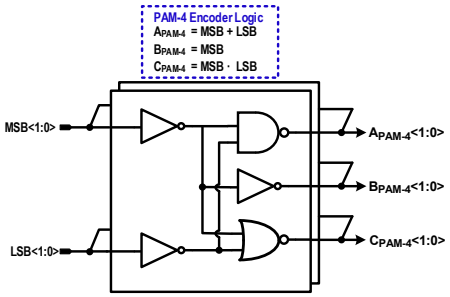



Fig. 6. Structure of the PAM-4 encoder.

shown in Fig. 7. The FFE driver consists of four PU drivers and four PD drivers, each PU and PD driver comprising an NMOS transistor in series with a passive resistor. The value of the passive resistor is set to 150Ω. 2-tap FFE can be expressed as [7]:

$$Y[N] = (1-\alpha)X[N] - \alpha X[N-1] \quad (2)$$

where $X[N]$ is current data, $X[N-1]$ represents previous input data, and $\alpha$ is the tap coefficient.

The PU and PD drivers are controlled by 3-bit binary FFE codes, respectively. In NRZ and PAM-3 modes, the PU FFE codes (AFFEP<2:0>, BFFEP<2:0>, CFFEP<2:0>, DFFEP<2:0>) and PD FFE codes (AFFEN<2:0>, BFFEN<2:0>, CFFEN<2:0>, DFFEN<2:0>) are used to control the number of activated PU and PD drivers, thereby providing different equalization strength coefficients. For example, in NRZ mode, when transitioning from 0 to 1, all the PU FFE codes are activated and adjusted to control the PU equalization strength. In PAM-4 mode, the FFE codes CFFEP<2:0> and CFFEN<2:0> are disabled, leaving the three PU FFE codes (AFFEP<2:0>, BFFEP<2:0>, DFFEP<2:0>) and three PD FFE codes (AFFEN<2:0>, BFFEN<2:0>, DFFEN<2:0>) to adjust the equalization coefficients for the upward and downward transitions of the PAM-4 mode. For example, when the signal transitions from the "+1 level" to the "+2 level", the PU FFE codes BFFEP<2:0> and DFFEP<2:0> and the PD FFE code AFFEN<2:0> are enabled and adjusted to control the equalization strength. When FFE mode is enabled, the FFE code needs to be manually adjusted according to the channel loss to control the number of FFE drivers that are enabled until the optimal coefficients are found.

### *D. Four-Point ZQ Calibration*

TABLE I. PAM-3 Encoding Table and Output Waveform.

| Input Data | | | Encoded Data (Odd) | | Encoded Data (Even) | | Output (Odd+Even) |
|---|---|---|---|---|---|---|---|
| $A_{PAM-3}$ | $B_{PAM-3}$ | $C_{PAM-3}$ | $H_O$ | $L_O$ | $H_E$ | $L_E$ | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | |

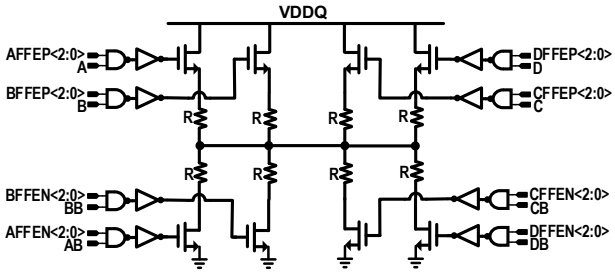



Fig. 7. Block diagram of tri-mode FFE driver.

To improve signal integrity and enhance RLM performance in PAM-3 and PAM-4 modes, a four-point calibration is performed. In memory interfaces, ZQ calibration is performed in the foreground after the chip powers on. In addition, recalibration is performed between normal operations to cope with VT variations. Fig. 8 illustrates this process. The calibration circuit includes six replica PU drivers, six replica PD drivers, and comparators to determine the correct output levels.

The ZQ calibration process for the tri-mode TX involves seven steps to ensure accurate impedance settings. In step 1, a replica PUA driver is connected to an external 300-Ω resistor via the ZQ pin, and the ZQPA code is adjusted until $V_{OUT}$ equals VDDQ/2, setting the PU segment $R_{ON}$ at 300 Ω. In step 2, the PDD driver is connected to the calibrated PUA driver, and the ZQPD code is adjusted to achieve $V_{OUT}$ of VDDQ/2, setting the PD segment $R_{ON}$ at 300 Ω. In step 3, both PU and PD segments are connected to the external 300-Ω resistor, and the ZQPB code is swept until $V_{OUT}$ reaches VDDQ/4, setting the pull-up segment $R_{ON}$ at 100 Ω. In step 4, the PUA, PUB, PDC, and PDD drivers are activated, and the ZQNC code is adjusted to set the PD segment $R_{ON}$ to 100 Ω when $V_{OUT}$ equals VDDQ/4. Steps 5 to 7 follow a similar calibration process at VDDQ/6,

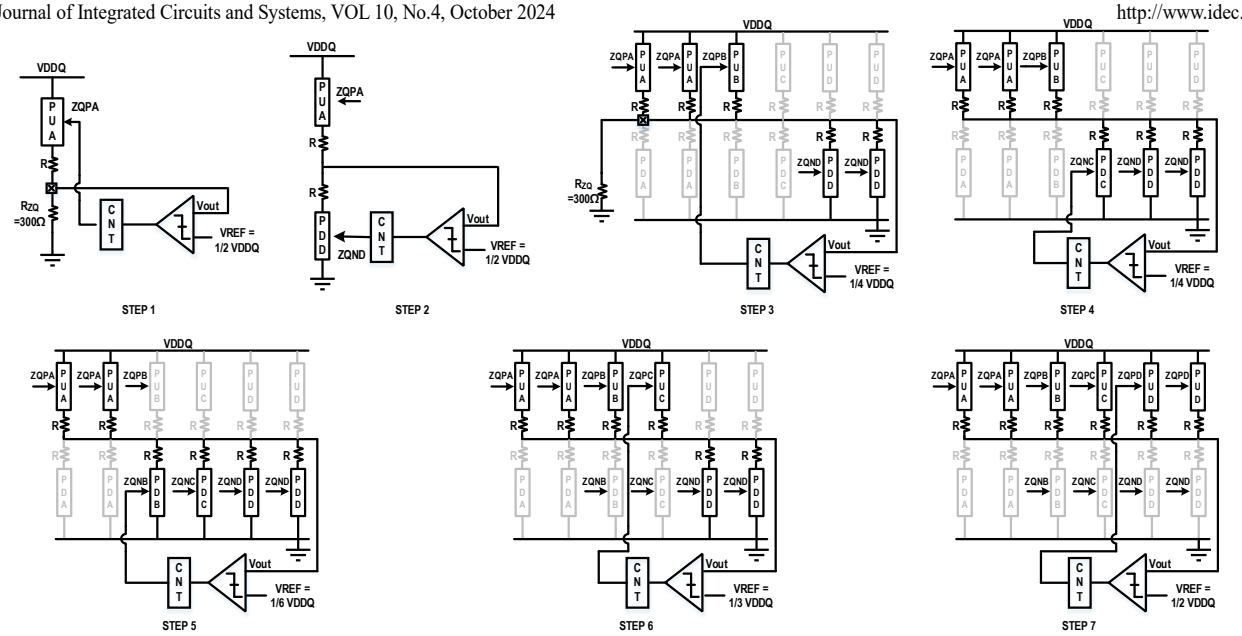



Fig. 8. Four-point ZQ calibration to enhance RLM.

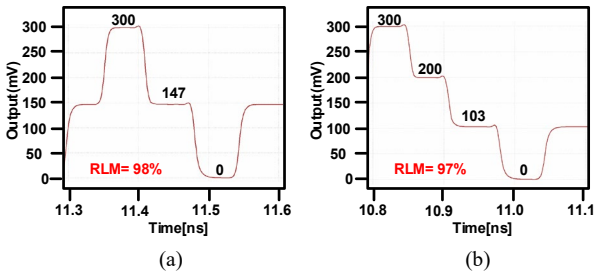



Fig. 9. Simulated RLM in (a) PAM-3 and (b) PAM-4 signaling.

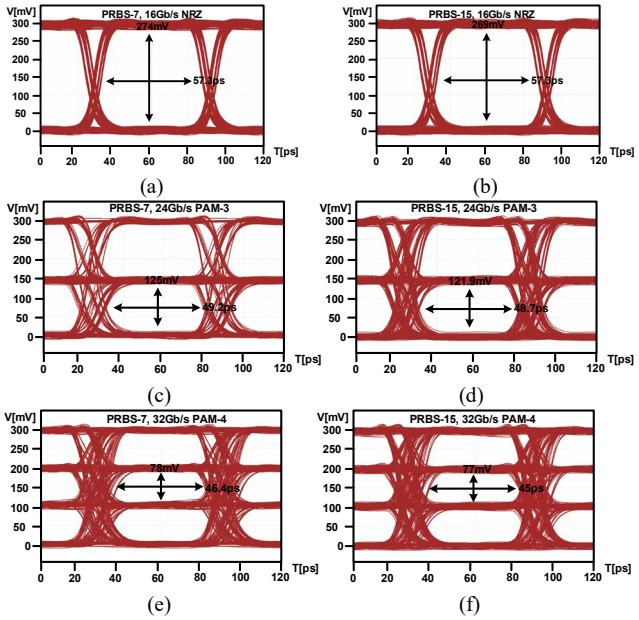



Fig. 10. Simulated 16-Gb/s NRZ eye diagrams without a channel using (a) PRBS-7 and (b) PRBS-15 patterns, 24-Gb/s PAM-3 eye diagrams without a channel using (c) PRBS-7 and (d) PRBS-15 patterns, and 32-Gb/s PAM-4 eye diagrams without a channel using (e) PRBS-7 and (f) PRBS-15 patterns.

VDDQ/3, and VDDQ/2 to find the codes for ZQNB, ZQPC, and ZQPD, respectively. Each step compensates for impedance variations caused by changes in $V_{DS}$.

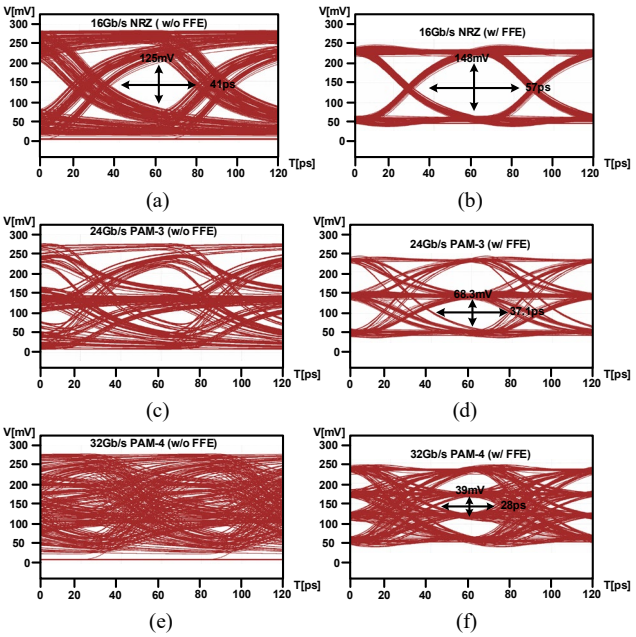



Fig. 11. Simulated PRBS-7 eye diagrams with the channel at 16-Gb/s NRZ (a) without and (b) with FFE, 24-Gb/s PAM-3 (c) without and (d) with FFE, and 32-Gb/s PAM-4 (e) without and (f) with FFE.

## IV. Simulation Results

The proposed tri-mode NRZ/PAM-3/PAM-4 transmitter is designed using a 65-nm CMOS process. The VDD supply voltage is 1 V, and the VDDQ supply voltage is 0.6 V. The channel employed for the test experiences a loss of 6.21dB at 8GHz. Four-point ZQ calibration results in an RLM of 98% for PAM-3 signals and 97% for PAM-4 signals, as shown in Fig. 9. Fig. 10 illustrates the eye diagrams simulated with PRBS-7 and PRBS-15 patterns without a channel. At 16 Gb/s in NRZ mode, the eye height is 274 mV with the PRBS-7 pattern and decreases to 269 mV with the PRBS-15 pattern, as illustrated in Figs. 10(a) and (b). In 24-Gb/s PAM-3 mode, the eye diagram shows

TABLE II. Power Breakdown of 16 Gb/s NRZ, 24 Gb/s PAM-3, and 32 Gb/s PAM-4.

| NRZ | | PAM-3 | | PAM-4 | |
|---|---|---|---|---|---|
| **Block** | **Power [mW]** | **Block** | **Power [mW]** | **Block** | **Power [mW]** |
| PRBS Gen. | 1.95 | PRBS Gen. | 2.19 | PRBS Gen. | 2.06 |
| 64:4 SER | 3.91 | 16:1 SER | 5.45 | 64:4 SER | 5.14 |
| 4:2 SER | 4.20 | Encoder | 5.30 | Encoder | 5.25 |
| Mode Sel.+ 2:1 SER | 3.96 | Mode Sel.+ 2:1 SER | 5.47 | Mode Sel.+ 2:1 SER | 5.59 |
| Output Driver | 12.98 | Output Driver | 9.75 | Output Driver | 15.24 |
| Clock Path | 13.50 | Clock Path | 13.50 | Clock Path | 13.50 |
| **Total** | **40.50** | **Total** | **41.66** | **Total** | **46.78** |

TABLE III. Performance Summary and Comparison Table.

| **Reference** | **[6] ISCAS'19** | | **[10] ACCESS'22** | | **This Work** | | |
|---|---|---|---|---|---|---|---|
| **Technology** | 65nm | | 65nm | | 65nm | | |
| **Supply[V]** | 1.0 | | 1.0 | | 1.0 | | |
| **Modulation** | NRZ | PAM-4 | NRZ | PAM-4 | NRZ | PAM-3 | PAM-4 |
| **Driver Topology** | Voltage-mode | | Voltage-mode | | Voltage-mode | | |
| **Signaling** | Single-ended | | Single-ended | | Single-ended | | |
| **Data rate (Gb/s)** | 10 | 20 | 16 | 32 | 16 | 24 | 32 |
| **TX FFE** | 4-tap DEE | 2-tap DEE | 2-tap DEE | 2-tap DEE | 2-tap DEE | 2-tap DEE | 2-tap DEE |
| **ZQ calibration** | Additional PU driver | | - | | Four-point Cal. | | |
| **RLM (%)** | - | 98 | - | 96 | - | 98 | 97 |
| **Power[mW]** | 72 | 61.5 | 27 | 47 | 40.5 | 41.66 | 46.78 |
| **Energy efficiency (pJ/bit)** | 7.2 | 3.08 | 1.69 | 1.47 | 2.53 | 1.73 | 1.46 |

125 mV in height and 49.2 ps in width with the PRBS-7 pattern, and 121.9 mV in height and 48.7 ps in width with the PRBS-15 pattern, as shown in Figs. 10(c) and (d). For 32 Gb/s PAM-4 mode, the eye width is 46.4 ps and height is 78 mV with the PRBS-7 pattern, and 45-ps width and 77-mV height with the PRBS-15 pattern, as depicted in Figs. 10(e) and (f).

Fig. 11 presents the eye diagrams simulated with a PRBS-7 pattern through the channel. The FFE tap coefficient $\alpha$ is 0.15 in NRZ mode, 0.22 in PAM-3 mode, and 0.19 in PAM-4 mode. Without FFE, the NRZ mode presents an eye-opening measuring 41 ps in width and 125 mV in height, as shown in Fig. 11(a). In PAM-3 mode, the worst-case eye is almost closed, as shown in Fig. 11(c), whereas in PAM-4 mode, it is fully closed, as shown in Fig. 11(e). With FFE, the NRZ-mode eye improves to 57-ps width and 148-mV height, as shown in Fig. 11(b). The PAM-3 eye improves to 37.1-ps width and 68.3-mV height with FFE, as illustrated in Fig. 11(d). In PAM-4 mode with FFE, the eye width improves to 28 ps and the height to 39 mV, as shown in Fig. 11(f).

The tri-mode transmitter consumes 40.50 mW at 16 Gb/s in NRZ operation, 41.66 mW at 24 Gb/s in PAM-3 operation, and 46.78 mW at 32 Gb/s in PAM-4 operation. TABLE II presents the power breakdown of the designed transmitter for each mode. TABLE III provides a performance comparison between our tri-mode transmitter and other dual-mode transmitters.

## V. Conclusion

To support various memory interface standards and facilitate rapid interchangeability during technological transitions, we propose a tri-mode transmitter that supports NRZ, PAM-3, and PAM-4 signaling. The tri-mode transmitter, fabricated using a 65-nm CMOS process, supports data rates of 16/24/32 Gb/s in NRZ, PAM-3, and PAM-4 modes. The 2-tap FFE can achieve different equalization strengths for different modes. High linearity and impedance matching are achieved through a four-point ZQ calibration that compensates for impedance variations due to changes in $V_{DS}$. Our transmitter achieves a data rate of 24 Gb/s/pin with a 98% RLM in PAM-3 mode and 32 Gb/s/pin with a 97% RLM in PAM-4 mode. It also achieves energy efficiencies of 2.53 pJ/bit at 16 Gb/s in NRZ mode, 1.73 pJ/bit at 24 Gb/s in PAM-3 mode, and 1.46 pJ/bit at 32 Gb/s in PAM-4 mode.

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## References

[1] S. -M. Lee *et al*., "A single-ended parallel transceiver with four-bit four-wire four-level balanced coding for the point-to-point DRAM interface," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1890–1901, Aug. 2016.

[2] H. Park, J. Song, J. Sim, Y. Choi, J. Choi, J, Yoo, and C. Kim, "30-Gb/s 1.11-pj/bit single-ended PAM-3 transceiver for high-speed memory links," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 581–590, Feb. 2021.

[3] S.-H. Kim, S.-H. Kim, X. Jin, Y. Lee, and J.-H. Chun, "A 21-Gb/s dual-channel voltage-mode transmitter with stacked NRZ and PAM4 drivers," *IEEE Access*, vol. 6, pp. 59761–59767, 2018.

[4] T. M. Hollis, R. Schneider, and M. Brox, "An 8Gb GDDR6X DRAM achieving 22Gb/s/pin with single-ended PAM4 signaling," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 348–349.

[5] S. -Y. Cho, M. -C. Choi, and J. Baek, "A 16Gb 37Gb/s GDDR7 DRAM with PAM3-optimized TRX equalization and ZQ calibration," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 242–243.

[6] C. Hyun, H. Ko, J. -H. Chae, H. Park, and S. Kim, "A 20Gb/s dual-mode PAM4/NRZ single-ended transmitter with RLM compensation," *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1–4.

[7] X. Wang, J. Jin, X. Liu, Z. Yang, S. Wang, and J. Zhou, “A 16/32-Gb/s/pin dual-mode single-ended transmitter with pre-emphasis FFE and RLM enhanced ZQ calibration for memory interfaces,” *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2023, pp. 1–4.

[8] C. Han, K. –S. Lee, and J. -H. Chae, “A 25.2Gb/s/pin NRZ/PAM-3 dual-mode transmitter with embedded partial DBI achieving a 133% I/O bandwidth/pin efficiency and 19.3% DBI efficiency,” *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 248–249.

[9] Y. -U. Jeong, H. Park, C. Hyun, J. -H. Chae, S. -H. Jeong, and S. Kim, “A 0.64-pJ/bit 28-Gb/s/pin high-linearity single-ended PAM-4 transmitter with an impedance-matched driver and three-point ZQ calibration for memory interface,” *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1278–1287, Apr. 2021.

[10] S. -H. Kim, B. Cho, J. Jin, Y. H. Song, and J.-H. Chun, “A 16/32 Gb/s dual-mode NRZ/PAM4 voltage-mode transmitter with 2-tap FFE,” *IEEE Access*, vol. 10, pp. 119140–119149, 2022.

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