A Low-Power, Highly Linear Sub-GHz Receiver Front-End with a Voltage Follower-Based 4th-Order Channel Selection Filter

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***Abstract* - A low-power, highly linear sub-GHz receiver front-end designed for LPWAN IoT applications is presented, featuring a voltage follower-based 4th-order channel selection filter. The receiver front-end comprises a wideband single-to-differential (S-to-D) low-noise amplifier (LNA), an in-phase/quadrature (I/Q) passive mixer, and the proposed advanced channel selection filter. The S-to-D LNA utilizes two cascaded inverters and a correction amplifier to achieve high gain, low noise, and high linearity while minimizing power consumption. The channel selection filter employs a novel design that combines the flipped voltage follower (FVF) and super source follower (SSF), enabling the implementation of a 4th-order filter without degrading the noise figure (NF). Implemented in 130-nm CMOS technology, the receiver achieves a conversion gain of approximately 30 dB, a double-sideband NF (NF_{DSB}) of 3 dB at a cut-off frequency, and an output-referred third-order intercept point (OIP3) between +6.2 dBm and +7.7 dBm in the sub-GHz band, with a total power consumption of 8.9 mW from a 1.2 V supply.**

***Keywords* - CMOS, channel selection filter, flipped voltage follower, inverter**

I. INTRODUCTION

The Internet of Things (IoT) mobile communication is moving toward high frequency bands for higher data rate, and on the other hand, it is also moving toward low frequency bands, which generally refer to the frequency band below 1 GHz, in order to ensure long transmission distance, wide scope, and good signal penetrability. This is for interconnecting a variety of devices, people, and data for a wide range of applications such as manufacturing, agriculture, commercialization, smart homes and buildings, autonomous vehicles, healthcare, and almost everywhere. In contrast to the short-range wireless communication systems such as 2.4 GHz IEEE 802.15.4 (ZigBee) and Bluetooth Low-Energy drawing little power and transferring data at a high data rate, many low-power wide-area network (LPWAN) technologies including long-range wide-area networks (LoRaWAN), narrowband-IoT (NB-IoT), and long-term evolution for machines (LTE-M) can extend the communication coverage and improve battery life [1]. These technologies occupy sub-GHz multi-ISM-bands (typically 433 or 868 MHz), and the narrowband operation of a sub-GHz radio enables transmission between 1 and 50 kilometers. Because sensitivity is inversely proportional to channel bandwidth, a narrower bandwidth leads to higher receiver sensitivity and improved efficiency at lower transmission rates.

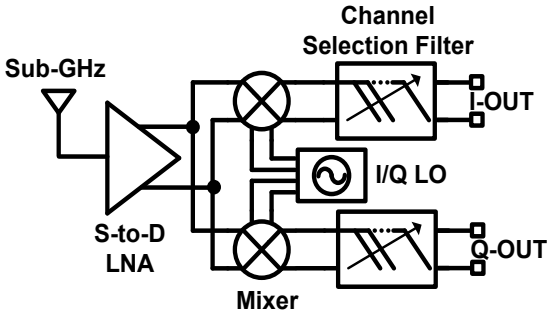

Fig. 1. Schematic of the proposed receiver front-end composed of wideband single-to-differential (S-to-D) low noise amplifier (LNA), in-phase/quadrature (I/Q) passive mixer and channel selection filter.

The sub-GHz receiver front-end should provide a higher out-of-band (OOB) rejection characteristic because of very crowded strong interference signals in the sub-GHz frequency band such as digital TV, 4G/5G cellular, 802.11ah, and other sub-GHz protocols. Especially, the requirements for the adjacent and alternative channel rejection of the sub-GHz receiver have become much more stringent. Because the adjacent and alternative channel rejection ratio are dominated by the channel selection filter, it is necessary to design of a highly linear low-noise, higher-order channel selection filter with low power consumption.

In this paper, a low-power, highly linear sub-GHz receiver front end employing a voltage follower-based 4th-order channel selection filter is proposed for LPWAN IoT applications. Especially, this work focuses on the design a highly linear low noise channel selection filter with low power consumption for high-frequency applications.

II. REVIEW OF TRADITIONAL CHANNEL SELECTION FILTERS

Fig. 1. shows the schematic of the proposed receiver front-end composed of a wideband single-to-differential (S-to-D) low noise amplifier (LNA), an in-phase/quadrature (I/Q) passive mixer and a channel selection filter. The continuous-time channel select filters can be implemented using active-RC, transconductance-C (G_m-C), and MOSFET-C topologies as shown in Fig. 2, with each solution presenting significant drawbacks. The active-RC topology is a promising candidate for channel selection filter owing to the excellent linearity by the negative feedback operation. It is well known that the harmonic distortion can be suppressed by an amount of the

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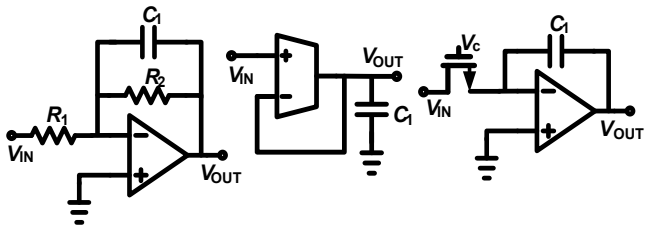


Fig. 2. Traditional continuous-time channel selection filters: (a) active-RC filter, (b) transconductance (G_m)-C filter, (c) MOSFET-C filter.

loop gain. However, it suffers from high power consumption because the unity gain bandwidth of the operation amplifier in active-RC filter should be much higher than the cut-off frequency of the filter in order to ensure a sufficiently high open loop-gain within the operating frequency of the filter. Concerning for G_m-C filter topology, it can operate at high frequency band with low power consumption and relatively low noise performance, but its linearity is quite poor due to the transconductance nonlinearity. Many studies have tried to improve the linearity of G_m-C filter using MOSFET derivative superposition methods [2]-[4], but its improvement is very sensitive to process, voltage, and temperature variations. The MOSFET-C filter is implemented using triode region MOSFETs as voltage-controlled resistors in the integrators, but unfortunately this severely degrades the linearity. Furthermore, as the supply voltage decreases together with channel length scaling, the threshold voltage does not reduce at the same rate, resulting in a lower frequency coverage for this filter. As a result, it is highly required to implement a low power high-frequency channel selection filter to overcome the issues of the traditional filter topologies.

III. Design of Proposed Low Noise Amplifier (LNA) and Mixer

Fig. 3 presents a schematic of the proposed S-to-D LNA. The CMOS inverter with DC feedback has been widely used in the design of high-frequency amplifiers for its high gain, low noise, high linearity, and simple hardware configuration. The effective transconductance can be easily increased through the current reuse technique. As a result, the proposed LNA is built on the basis of the cascaded two inverters. A large resistor is connected between the gate and drain nodes to stabilize the DC operating point. The drain node voltage of the inverter is biased at half the supply voltage in order to provide the largest output voltage swing and high linearity. The value of the DC feedback resistor between the gate and drain nodes of inverter is 50 kΩ. This large resistance is implemented using a high-sheet-resistance polysilicon resistor provided by the commercial process design kit (PDK). On the other hand, the simulated input common-mode range of the inverter ranges from 570 mV to 620 mV.

The cascaded inverters provide the single-to-differential conversion to exclude the use of the bulky off-chip transformer in sub-GHz band. However, the amplitude imbalance is inevitable in the cascaded inverters. To compensate these amplitude and phase imbalances, two single-ended outputs of two cascaded inverters are applied to the imbalance correction amplifier, which is a combined topology of the differential common-source amplifier and a source follower.

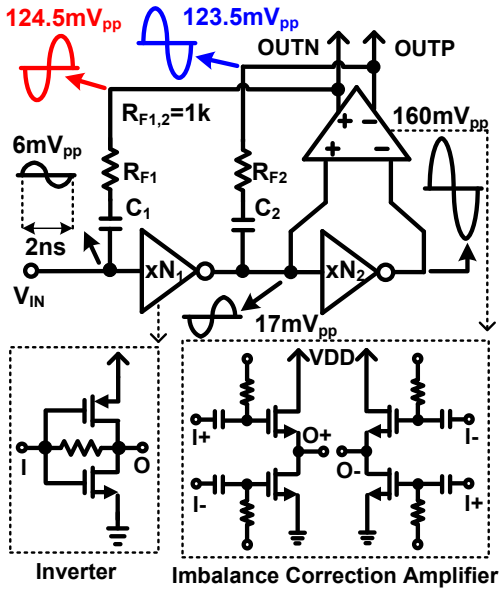


Fig. 3. The proposed wideband inverter-based single-to-differential (S-to-D) LNA. The voltage swing waveform at each node is shown when a 500 MHz RF signal with a power of -40 dBm is applied to the LNA.

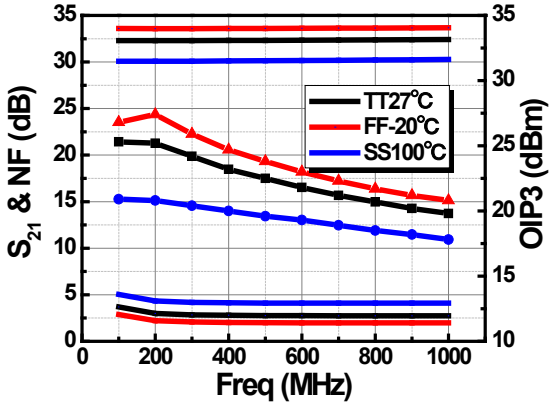


Fig. 4. The simulated power gain (S_{21}), NF and output-referred third-order intercept-point (OIP3) of the proposed LNA against process corner and temperature variations. The symbol 'T', 'F', and 'S' stand for the typical, fast, and slow model, respectively.

On the other hand, the resistive or source follower feedback is very effective technique for wideband input impedance matching. To implement a wideband active feedback S-to-D LNA, two feedback resistors (R_F) are connected between the input of the first (second) inverter and the non-inverting output OUTP (inverting output OUTN) of the correction amplifier, respectively. This configuration ensures the identical loading conditions for the differential output (OUTN and OUTP) of the correction amplifier, thereby minimizing the imbalances with low power consumption. As shown in the voltage swing levels at each node in the proposed LNA, most of the voltage gain is achieved through the second inverter stage. In the open-loop state (without R_{F1} and R_{F2}), the voltage gains of the first and second inverter stages is approximately 16.7 dB (xN_1) and 21.7 dB (xN_2) respectively. The transconductance (g_m) value of the common source (CS) and source follower (SF) transistors in the imbalance correction amplifier are the same, implying the voltage gain through the CS and SF stages is almost identical for a specific value of the feedback resistor.

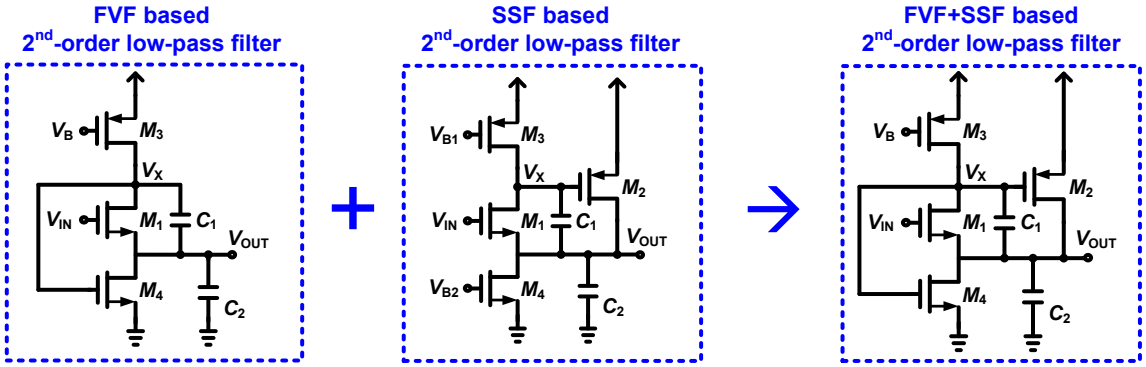


Fig. 5. The 2nd-order low-pass filter combining a flipped voltage follower (FVF) based version and a super source follower (SSF) based version [12].

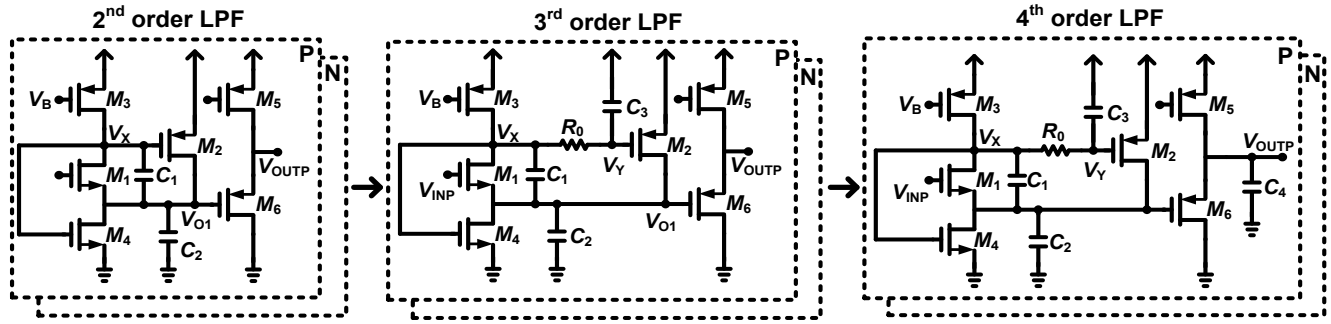


Fig. 6. Proposed 4th-order channel selection filter.

On the other hand, the loop gain and voltage gain of the proposed LNA are expressed as:

$$T_{LOOP} \approx (N_1 + N_1 N_2) \text{ and} \quad (1)$$

$$A_V \approx \frac{2R_F}{R_S}\frac{T_{Loop}}{1+T_{Loop}} \approx \frac{2R_F}{R_S}. \quad (2)$$

When negative feedback is applied to the open loop amplifier, the harmonic distortions are reduced by a factor of the loop gain, and the relationship between input-referred third-order intercept point (IIP3) of the open-loop and closed-loop amplifiers is given by:

$$IIP3_{Closed-Loop} \approx IIP3_{Open-Loop} \times (1+T^*_{LOOP})^{3/2} \quad (3)$$

where $IIP3_{Closed\text{-}Loop}$ and $IIP3_{Open\text{-}Loop}$ denote IIP3 of the closed- and open-loop amplifier, respectively [5]. T^*_{LOOP} is the loop gain when the input of the LNA is terminated with the source impedance R_S. In comparison with the conventional resistive or source follower feedback LNAs in [6]-[9], the proposed LNA shows the lower noise figure (NF) and higher linearity due to the enhanced loop gain. Fig. 4. presents the simulated power gain (S_{21}), NF, output-referred third-order intercept-point (OIP3) of the proposed LNA across process corner and temperature variations. The symbol 'T', 'F', and 'S' stand for the typical, fast, and slow model, respectively. The S_{21} and NF range from 30 dB to 33.5 dB and from 2 dB to 4.1 dB, respectively. The OIP3 ranges from +19.7 dBm to 23.8 dBm in the 500 MHz frequency band. For the mixer, the current communicating passive mixer is employed for high linearity.

IV. Design of Proposed Channel Selection Filter

The source follower-based filters show better performance than op amp-based filters in the aspects of gain bandwidth, linearity and power dissipation. As is well known, the flipped voltage follower (FVF) [10] and the super source follower (SSF) [11] are improved versions of the conventional source follower, which have better linearity and unity-gain bandwidth under the same power dissipation. The proposed channel selection filter is designed on the basis of the more advanced source follower reported in [12], which combines FVF and SSF as shown in Fig. 5. Two feedback paths (M_2 and M_4) increase the loop gain, and, as a result, enhance the effective transconductance (g_{m1}) of the input transistor M_1. This improves the noise performance of the filter. In other words, the dual loop configuration using both M_2 and M_4 can have larger loop gain than the single loop configuration using only M_4 because the overall loop gain by the dual loop is given by the product of each loop gain. In addition, the current consumed by M_2 can be re-used by M_4. Since the FVF+SSF structure has a larger number of nodes to connect than FVF, it is easier to design a higher-order filter.

The schematic of the complete FVF+SSF based 2nd-order low-pass filter is shown in Fig. 6. The source follower stage composed of transistors M_5 and M_6 is added to shift the DC level of the output voltage and match the DC level with the next building block. In addition, it is useful to implement a higher-order filter by simply connecting the capacitor to its output. The transfer function of the proposed filter is calculated as:

$$H(s) \approx \frac{1}{s^2 \dfrac{C_1 C_2}{g_{m1}(g_{m2}+g_{m4})} + s\dfrac{C_1}{g_{m1}} + 1}, \quad (4)$$

where g_{mi} is the transconductance of the transistor M_i. From Eq. (4), the cut-off frequency (ω_0) and quality factor (Q-factor) of the filter is given as:

$$\omega_0 \approx \sqrt{\frac{g_{m1}(g_{m2}+g_{m4})}{C_1C_2}} \text{ and } Q \approx \sqrt{\frac{C_2 g_{m1}}{C_1(g_{m2}+g_{m4})}}. \quad (5)$$

On the other hand, the output-referred noise voltage ($V_{n,o}$) of the 2nd-order low-pass filter is calculated as:

$$\overline{V_{n,o}^2} = \sum_{i=1}^{6} \left| H_{n,Mi}^2 \right| \cdot \overline{i_{n,Mi}^2}, \quad (6)$$

where $H_{n,Mi}$ is the transfer function of the output voltage from the current noise $i_{n,Mi}$ of each transistor M_i. The $H_{n,Mi}$ of each transistor M_i is given as:

$$H_{n,M1} \approx \frac{g_{m2}+g_{m4}}{s^2C_1C_2 + sC_1(g_{m2}+g_{m4}) + g_{m1}(g_{m2}+g_{m4})}, \quad (7)$$

$$H_{n,M2,4} \approx \frac{sC_1}{s^2C_1C_2 + sC_1(g_{m2}+g_{m4}) + g_{m1}(g_{m2}+g_{m4})}, \quad (8)$$

$$H_{n,M3} \approx \frac{sC_1 - (g_{m2}+g_{m4})}{s^2C_1C_2 + sC_1(g_{m2}+g_{m4}) + g_{m1}(g_{m2}+g_{m4})}, \quad (9)$$

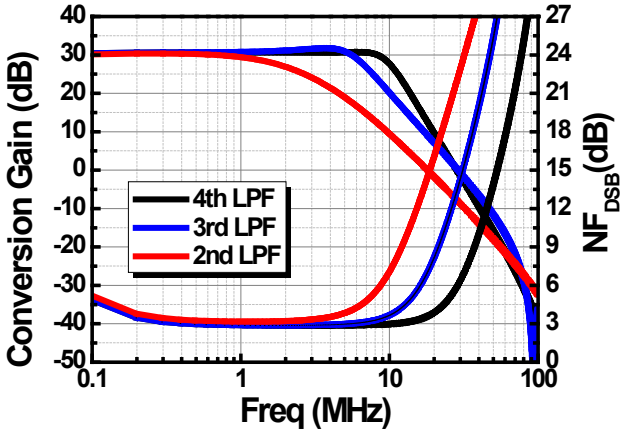
$$H_{n,M5} \approx \frac{1}{g_{m5}}, \text{ and } H_{n,M6} \approx \frac{1}{g_{m6}}. \quad (10)$$

Because the channel bandwidth is quite wide and the channel length of all transistors is set to be 0.6-μm in order to minimize the effect of the flicker noise, the thermal noise is only considered for the noise calculation. As a result, the square of $i_{n,Mi}$ is approximately given by $4kT\gamma g_{mi}$, where k is the Boltzmann constant, T is the absolute temperature, and γ is the bias-dependent channel thermal noise coefficient of the MOSFET device. In conclusion, the output-referred noise voltage of Eq. (6) at a low frequency band around DC can be simplified as:

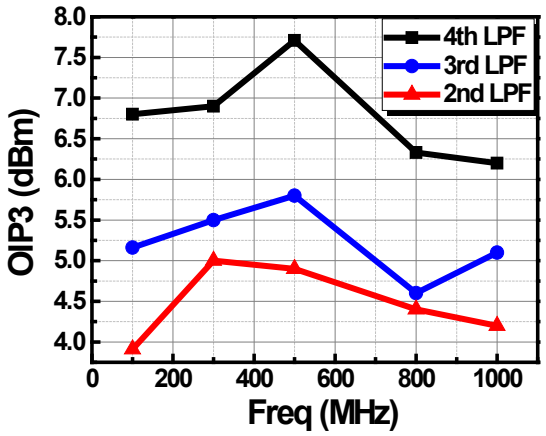
$$\overline{V_{n,o}^2} \approx \frac{4kT\gamma}{g_{m1}} + \frac{4kT\gamma g_{m3}}{g_{m1}^2} + \frac{4kT\gamma g_{m5}}{g_{m6}^2} + \frac{4kT\gamma}{g_{m6}}. \quad (11)$$

One interesting thing is that the thermal noise contributions from transistors M_2 and M_4 are almost zero at the output as the operating frequency is close to DC because of the band-pass characteristic of $H_{n,M2}$ and $H_{n,M4}$. In order to reduce $V_{n,o}$ and achieve a NF of the filter, it is desirable to increase g_{m1} and g_{m6} and decrease g_{m3} and g_{m5}.

As shown in Fig. 6, the proposed 3rd and 4th-order low-pass filters are designed on the basis of the 2nd-order low-pass filter without the use of extra transistors and power consumption. In case of the 3rd-order low-pass filter, it is easily built by adding R_0 and C_3 to the core of the 2nd-order low-pass filter. On the other hand, the 4th-order low-pass filter is easily designed by adding C_4 to the core of the 3rd-order low-pass filter. An interesting point is that the output-referred noise voltage of the 3rd- and 4th-order low-pass filters at a low frequency band around DC is the same as that of the 2nd-order low pass filter. This is because the thermal noise contributions from transistors M_2 and M_4 and resistor R_0 at a low frequency band around DC become almost zero at the output because of the band-pass characteristic. In the simulation, the degradation of NF is about 3 dB at a cut-off frequency of 6 MHz when the R_0 and C_3 are moved to the V_{o1} node to implement 3rd-order filter. In addition, the effect of C_4 can be ignored at a low frequency band around DC. In conclusion, the NF of the proposed 2nd, 3rd, and 4th-order low-pass filters in the passband is almost the same. This implies that the proposed 4th-order channel selection filter can achieve lower NF and higher linearity with lower power consumption than the conventional active-RC or G_m-C filters with the same filter order.



(a)



(b)

Fig. 7. Simulation results of the proposed receiver employing the 2nd-, 3rd-, and 4th-order low pass filter: (a) conversion gain and double-sideband noise figure (NF_{DSB}), (b) OIP3.

V. Simulation Results

Fig. 7. presents the simulated conversion gain, double-sideband noise figure (NF_{DSB}), and OIP3 of the proposed receiver employing the 4th-order low pass filter. It is designed and simulated using a 130-nm CMOS technology. The power consumption of the proposed receiver, excluding the local oscillator (LO) generation circuit, is approximately 8.9 mW from a 1.2 V supply voltage. The cut-off frequency of the proposed 4th-order channel selection filter is set equal to about 10 MHz, and the receiver employing it achieves the simulated conversion gain of about 30 dB and NF_{DSB} of 3 dB at a cut-off frequency. The simulated OIP3 ranges from 6 dBm to 8 dBm in sub-GHz band. For comparison, the simulation results of the receiver adopting the 2nd- and 3rd-order low pass filter of Fig. 6 are plotted together in Fig. 7. Note that the

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUSLY REPORTED STUDIES

	[13]	[14]	[15]	*This work
Frequency Range (GHz)	0.05-0.7	0.2-1	0.3-0.8	0.1-1
Conversion Gain (dB)	26.5	44.4-50.5	28	30
NF_{DSB} (dB)	< 4.25	4.4-5.7	< 4.2	3
In-band OIP3 (dBm)	12 @300MHz	27.5	14 @400MHz	6.2-7.7
Filter order	4	*N*-path	2	4
Power(mW)	33.6 @1.2V	8.7 @1.2V	6 @1.2V	8.9 @1.2V
CMOS Technology(nm)	130	65	65	130

*: Simulation results

proposed receiver with 4th-order low pass filter shows an almost the same in-band noise and OIP3 performances in spite of higher order of filter.

TABLE I compares the performance of the proposed sub-GHz receiver to that reported in previous works. Compared to [13], it achieves higher conversion gain and lower NF with lower power consumption.

VI. CONCLUSION

The low-power low-noise sub-GHz receiver employing a voltage follower-based 4th-order channel selection filter is designed using 130-nm CMOS technology for LPWAN IoT applications. The proposed 4th-order channel selection filter achieved a cut-off frequency of about 10 MHz with lower NF than the traditional active-RC and G_m-C filter topologies, while consuming a lower power. The receiver showed a total double-sideband NF of around 3 dB eliminating an expensive off-chip balun in the sub-GHz band due to the proposed wideband feedback-based single-to-differential LNA.

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