Design of a Prototype 64−Channel ROIC for SWIR Imaging Sensor Applications

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***Abstract* –This paper presents the design and validation of a 64-channel prototype Readout Integrated Circuit (ROIC) for InGaAs-based compound semiconductor pixels, specifically aimed at Short-Wave Infrared (SWIR) imaging systems. The ROIC, fabricated using a 0.18μm CMOS process, Consists of a 64-channel array with a pitch of 50μm and a total chip area of 5 × 2.5 mm². Comprehensive silicon-level validation has been performed to ensure stability and performance reliability. The ROIC achieves a random noise level of 119.48 μV_{rms} and operates with a total power consumption of 22.55 mW, demonstrating its suitability for infrared imaging applications. The study highlights the innovative approach of incorporating variable conversion gain and sensitivity adjustment to accommodate different pixel signal characteristics, thereby enhancing the overall imaging performance.**

***Keywords*—Short-Wave Infrared (SWIR) imaging technology, Readout Integrated Circuit (ROIC), Conversion gain control, Sensitivity adjustment**

I. INTRODUCTION

Infrared imaging systems are designed to detect infrared wavelength bands and convert them into image information [1], [2]. These systems have the advantage of capturing features that are invisible in the visible light spectrum by sensing the longer wavelengths of infrared signals. Specifically, imaging systems utilizing Short-Wavelength Infrared (SWIR) wavelengths of 0.9 μm to 2.6 μm offer significant benefits for object recognition in that they acquire information about reflected light differently from Medium-Wavelength Infrared (MWIR) and Long-Wavelength Infrared (LWIR) detection systems generated from the heat of the object [3], [4]. SWIR imaging systems are widely employed in various industries such as military, aerospace, medical, and night surveillance due to their superior capabilities [4]. Consequently, the research and development of infrared imaging systems can drive advancements across multiple sectors.

SWIR imaging systems leverage the unique properties of SWIR wavelengths to penetrate atmospheric obscurants such as smoke, fog, and dust, providing clear images under challenging conditions [5], [6]. This capability is particularly valuable in military and aerospace applications where visibility can be compromised. In medical imaging, SWIR systems can offer enhanced tissue contrast and improved visualization of vascular structures, aiding in diagnosis and treatment. For industrial process monitoring, SWIR cameras can detect heat patterns and material properties that are not visible to conventional imaging systems [7].

A critical component in the development of SWIR imaging systems is the pixel and the readout integrated circuit (ROIC) [8]. Silicon-based pixels are less effective in detecting SWIR signals due to their limited wavelength range. Therefore, pixels are manufactured using compound semiconductors such as Indium Gallium Arsenide (InGaAs), which possess a broader wavelength range and can accurately detect SWIR signals. InGaAs-based sensors are preferred for their high quantum efficiency and low noise characteristics, making them suitable for high-performance imaging applications. The ROIC plays an important role in amplifying the charge generated by the pixels and converting it into electrical signals to acquire image information [9]. High-quality imaging necessitates that the ROIC ensures the integrity of the signals received from the pixels, maintaining proper signal levels and range. If the signal contains noise or is extremely weak, the design must minimize noise and accurately read the signal to obtain precise information. This aspect is crucial in ROIC design as reducing noise enhances the overall reliability of the system, yielding clearer and more accurate images [10].

Additionally, the integration of the ROIC with compound semiconductor-based pixels involves overcoming the physical limitations of the pixels through effective correction techniques within the ROIC [11]. For example, variations in pixel performance due to manufacturing inconsistencies or environmental factors can be mitigated by implementing adaptive gain control and noise reduction strategies in the ROIC. These techniques are essential for maintaining consistent image quality across the entire sensor array. Given this importance, there has been significant

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progress in the research and development of ROICs for SWIR imaging systems in recent years [12], [13], leading to considerable improvements in key performance metrics such as dynamic range, signal-to-noise ratio (SNR), and power consumption. Advanced ROIC designs now include features such as multi-mode operation, enabling them to switch between different imaging modes (e.g., high sensitivity vs. high dynamic range) based on the application requirements [14].

This paper introduces the design methodology for a 64-channel prototype ROIC specifically targeting InGaAs-based compound semiconductor pixels, each with a pitch of 50μm. The prototype ROIC is designed to operate at a supply voltage of 3.3V and is fabricated using a 0.18μm CMOS process. The design focuses on enhancing the performance and flexibility of SWIR imaging systems, making it a critical step forward in the continuous advancement of infrared imaging technologies. Key features of the prototype include adjustable gain and sensitivity settings, which allow for the optimization of image quality under varying operating conditions. The prototype also incorporates power-saving modes and advanced noise reduction techniques to improve the overall efficiency and effectiveness of SWIR imaging applications. By addressing the challenges associated with SWIR imaging, this research aims to contribute to the development of next-generation imaging systems that can meet the demanding needs of diverse applications. The advancements presented in this paper highlight the potential for significant improvements in imaging performance, paving the way for new innovations in the field of infrared technology.

The structure of the remainder of this paper is organized as follows: Section II details the overall architecture and design methodology of the ROIC with 64 channels. Section III presents the measurement results of the prototype chip. Finally, Section IV provides the conclusion.

II. CIRCUIT IMPLEMENTATION

Fig. 1 illustrates the signal chain of the targeted SWIR imaging system. The pixels in this system are made from InGaAs-based compound semiconductors, designed to detect wavelengths in the 0.9μm to 2.6μm range. When SWIR light is detected by the pixel, it converts the light into a proportional signal in the form of charge, which is then input in the ROIC. The pixels and the ROIC are integrated through wire bonding via their respective pads.

The primary purpose of the ROIC is to accurately read and transmit the signals generated by the pixels. Numerous prior studies have discussed various readout circuit architectures such as Source Follower per Detector (SFD) [15], Direct Injection (DI) [16], Buffered Direct Injection (BDI) [17], and Capacitive Transimpedance Amplifier (CTIA) [18]. Key performance criteria include power consumption, linearity, area, and noise, with the goal of maintaining low power consumption and high SNR within a limited area being paramount for readout circuit design [19]. Designers must develop devices and select appropriate readout circuit architectures that meet these challenges. Among the successful and widely applied architectures is the CTIA,

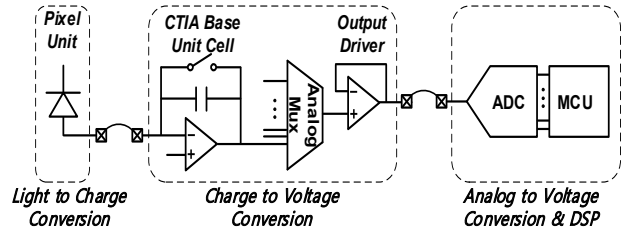


Fig. 1. Signal extraction chain for SWIR imaging system.

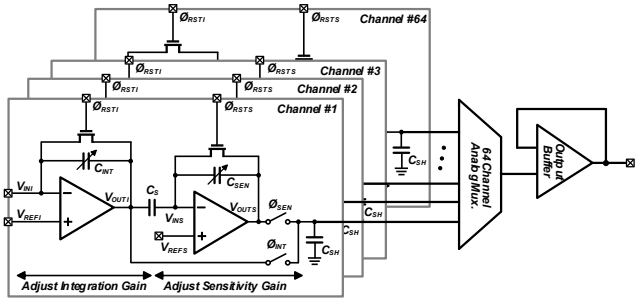


Fig. 2. Block diagram for ROIC channel array.

which operates as a current-to-voltage converter composed of an amplifier integrated with a feedback capacitor. The CTIA architecture ensures stability by controlling the positive input terminal of the amplifier and providing an adjustable bias voltage to ensure stable bias supply to the pixels. Furthermore, it has low input impedance, ensuring excellent injection efficiency, making it suitable for SWIR imaging systems. This design employs the conventional CTIA architecture, which provides stable bias voltage, low impedance, and low noise. The basic mechanism of the CTIA is to process the signal charge generated by the pixel through the feedback capacitor of the CTIA. For accurate reading, a reset switch discharges the integration capacitor and resets the output to a reference voltage. The virtual short characteristic of the negative feedback amplifier ensures excellent control of the detector's bias point. The integrated signal voltage output from the CTIA is sequentially selected by the analog multiplexer and sent to the output driver. The number of input terminals of the analog multiplexer matches the number of channels. In this design, the prototype ROIC consists of 64 channels. The signal voltage output from the ROIC is fed into the ADC attached to the driving board, where the analog signals are converted into digital signals. These digital signals then undergo digital signal processing via the MCU to produce high-quality image information.

Fig. 2 shows the block diagram for each of the 64 channels in the ROIC. Each channel's readout circuit is based on a CTIA interface circuit. The input for each channel is designed with pads to connect to the pixel. The readout circuit operates in two modes: a basic readout mode and a sensitivity adjustment mode for the integrated signal. In the basic readout mode, the pixel bias is set to the reference voltage (V_{REFI}) by the initial reset switch ($Ø_{RSTI}$) of the CTIA. This setup leverages the characteristics of the negative feedback amplifier, ensuring a stable and adjustable bias. The charge signal generated by the pixel is input in the form

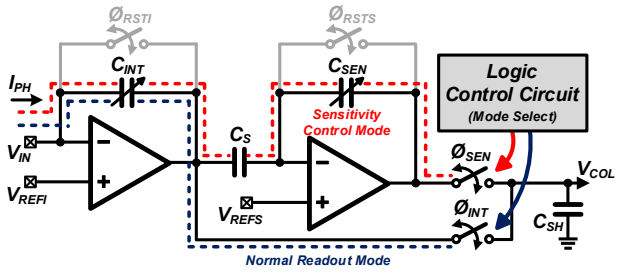
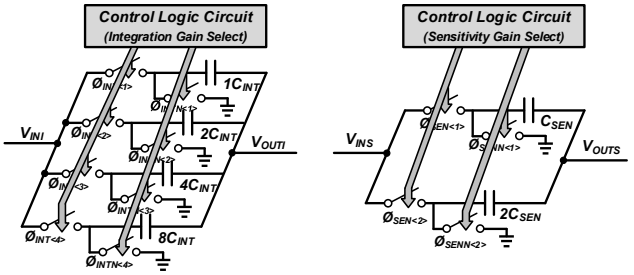


Fig. 3. Simplified signal flow depending on operational modes.



(a) (b)

Fig. 4. (a) Integration gain control. (b) Sensitivity gain control.

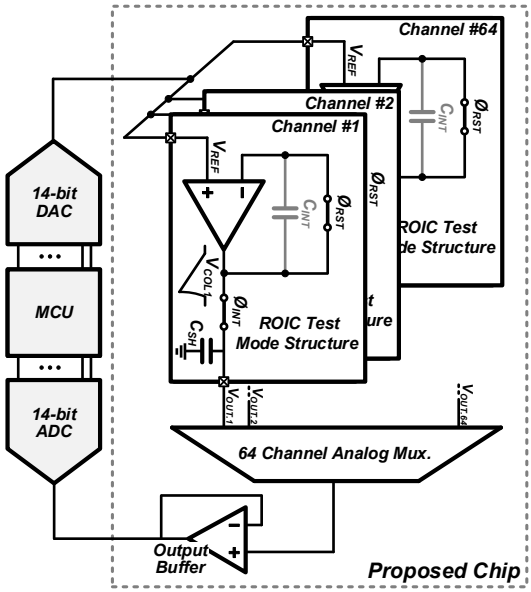


Fig. 5. Block diagram of verification mode for ROIC channel.

of a current and begins to integrate and convert to voltage through the CTIA's integration capacitor (C_{INT}). This converted voltage is proportional to the input photocurrent (I_{PH}) and the integration time (t_{INT}), and it is inversely proportional to the C_{INT}. The readout circuit is designed to allow for variable values of C_{INT}, enabling the selection of gain when converting the input current signal to voltage. This feature provides flexible control over the pixel's selectivity. In the sensitivity adjustment mode, the initial setting is performed by the reset switch ($Ø_{RSTS}$), which sets the amplifier to the reference voltage (V_{REFS}). After integration, the charge corresponding to the voltage change integrated by the CTIA accumulates on the sampling capacitor (C_S). The sensitivity is adjusted based on the values of C_S and the sensitivity capacitor (C_{SEN}). The value of C_{SEN} is also variably designed to adjust the sensitivity of the pixel signal to constant light. This flexibility helps mitigate the physical limitations of the pixel. The outputs from both modes are sampled onto the sampling capacitor (C_{SH}) during the integration time and are sequentially sent to the output buffer through an analog multiplexer (Mux.). The number of input terminals in the analog multiplexer corresponds to the number of channels, which in this design, is 64 channels.

Fig. 3 illustrates the signal conversion process and mode settings for the ROIC in two different modes. In the normal readout mode, the current generated by the charge flow from the pixel is input into the CTIA interface, where it is converted into a voltage signal. The conversion process can be described by the following equation:

$$C_{INT} \times \Delta V = I_{PH} \times t_{INT} \quad (1)$$

$$V_{OUTI} = V_{REFI} - \Delta V \quad (2)$$

$$\text{Where, } \Delta V = (I_{PH} \times t_{INT}) / C_{INT} \quad (3)$$

Here, V_{OUT} is the output voltage, I_{PH} is the photocurrent generated by the pixel, t_{INT} is the integration time, and C_{INT} is the integration capacitor. The gain of the conversion is determined by the value of C_{INT}. Assuming the charge generated by the pixel is constant and t_{INT} is fixed, the gain can be adjusted by varying C_{INT}. The converted signal is sampled to C_{SH} by the $Ø_{INT}$ timing. In the sensitivity adjustment mode, the charge corresponding to the voltage change converted by the CTIA accumulates on the C_S capacitor. The output of the sensitivity adjustment mode, V_{OUTS}, is determined by integrating the charge accumulated on C_{SEN}, starting from the initial reference value, V_{REFS}. The charge accumulated on C_{SEN} is equal to the charge accumulated on C_S. Therefore, the output value V_{OUTS} is the voltage change converted at the interface multiplied by the gain determined by the values of C_S and C_{SEN}. This process can be described by the following equation:

$$\Delta Q_{CS} = \Delta V \times C_S \quad (4)$$

$$V_{OUTS} = \Delta Q_{SEN}/C_{SEN} + V_{REFS} \, (\Delta Q_{CS} = \Delta Q_{SEN}) \quad (5)$$

$$\text{Where, } VOUTS = (\Delta V \times C_S/C_{SEN}) + V_{REFS} \quad (6)$$

Where V_{OUTS} is the output voltage of the sensitivity adjustment mode, V_{REFS} is the reference voltage, ΔV is the voltage change, C_S is the sampling capacitor, and C_{SEN} is the sensitivity capacitor. Both modes are set by the $Ø_{SEN}$ and $Ø_{INT}$ signals and are controlled by the logic control circuit. During the integration process, the $Ø_{SEN}$ and $Ø_{INT}$ signals are opposite to ensure that only one mode is selected at a time. The timing of sampling the output values is also controlled.

Fig. 4 explains how the conversion gain in the interface (CTIA) stage and sensitivity adjustment stage is controlled through the logic control circuit. In the interface stage, the CTIA is designed with four selectable structures, each having capacitors set at multiples to adjust the conversion gain. The values of these capacitors allow for a maximum

gain adjustment up to 16 times. This gain adjustment is crucial for optimizing the signal conversion based on the input photocurrent and the desired output voltage. Similarly, the sensitivity adjustment stage consists of two selectable structures with capacitors also set at multiples, allowing for a maximum gain adjustment up to 4 times. These capacitors, when not used for integration, function as load capacitors for the amplifier. This dual functionality helps in reducing noise by decreasing the bandwidth. The gain control for these stages is managed through signals $Ø_{INT<1:4>}$ and $Ø_{SEN<1:2>}$. Corresponding signals $Ø_{INTN<1:4>}$ and $Ø_{SENN<1:2>}$ are set oppositely to ensure precise control. All these signals are managed by the logic control circuit, which orchestrates the gain adjustments dynamically based on the operating conditions and input signal characteristics. This design aims to enhance the versatility and performance of the ROIC by providing adjustable conversion gain. By doing so, it expands the selection range for target pixels and improves noise performance. This adaptability is essential in integrating the ROIC with the pixels, helping to mitigate the limitations of pixel performance and achieving optimal imaging quality.

Fig. 5 shows the test structure for verifying the ROIC. This verification test uses an analog ramp waveform output from a 14-bit DAC [19] as the input signal. The 14-bit DAC is controlled by an MCU on the driving board. To verify the ROIC, the interface stage (CTIA) is set to unit gain buffer mode. When the analog ramp waveform from the DAC is input to the VREF node, the output value of the CTIA can be checked for verification. During this process, sampling is not performed, and the analog multiplexer is configured to fix one column value and send it to the output driver. This process is repeated identically for all 64 channels, and the output signal is connected to the input of a 14-bit ADC [20]. The output of the ADC can be monitored through the MCU. This method is a standardized structure for verifying CTIA-based ROICs and is used to validate the ROIC through this approach.

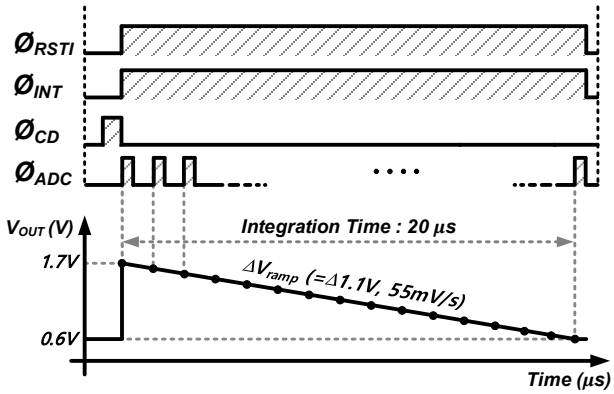


Fig. 6. Simplified test timing diagram.

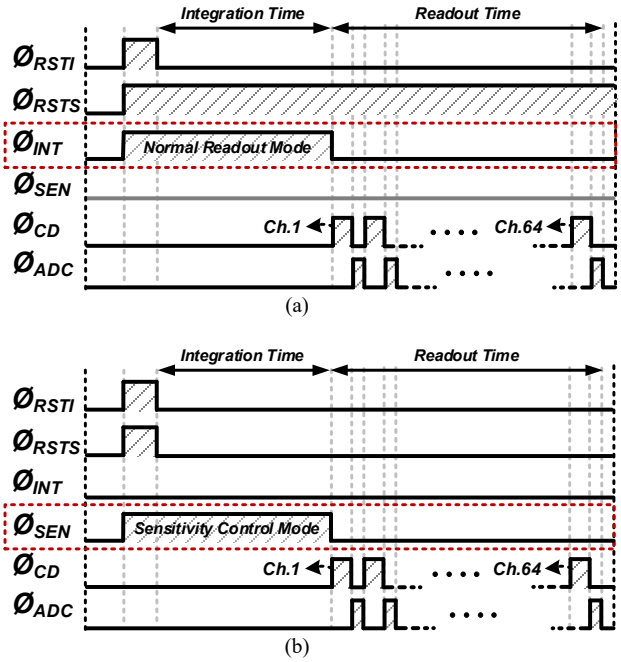


Fig. 7. Simplified operational timing diagram of two modes: (a) normal readout mode, (b) sensitivity control mode.

III. RESULTS AND DISCUSSIONS

Fig. 6 shows the timing and output waveform in the verification mode of the ROIC. In this mode, the CTIA is initially kept in the $Ø_{RSTI}$ reset state and is configured in a unit gain buffer structure. The $Ø_{INT}$ signal is used to set the standard readout circuit mode. The $Ø_{CD}$ signal serves as the selection signal for the analog multiplexer, allowing for the selection of channels from the first to the 64th. During the integration time, the output of only one channel is maintained. During this period, the output value of the ramp signal input through the DAC is fed into the ADC, and the resulting output can be monitored through the MCU. A 20µs integration time is set for the measurement process, and the ramp signal is generated to operate within the CTIA amplifier's output swing range of 1.1V. The change rate of 55µV per 1µs was observed through the ADC output, and the stability was verified with an error margin within 1LSB of the ADC.

Fig. 7 shows the simplified operational timing diagrams for two modes: normal readout mode and sensitivity adjustment mode. This diagram illustrates how each mode is selected through the timing of the $Ø_{INT}$ and $Ø_{SEN}$ signals. In the normal readout mode, the amplifier used in the sensitivity adjustment mode remains reset by the $Ø_{RSTS}$ signal. This means that the sensitivity adjustment amplifier does not participate in the signal readout process, ensuring the standard readout operation is maintained. In the sensitivity adjustment mode, both $Ø_{RSTI}$ and $Ø_{RSTS}$ signals are used to set the initial values. During the integration time, the change in the voltage value converted by the interface stage is taken as the input, and the gain is selected to adjust the sensitivity. This mode allows for fine-tuning the signal based on the initial voltage changes. In both modes, sampling is conducted through the sampling capacitor (C_{SH}) during the integration time. The analog multiplexer then sequentially outputs the values from the first to the 64th channel to the output buffer, and the output values are fed into the ADC. This operational timing ensures that the functions of both modes are efficiently managed, allowing

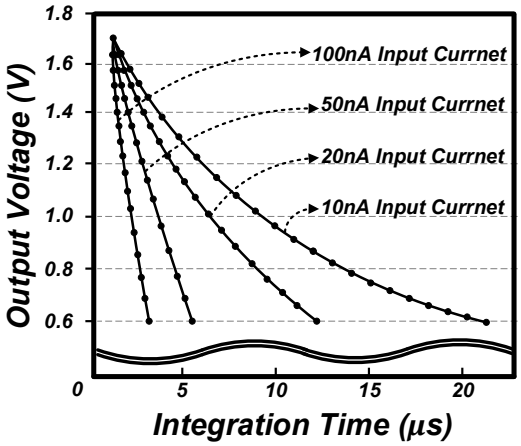


Fig. 8. Measured output voltage characteristics in normal readout mode.

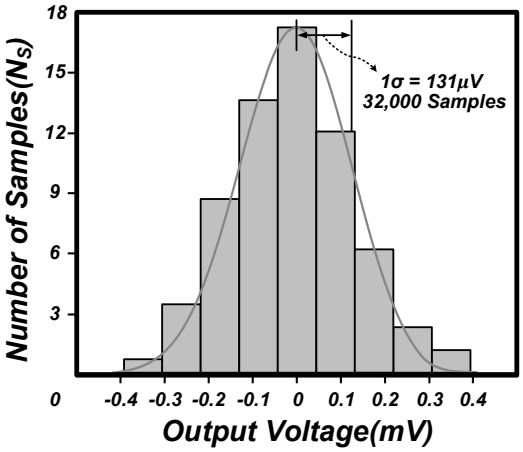
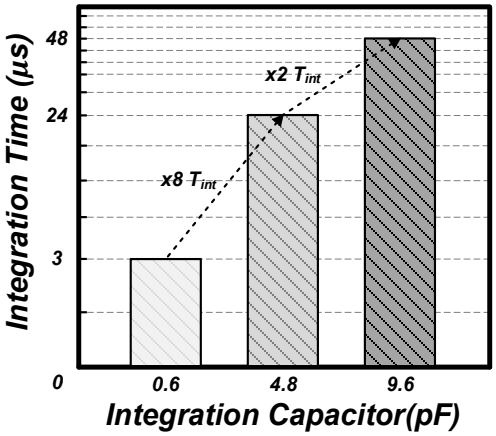
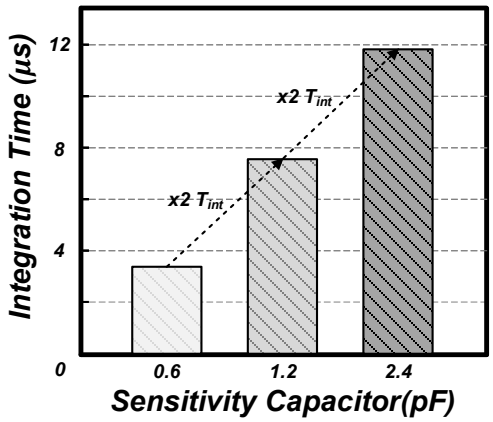


Fig. 10. Measured output noise histogram of prototype ROIC.



(a)



(b)

Fig. 9. Measured output voltage characteristics in (a) CTIA gain adjustment, and (b) sensitivity adjustment.

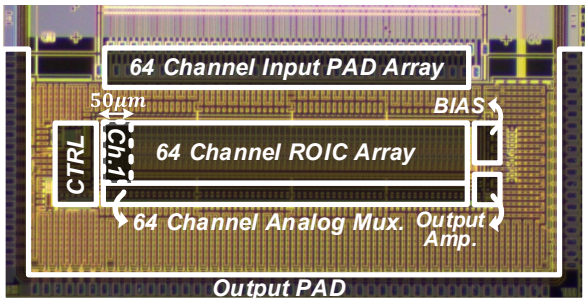


Fig. 11. Microphotograph of the prototype ROIC chip.

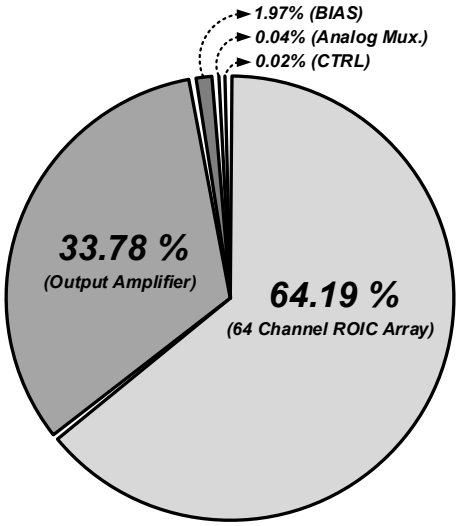


Fig. 12. Power Consumption distribution of proposed chip.

for accurate and flexible readout of the SWIR imaging system.

Fig. 8 shows the measured output voltage from the interface CTIA of the prototype ROIC under various test conditions. This graph illustrates the output voltage and the integration time required to reach the set saturation level for different input currents applied to each interface CTIA. The tests were conducted with an integration capacitor value set to the minimum of 0.6pF. The input currents used for the tests were 10nA, 20nA, 50nA, and 100nA. The results demonstrate that as the input current increases from 10nA to 20nA, 50nA, and 100nA, the time required to reach the set saturation voltage of 0.6V decreases approximately by factors of 2, 5, and 10, respectively. This verification confirms the inverse relationship between the input current from the pixel and the integration time, indicating that the ROIC operates reliably and efficiently. The findings validate that the ROIC can stably handle various input currents, maintaining accurate and predictable performance across different operating conditions.

TABLE I. PERFORMANCE SUMMARY

Parameter	Value
Technology	0.18 μm
Total area	5 × 2.5 mm^2
Pixel Type	InGaAs detector
Channel Pitch	50 μm
Channel Array	64
Random Noise	119.48 μV_{rms}
Power Consumption	26.55 mW

TABLE II. PERFORMANCE COMPARISION

Parameter	This Work	SD7110 Ref. [21]	ISC9717 Ref. [22]
Technology	0.18 μm	0.5 μm	0.5 μm
Total area	5 × 2.5	12.7 × 5.2	11.2 × 4.7
Pixel Type	InGaAs detector	-	-
Channel Pitch	50 μm	150 μm	80 μm
C_{INT}	0.6~9.6 pF	0.5~4.0 pF	0.5~4.0 pF
Channel Array	64	128	128
Random noise	448 e^-_{rms}	400 e^-_{rms}	500 e^-_{rms}
Power Consumption	26.55 mW	230.1 mW	220 mW

Fig. 9 presents the verification results of conversion gain in two modes. The interface CTIA converts current to voltage, while the sensitivity adjustment CTIA takes the converted voltage signal as input and adjusts the sensitivity. The conversion gain for both modes can be varied by adjusting the integration capacitor, with a maximum change of up to 16 times for the interface stage and 4 times for the sensitivity adjustment stage. In Fig. 9(a), the results of the interface CTIA's conversion gain are shown. The integration capacitor was set to minimum (0.6pF), middle (4.8pF), and maximum (9.6pF) values. The saturation voltage time was measured at each setting with the input current fixed at 100nA. The results demonstrate that the time to reach the saturation voltage at the minimum capacitor value of 0.6pF is 8 times longer than at 4.8pF and 16 times longer than at 9.6pF. This confirms that the time to reach the set saturation voltage is proportional to the variable gain of the integration capacitor. In Fig. 9(b), the results for the sensitivity adjustment CTIA's conversion gain are detailed. The change in voltage converted by the interface stage is used as the input, and the time to reach the saturation voltage was measured according to the sensitivity adjustment capacitor values. When the capacitor values were set to minimum (0.6pF), middle (1.2pF), and maximum (2.4pF), it was observed that changing from 0.6pF to 1.2pF doubled the time, and changing to 2.4pF quadrupled the time. These results demonstrate the flexibility in controlling the gain and sensitivity adjustment during the current-to-voltage conversion, effectively mitigating the limitations of pixel performance.

Fig. 10 shows the output noise histogram of the prototype ROIC, which is crucial for evaluating the random noise (RN) characteristics of the device. To determine the standard deviation of the noise, the experimental procedure involved capturing 32,000 samples in test mode. When operating within its full input voltage range of 1.1V, the total measured RN was 131μV_{rms}. The contributions to this total noise from external sources included 43.9μV_{rms} from the external ADC and an additional 30.9μV_{rms} from the external DAC. By subtracting these known external noise contributions from the total measured noise, the intrinsic noise level of the ROIC itself was isolated and identified, resulting in a calculated value of 119.48μV_{rms}.

Fig. 11 presents a microscope photograph of the designed ROIC chip along with its detailed specifications. The chip was fabricated using a 0.18μm 1P6M (1 poly 6 metal) CMOS process. The total area of the chip is 5 × 2.5mm², with each channel designed to fit a 50μm pitch. For operation and verification, an I/O pad array is arranged, which is integrated with a verification PCB via wire bonding. The input current for each channel can be tested using a resistor array that models the pixel operation through the external PCB. The ROIC operates at a master clock speed of 20MHz, with a total power consumption of 26.55mW. In the proposed ROIC chip, the blocks contributing to the noise can be identified as the ROIC core array and the output driver. The ROIC core array comprises a CTIA-based interface circuit array and a bias circuit, designed to convert the charge generated by the pixel into a voltage. Noise simulations were conducted using the standardized methods provided by the Design Tool's Noise Simulation feature. The simulations covered a frequency range from 1Hz to approximately 100kHz, which is about five times the -3dB frequency of the amplifier, to estimate the input referred noise. The results indicate that the noise from the ROIC core array is 2.656μVrms, accounting for 14.7% of the total noise. In contrast, the output buffer contributes significantly more noise, measured at 15.3μVrms, representing 85.2% of the total noise. These findings demonstrate that the majority of the overall noise originates from the output buffer, which is a reasonable conclusion given its function and design within the ROIC. This chip is a prototype ROIC aimed at InGaAs-based compound semiconductor pixels for infrared imaging systems, developed to provide stable variable conversion gain and flexible pixel selection, making it suitable for key performance requirements in infrared imaging systems.

Fig. 12 illustrates the power consumption of each block within the proposed ROIC. The total power consumption is 26.55 mW. Among the blocks, the 64-channel ROIC Array consumes the largest portion, accounting for 64.19% of the

total power. This is followed by the Output Buffer, Bias Circuit, Analog Mux., and Control Logic Block, in descending order of power consumption.

Table I presents a performance summary of the prototype ROIC. The proposed prototype ROIC is designed for an InGaAs-based compound semiconductor pixel infrared imaging system. The total area of the ROIC chip is 5 × 2.5 mm², and it consists of an array of 64 channels, with each channel having a pitch of 50 μm. The random noise of the chip is measured to be 119.48 μV_{rms}, and the total power consumption is 22.55 mW, making it suitable for infrared imaging applications.

Table II compares the key performance metrics of the proposed ROIC with previous studies [21], [22]. The proposed design utilizes a 0.18μm process and operates at 3.3V, targeting InGaAs-based pixels with a 50μm pixel pitch. The proposed structure employs a variable integration capacitor with a maximum value of 9.6pF, enhancing the flexibility in pixel selection. In terms of random noise, the proposed ROIC demonstrates comparable performance to similar structures. Additionally, the total power consumption is significantly lower than that of comparable structures, achieving more than an eightfold reduction.

IV. CONCLUSION

This study introduces the design of a 64-channel prototype ROIC targeted for InGaAs-based compound semiconductor pixels in SWIR imaging systems. The developed ROIC has undergone thorough validation at the silicon level using standardized verification methods, ensuring its stability. comprehensive analysis of the performance parameters has been conducted. The primary goal of this research is to generate and validate innovative concepts to enhance various aspects of SWIR imaging performance.

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