Floating Gate Radiation Sensor Interface ICs with Regulated-Cascode Current Reference and Time-Based Quantizer

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***Abstract* - This paper proposes power-efficient ICs for measuring the signal of a Floating Gate (FG) radiation sensor. The ICs include the function of converting the current signal generated in the FG into a digital signal through a regulated-cascode current reference (RCCS) and a time-based quantizer. The proposed sensor interface ICs are implemented with the PDK of DB Hitek process, securing a 45 dB SNR with only 14.7 µW power consumption.**

***Keywords*—Radiation Sensor Interface ICs, Floating Gate radiation sensor, Time-based quantizer**

I. INTRODUCTION

Radiation detection electronic systems reported to date are broadly classified into two main types. The first type utilizes traditional radiation detectors [1], which feature large volumes and high accuracy due to the use of radiation sensors requiring high operating voltages. The second type consists of modular radiation detectors [2], which utilize radiation sensors requiring relatively low operating voltages, leading to smaller sizes but lower resolution.

Recently, to overcome the drawbacks of photodiode-based radiation detection systems, integrated circuits for FG-based radiation sensor interfaces have been proposed [3]. FG-based radiation sensors exploit the Total Ionizing Dose (TID) effect [4], associated with changes in semiconductor device performance (such as Vth variation, leakage current, etc.), to convert radiation particles into light signals, eliminating the need for bulky scintillators.

FG-based radiation detection systems operate by detecting the leakage current generated in the FG. The FG-based radiation detection system proposed in [3] measures the oscillation frequency per unit time of the clock signal outputted from the oscillator by inputting the current signal generated in the FG into a current-controlled oscillator. However, such FG-based radiation detection systems suffer from issues such as counter overflow and high-power consumption.

In this paper, we propose overcoming the drawbacks outlined in [3] by utilizing a time-based quantizer based on a differential phase detector, ensuring low power consumption and high resolution with 1st order noise shaping performance.

II. DESIGN METHODOLOGY

A. System Configuration

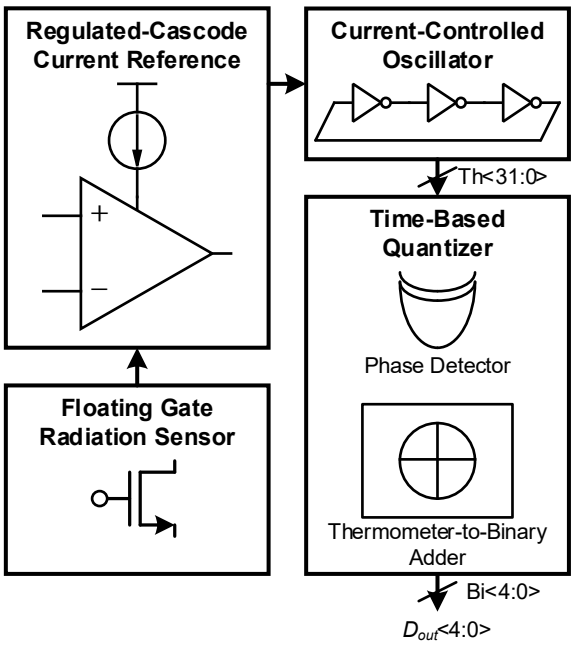

Fig. 1. System configuration of proposed FG radiation sensor interface ICs

Fig. 1. depicts the architecture of the FG-based radiation sensor interface ICs proposed in this study. The FG radiation sensor, modeled as a resistor, is designed to vary its value due to radiation particles, and it modulates the current value determined by the feedback loop of the regulated-cascode current reference circuit. The modulated current signal alters the phase of the current-controlled oscillator (CCO), which

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is then detected by the Phase Detector (PD) consisting of D Flip-Flops (D FFs) and XOR gates.

The cascaded D FFs and PD result in quantization noise shaping to the 1st order during the process of generating the difference between the previous and current phases [5]. This prevents an increase in output bit count, resolution, and power consumption by avoiding the escalation of the number of PD arrays. In this study, 31 thermometer bits are outputted from 31 PD arrays at a 1 MHz sampling clock, and after passing through an adder, 5 binary bits are generated as output.

B. Detailed Implementation

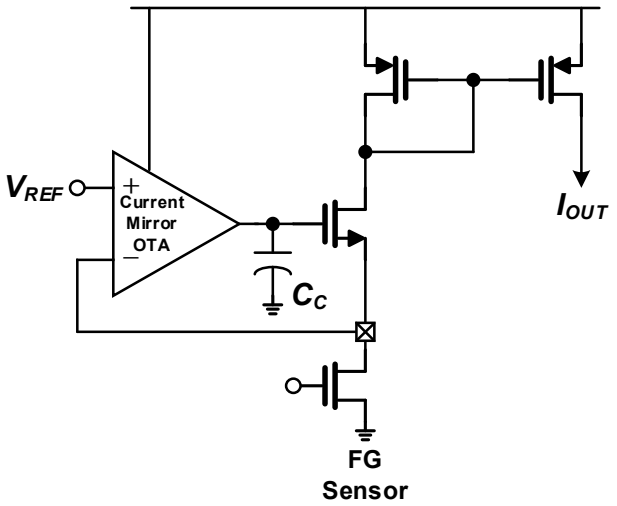

Fig. 2. Schematic of regulated-cascode current reference for FG radiation sensor

Fig. 2. illustrates the circuit diagram of the RCCS designed in this study. The FG-based radiation sensor, modeled as a resistor RFG, assumes a variable range of 0.9 Mohm to 1.1 Mohm, designed to vary the current from 0.9 µA to 1.1 µA. The bandwidth of the radiation signal is set to 1 kHz, while the bandwidth of the internal feedback loop gain of the RCCS is designed to be 100 kHz. The RCCS consumes an average power of 12.9 µW and ensures sufficient linearity to transmit signals generated from the FG sensor to the CCO.

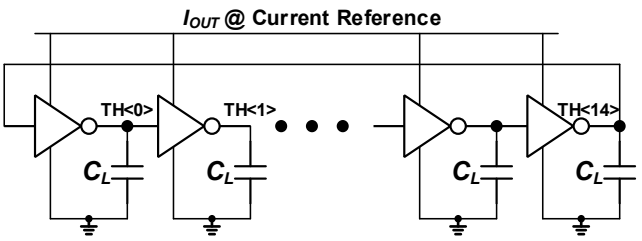

Fig. 3. Schematic of inverter-based ring oscillators

Fig. 3. presents the implementation results of the ring oscillator-based CCO composed of 31 stages. The oscillation frequency of the CCO is set to 100 kHz, and it is designed to detect the output value of the CCO at each rising edge of the 1 MHz sampling clock.

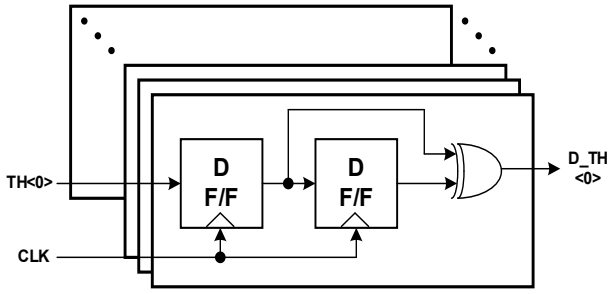

Fig. 4. Schematic of phase detector circuit with cascaded D flip-flops

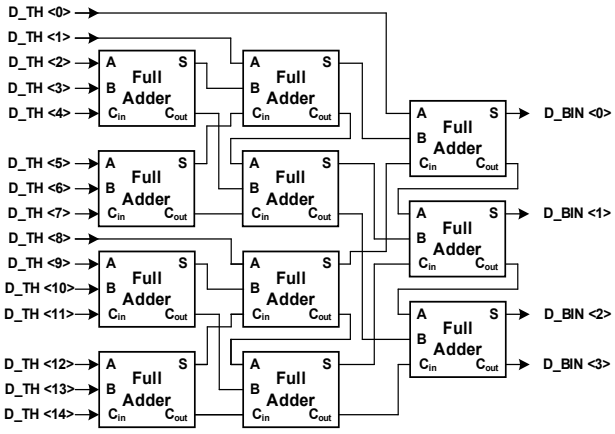

Fig. 5. Schematic of thermometer-to-binary adder

Fig. 4. displays the implementation results of the PD circuit consisting of two cascaded D FFs and XOR gates. The 31 thermometer bits detected from the PD arrays connected to the outputs of 31 CCOs represent a 5-bit binary digital output. Fig. 5. illustrates the implementation results of the adder for summing up the thermometer outputs to produce a binary 5-bit output. The implemented quantizer shown in Fig. 4. to 5. operates at 1 MHz and is simulated to consume 1.8 µW of power.

III. RESULTS AND DISCUSSIONS

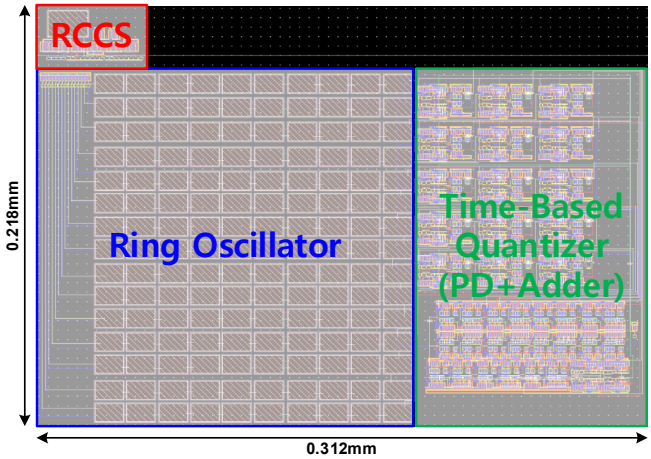

Fig. 6. Layout of proposed FG radiation sensor interface ICs

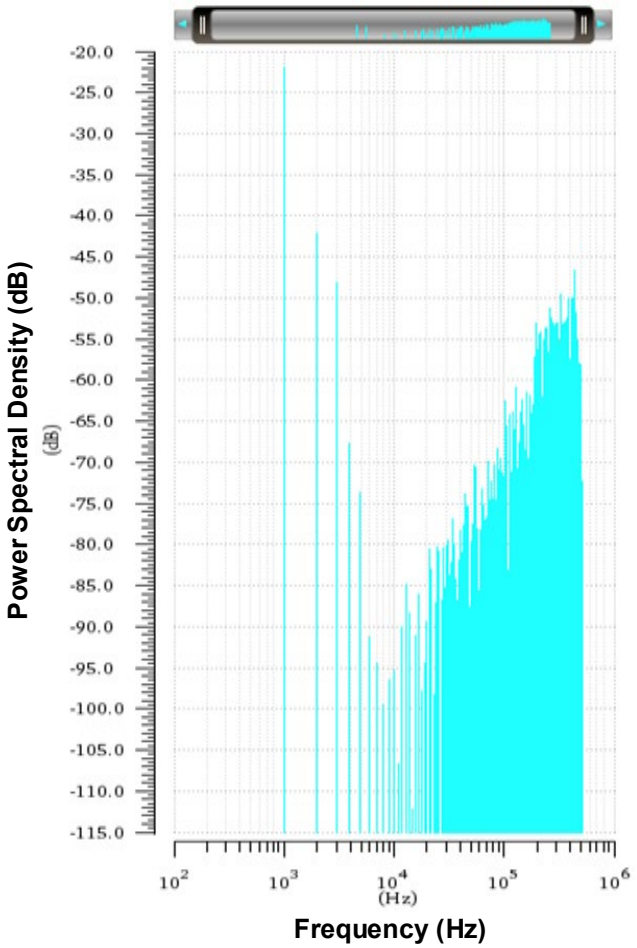

Fig. 7. Post layout simulation results of proposed FG radiation sensor interface ICs

Fig. 6. shows the layout design results of the circuit described earlier. The implemented circuit occupies an area of 0.068 mm^2, and the post-layout simulation results (Fig. 7.) confirm an SNR of 45 dB for the quantizer. However, it should be noted that while the SNR is 45 dB, the SNDR is significantly lower at 25 dB. The cause of this low SNDR is attributed to linearity issues in the CCO, which will be addressed through digital backend calibration.

IV. CONCLUSION

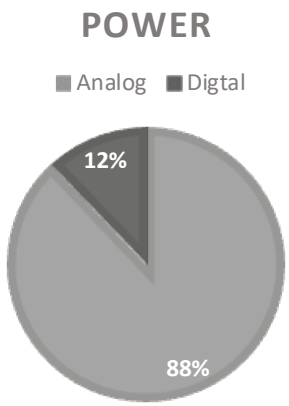

Fig. 8. Power breakdown

TABLE I. Performance Summary

Parameters	This Work
Process	0.18um BCDMOS
Area	0.0680mm^2
F_{OSC} of CCO	100kHz
Sampling Frequency	1MHz
SNR	45dB
Power Consumption	14.657uW

This paper proposes an integrated circuit for FG-based radiation sensor interface utilizing RCCS, CCO, and time-based quantizer. As shown in Fig. 8, the total power consumption was 14.7 μW, with analog occupying 88% and digital occupying 12%. Although a relatively high level of SNR (45 dB) was achieved, improvements are necessary due to the low linearity.

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