On-Die Noise Monitoring Circuit for System-Level ESD

KyungHoon Lee, Sangyeong Jeong, and Jingook Kim[a]
School of ECE, Ulsan National Institute of Science and Technology
E-mail : khlee95@unist.ac.kr, sangyeong@unist.ac.kr, jingook@unist.ac.kr

***Abstract* - Electrostatic discharge (ESD) poses a significant risk to electronic systems, potentially leading to operational malfunctions. Accurately assessing the noise waveforms induced within these systems is challenging due to various factors such as common mode (CM) noise, direct radiation coupling, and limited accessibility of external equipment. To tackle these hurdles, a novel approach involving an on-die monitoring circuit (OMC) has been proposed for integration within electronic systems. This embedded circuit enables precise measurement of noise without external interference. The OMC, can detect abnormal noise levels surpassing predefined thresholds on both signal and power networks, accurately capturing their waveforms. To validate its practicality, the OMC was implemented in a evaluation board and tested in ESD experiments. Unlike traditional oscilloscope equipment vulnerable to CM noise, the OMC successfully isolated and measured only the relevant differential mode (DM) noise generated within the system. This showcases its ability to isolate and quantify target DM noise even in complex environments, overcoming limitations of conventional equipment.**

***Keywords*— Analog-to-digital converter (ADC), delay locked loop (DLL), electrostatic discharge (ESD), monitoring circuit, common mode (CM), differential mode (DM)**

I. INTRODUCTION

ESD occurrences, often triggered by human activities, can result in diverse failures within electronic systems [1], [2]. To ensure product safety and customer satisfaction, ESD concerns should be addressed early in the product design phase. Consequently, adherence to international standards [3] necessitates the implementation of ESD immunity tests for all electronic products.

Addressing ESD risks demands a comprehensive understanding. Numerous studies have delved into ESD analysis and explored methods to enhance immunity. One approach involved near-field ESD scanning to identify susceptible networks within a system [4]. In [5], a technique was proposed to forecast system-level ESD coupling using frequency domain measurements. Additionally, [6] introduced a method leveraging a partial element equivalent circuit (PEEC) model to compute ESD coupling to the system, effectively reducing simulation time. Soft failures induced by ESD in flip-flops on a simplified motherboard were examined and analyzed [7], exploring the potential of decoupling capacitance to mitigate ESD-induced failures in D-flipflops. Furthermore, investigations were conducted into the primary cause of ESD-induced jitter in a delay-locked loop (DLL), which is crucial for timing data communication [8].

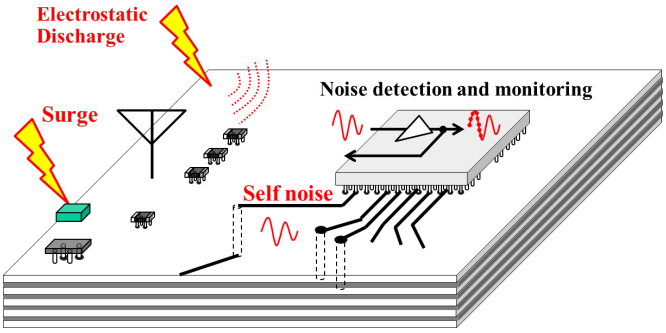

Fig. 1. The on-die monitoring Circuit integrated into a system to quantify effects.

Past research primarily focused on systems tethered to earth ground, such as personal computers or infrastructure. However, the impact of ESD extends to devices lacking earth grounding, such as mobile phones. Numerous studies have examined ESD or HPEM noise affecting systems independent of earth ground. The systematic analysis of ESD-induced noise in mobile phones led to the identification of soft failures, which were investigated through simulation and characterization [9]. Similarly, the investigation of ESD-induced soft failures in wearable devices prompted the proposal of immunity solutions [10].

This paper introduces an on-die monitoring circuit (OMC) designed to address constraints associated with measurement techniques utilizing cables and digital oscilloscopes. The OMC is encapsulated within a compact package to monitor transient noises induced by ESD within a system, a task challenging to accomplish using external equipment, as depicted in Fig. 1. When ESD occurs, radiated noise and common mode (CM) noise can be generated, which may be coupled into the measurement cable or equipment, making accurate measurement challenging. However, by using OMC to measure noise, it is possible to accurately capture only the noise induced in the system, as there are no coupling cables or equipment.

a. Corresponding author; jingook@unist.ac.kr

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II. CIRCUIT DESIGN OF THE ON-DIE MONITORING CIRCUIT

A. The operating mechanism of the on-die monitoring circuit

The OMC was proposed to detect when transient noise is applied to the power distribution network (PDN) or signal net of the system and to sample and reconstruct the injected noise. Fig. 2. represents the Block Diagram of the OMC for noise monitoring.

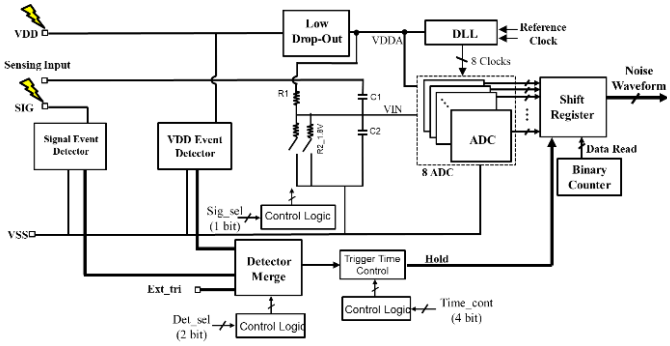


Fig.2. Diagram illustrating the on-die monitoring circuit.

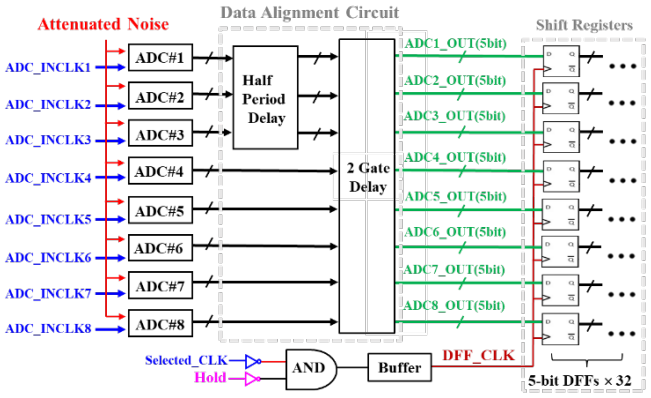


Fig.3. (a) The process where the digital output of eight ADCs is transmitted to the Shift Register. (b) Eight multiphase clocks generated by DLL. (c) Eight aligned ADC digital outputs and DFF_CLK.

The OMC operation overview is as follows: Low Drop-Out receives VDD of 3V ~ 5V as input and outputs a constant 1.8V to supply voltage to the blocks that constitute the system. By introducing sensing input, the design was aimed at enabling the reconstruction of not only power noise but also signal noise optionally. Outside the IC, VDD (or Signal) is connected to the sensing input, and the transient noise injected into the VDD (or Signal) is input into the system. Sensing Input is floating by default. The OMC can be characterized by applying a sine wave directly to the sensing input that is not connected to any net. Noise injected into the sensing input is attenuated by C1 and C2. Fig. 3(a) shows the process in which noise applied through the sensing input is sampled and stored in shift registers. The attenuated noise due to the capacitance ratio (by C1 and C2) is applied to the VIN of eight analog to digital converters (ADCs). The delayed locked loop (DLL) block receives a reference clock from an external clock source of the IC and generates eight multiphase clocks, ADC_INCLK1 to ADC_INCLK8, with a difference between phases of 1/8 period, as shown in Fig. 3(b). ADC_INCLK1 to ADC_INCLK8 are applied in order from ADC1 to ADC8. Since the phase difference between adjacent ADC_INCLK is T/8, 8 ADCs have a sampling rate that is eight times faster than 1 ADC. The 5-bit digital output from eight ADCs (ADC1_OUT to ADC8_OUT) is simultaneously transmitted to the Shift Register by DFF_CLK. The output of ADC1~ADC3 was delayed by half a period. Due to this delay, it was possible to secure the timing margin of DFF_CLK as much as T/2, as shown in Fig. 3(c). DFF_CLK is applied by selecting one of the DLL's eight multiphase clocks, expressed as Selected_CLK. Hold signal is generated by VDD or Signal Event Detector. The hold signal, activated when a noise-inducing event occurs in the system, halts the shift register's operation, allowing the data corresponding to the noise waveform to be stored. It is selected which detector will be used: VDD or Signal. When a voltage higher than the threshold voltage is injected into VDD or Signal Net, the detection signal of the event detector changes from 0 to 1. The hold signal intersects with an AND gate to halt the DFF_CLK. Because the clock is not applied, shift registers no longer shift data, and digital data including noise information is stored. Through simulation, it was confirmed that there is approximately a 2ns logic delay in the event detector and combinational logic. Additionally, it is possible to further delay the hold signal beyond 2ns using the trigger time control logic in Fig. 2.

Data can be extracted by externally applying the read clock while the hold signal is high. The binary counter increases by 1 according to the read clock and outputs the stored data in order. The extracted digital data is reconstructed into analog data through an appropriate software process. Due to the limitations of the ADC used in the OMC, only noise levels up to a maximum of 2.8 Vpp were evaluated.

B. Principle of noise injection to VSS causing system malfunction

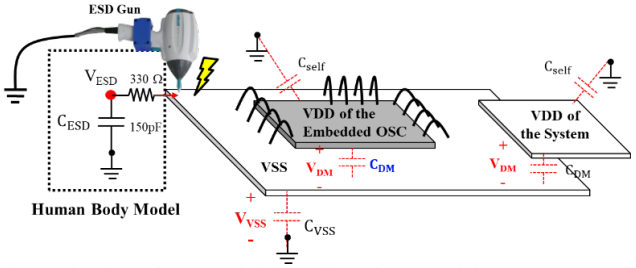


Fig. 4. Situation when ESD is injected into the VSS of the system.

$$V_{VSS} = \left(\frac{C_{ESD}}{C_{ESD} + C_{VSS}} \right) V_{ESD} \quad (1)$$

$$V_{DM} = -\left(\frac{C_{self}}{C_{self} + C_{DM}} \right) V_{VSS} \quad (2)$$

The VSS net typically encompasses the largest area within electronic systems, as it serves as the pathway for most current returns. Consequently, in many systems, ESD tends to affect the VSS net most significantly. Therefore, when subjecting VSS to ESD, it becomes crucial to comprehend the differential mode (DM) voltage between VDD and VSS applied to the system. Fig. 4 illustrates a scenario where ESD is introduced into the VSS of a system interconnected with the embedded OSC via wire bonding, sharing the same VDD and VSS. ESD is introduced through the depicted Human Body Model (HBM). The VDD and VSS of the system are linked by differential mode capacitance, C_{DM}. Additionally, the VDD net in the systems is associated with an ideal ground through self-capacitance, C_{self}. When ESD is applied into VSS, the VSS voltage (V_{VSS}) is determined by dividing the voltage by the capacitance contained in the HBM (C_{ESD}) and the capacitance between VSS and ideal ground (C_{VSS}), as shown in (1). C_{ESD} represents the modeling of a human's self-capacitance, ensuring that the self-capacitance component is considered in the design of the ESD gun. The DM voltage between VDD and VSS (V_{DM}) is determined based on the voltage distribution ratio of C_{DM} and C_{self}, as shown in (2). Compared to C_{DM}, C_{self} is significantly smaller because VDD and ideal ground are farther apart than VDD and VSS, typically separated by several hundred micrometers. If V_{VSS} remains within a few volts, V_{DM} is nearly 0V since C_{self} is negligible. However, when a voltage of several kV, such as ESD, is introduced into VSS, the influence of C_{self} becomes significant. As V_{VSS} increases, V_{DM} also rises by several volts, leading to noise between VDD and VSS (V_{DM}), which can result in system malfunctions.

III. RESULTS AND DISCUSSIONS

A. Manufacture of OMC evaluation board

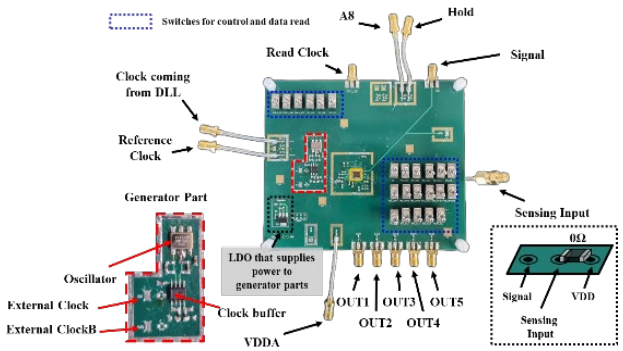


Fig. 5. Photograph of the PCB used to evaluate the OMC IC.

Fig. 5 depicts an evaluation printed circuit board (PCB) designed to assess the performance of the manufactured IC. At the core of the board, the IC is mounted using the chip-on-board (COB) method. The external clock, utilized by the OMC, is generated within the generator section. The clock generated by the voltage-controlled crystal oscillator (VCXO), operating in the low voltage pseudo emitter-coupled logic (LVPECL) method, is routed to the IC's clock input via a clock buffer. Positioned below is a low dropout regulator (LDO), responsible for converting the external voltage into a stable 3.3V supply voltage supplied to the generator section. The hold cable serves the purpose of verifying the operation of the event detector, generating a hold signal when activated. Switches are provided for controlling the functionality of the IC. Additionally, 5-bit digital output data, obtained via ADC, is routed through OUT1 to OUT5 Ports. Positioned at the lower right corner of Fig. 5 is the Sensing Input. By connecting this input to a 0Ω resistor, users can designate which net to reconstruct, either VDD or signal. In the image, the sensing input depicts VDD being connected.

B. ESD injection into VSS to verify the Embedded OSC

In Section II-B, when ESD is injected into the VSS of the system, the principle of injection as DM noise between VDD and VSS calculated as (2) was discussed. To validate this, an experimental setup was arranged to inject ESD into the VSS of the evaluation PCB, depicted in Fig. 6. The Sensing input and VDD were externally connected to 0Ω, enabling the measurement and reconstruction of DM noise between VDD and VSS. The ESD Gun, connected to earth ground via a grounding strap, was positioned to apply ESD into the VSS of the PCB. To mitigate the influence of noise radiating from the ESD gun on the IC, a metal cage shielded the ESD, while copper tape shielded the IC. The measurement cable linking the oscilloscope was shielded with copper and wrapped with ferrite to minimize the impact of radiated noise and CM noise generated during ESD injection.

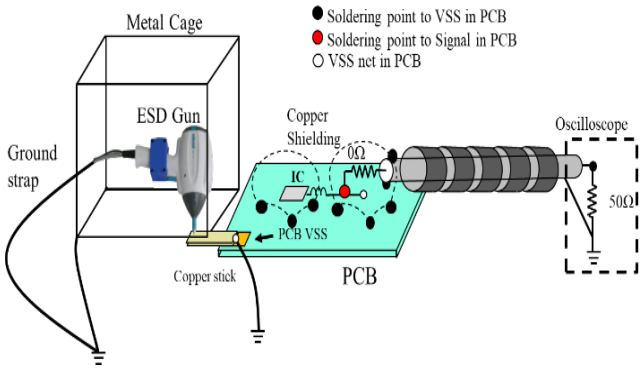
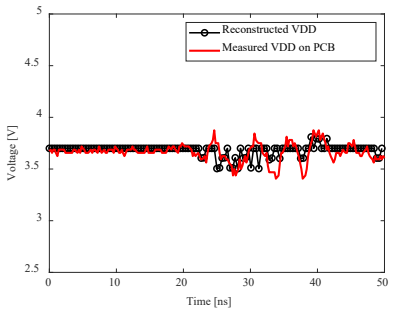
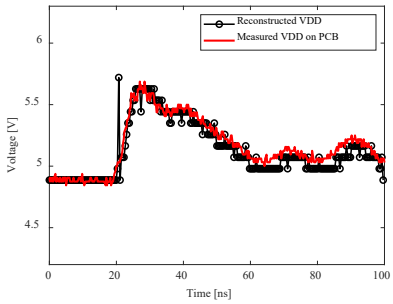


Fig. 6. Experimental setup for injecting ESD into the VSS of the evaluation PCB.



(a)



(b)

Fig. 7 (a) 12kV charging voltage ESD injection into VSS at 320Mhz external clock with 1.5nF VDD de-cap. (b) -4kV charging voltage ESD injection into VSS at 320Mhz external clock without VDD de-cap.

Fig. 7 (a) shows that the measured VDD corresponds to the reconstructed VDD when 12kV charging voltage ESD is injected into VSS of the evaluation PCB with 1.5nF VDD decoupling capacitor (de-cap). According to (1), as C_{DM} increases, the V_{DM} approaches zero. Consequently, even though ESD was injected into VSS, the DM noise was barely detected. Fig. 7 (b) shows that the measured VDD correspond to the reconstructed VDD when -4kV charging voltage ESD is injected into VSS of the evaluation PCB without VDD de-cap. Here, the external clock is 320MHz, the sampling rate is 2.56GHz, and the capturing time is 100ns. The consistency between the reconstructed VDD and the measured VDD has been confirmed. The voltage applied to VSS is measured as DM noise resulting from self-capacitance. The voltage polarity observed by the charging voltage exhibits negativity, whereas the measured noise exhibits the opposite polarity. This discrepancy is because, during ESD injection into VSS, the voltage being measured by the OSC and OMC represents the voltage of VDD relative to VSS.

IV. CONCLUSION

The introduction of the On-die Monitoring Circuit (OMC) enables the measurement of VDD to VSS DM noise without requiring external equipment connections. By utilizing the eight multiphase clocks output from the DLL, the ADC achieves an eightfold increase in sampling rate. Additionally, the removal of the de-cap between VDD and VSS enhances the measurement of DM noise.

In the ESD experiments at the VSS of the evaluation PCB, interfering with accurate measurements CM noise and radiated noise were thoroughly shielded during the measurements. As a result, it was confirmed that the noise waveforms reconstructed by the OMC matched those measured through the oscilloscope equipment accurately.

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Kyunghoon Lee received the B.S. degree in electronic engineering from Myong-ji University, Yongin, Republic of Korea, in 2021, and the M.S. degree in electrical engineering from Ulsan National Institute of Science and Technology (UNIST), Ulsan, Korea, in 2024.

His research interest includes analog circuits design, and electro-magnetic compatibility (EMC).

Sangyeong Jeong received the B.S. and Ph.D. degrees in electrical engineering from the Ulsan National Institute of Science and Technology, Ulsan, South Korea, in 2015 and 2021, respectively. Since March 2021, he has been working at the IC&EMC Laboratory at the Ulsan National Institute of Science and Technology, Ulsan, South Korea, as a postdoc fellow. He is also with EMcoretech Inc.. His current research interests include electromagnetic compatibility (EMC) problems in the power system and the noise reduction techniques by using integrated circuits (ICs).

Jingook Kim (M′09-SM′15) received his B.S., M.S., and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejon, Korea, in 2000, 2002, and 2006, respectively. From 2006 to 2008, he was with DRAM design team in Memory Division of Samsung Electronics, Hwasung, Korea, as a senior engineer. From January 2009 to July 2011, he worked for the EMC Laboratory at the Missouri University of Science and Technology, Missouri, USA, as a postdoc fellow. In July 2011, he joined the Ulsan National Institute of Science and Technology (UNIST), Ulsan, Korea, where he is currently a professor. He is also with EMcoretech Inc.. His current research interests include EMC, ESD, RF interference, and analog circuits design.