A *V*-Band CMOS Frequency Doubler in 65 nm CMOS

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***Abstract* – This article introduces a high output power and high conversion gain millimeter-wave CMOS frequency doubler. The frequency doubler adopts the optimum transistor size and gate bias voltage to achieve high output power, high conversion gain and high efficiency. The measured results demonstrate a peak conversion gain (CG) of 1.45 dB, a peak DC-to- RF efficiency of 11.26 % and a saturated output power of 5.65 dBm at 63 GHz. At the peak CG, the 3-dB bandwidth is 8.9 GHz from 57 to 65.9 GHz. The fundamental rejection is larger than 10.75 dB from 57 to 66 GHz. The chip area, including RF and DC pads, is 0.4 × 0.5 mm^2 in 65-nm CMOS process. The power consumption is 12 mW at an input power of 0 dBm.**

***Keywords*: 60 GHz, CMOS, conversion gain, efficiency, frequency doubler, fundamental rejection, millimeter-wave, multiplier, output power, *V*-band.**

I. INTRODUCTION

Wireless communication and sensing applications in the millimeter-wave bands, which offer wide available bandwidth, are emerging to meet the demand for high performance and high speed. The transceivers operating in the millimeter-wave band have achieved data rates over 10 Gb/s [1-4]. These transceivers require an oscillator to generate local oscillator signals. However, silicon-based fundamental voltage-controlled oscillator (VCO) in the millimeter-wave band has difficulty in achieving a wide tuning range, high output power and good phase noise as the frequency increase. Compared to a 60 GHz fundamental VCO, a 30 GHz VCO with a frequency doubler provides greater transconductance and tank inductance with higher capacitor quality factor under same DC power and device size [5].

The frequency doublers have been implemented using a variety of topologies [6]–[9]. The design of the frequency doubler requires performances such as wide bandwidth, second harmonic output power (P_{OUT}), DC-to-RF efficiency (η), conversion gain (CG) and fundamental rejection (FR). A transformer-based doubler with an output buffer [9] has achieved a peak η of 19.5%, a CG of 0.8 dB and a saturated power (P_{sat}) of 5.7 dBm at 66 GHz. However, adding the output buffer significantly increases the chip size and power consumption. Similarly, the push-push VCO topology showed a high peak η over 20% and a P_{sat} larger than 8 dBm [6], [9]. However, both approaches require high input power and large chip area.

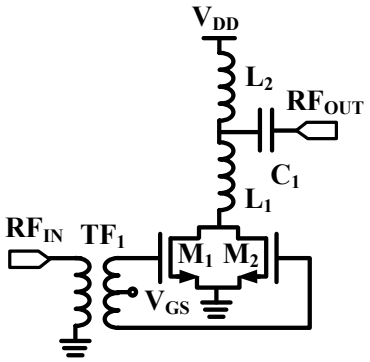

Fig. 1. Schematic of the designed frequency doubler.

In this study, we present the design of a millimeter-wave frequency doubler operating at 56–67 GHz, achieving high conversion gain and high output power within a small chip area using a 65-nm CMOS process. The proposed frequency doubler achieves a P_{sat} of 5.65 dBm, a peak η of 11.26 % at 63 GHz. A peak conversion gain of 1.45 dB is achieved from an input power of 0 dBm at 63 GHz. Section II describes the architecture and implementation of the frequency doubler. Section III presents the simulation and measurement results, and conclusion is presented in section IV.

II. CIRCUIT DESIGN

Fig. 1 depicts the schematic of the frequency doubler. The input transformer (TF) is used to convert single-ended signals to differential signals, which are then fed into the transistors M1 and M2. The drains of M_1 and M_2 are combined, where the output currents of M_1 and M_2 suppress odd harmonics. L_1 and L_2 are used for the output matching network for the second harmonic frequency rather than the matching network with capacitor and inductor for robust impedance matching. The balanced design achieves good suppression of the fundamental leakage (FL) and the high output power for second harmonic. The second harmonic of the frequency doubler is obtained from the nonlinear characteristics of M_1 and M_2. To analyze the operation principle of the NMOS transistor, we used the Taylor expansions from [10]. The simplified drain currents of M_1 and M_2 from the Taylor expansions can be expressed as shown below:

$$i_{DS} = I_{DS} + g_m V_{in}(t) + \frac{1}{2!} g_{m2} V_{in}(t)^2 + \frac{1}{3!} g_{m3} V_{in}(t)^3 + \cdots , \qquad (1)$$

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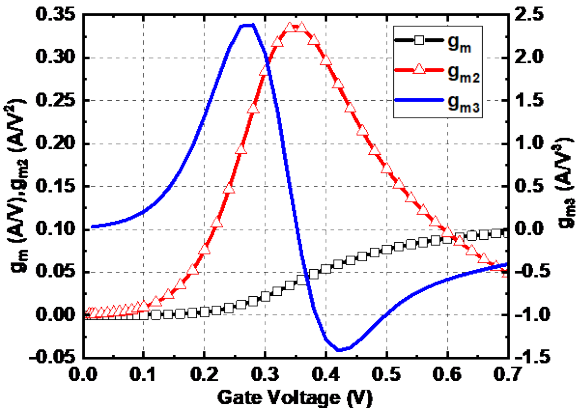


Fig. 2. Simulated transcoductance of NMOS.

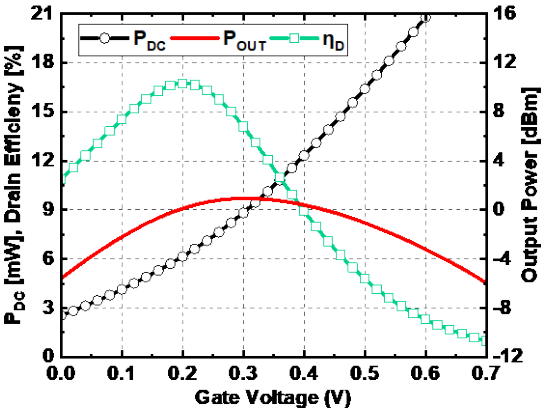


Fig. 3. Simulated P_{DC}, P_{OUT}, and η_D at 31.5GHz with input power of 0 dBm.

Where $V_{in}(t)$ is the input voltage and I_{DS}, g_m, g_{m2}, and g_{m3} are the DC current of the drain, the transconductance, the second order derivative of i_{DS} with respect to $V_{in}(t)$ and the third order derivative of i_{DS} with respect to $V_{in}(t)$, respectively.

Fig. 2 shows g_m, g_{m2} and g_{m3} versus gate voltage. As the gate bias increases, the fundamental output continuously increases, while the second harmonic and third harmonic outputs degrade beyond certain voltages. In the simulation, a gate voltage of 0.36 V gives the highest g_{m2} of 0.33 A/V^2. Additionally, the transistor size affects power consumption (P_{DC}), CG and P_{OUT}. Smaller transistor size limits CG and P_{OUT}, while large transistor size results in higher P_{DC} and limited η.

Fig. 3 shows the simulation results of P_{OUT}, P_{DC}, and drain efficiency (η_D). In this simulation, the transistor size for M_1 and M_2 is chosen as 40 μm to achieve optimum efficiency and P_{OUT}. At an input power of 0 dBm, a gate voltage of 0.3 V provides an optimal P_{OUT} of 0.95 dBm, but a low η_D of 14.1 %. Meanwhile, at a gate voltage of 0.2 V, the frequency doubler shows an optimal η_D of 16.74 %. However, P_{OUT} is 0.13 dBm. To simultaneously obtain optimal P_{OUT} and η_D, we chose a gate bias voltage of 0.25 V, which provides a P_{OUT} of 0.74 dBm, and an η_D of 16.06 %. All the transformer, inductors, interconnections, and capacitors are optimized and designed using electromagnetic (EM) simulation.

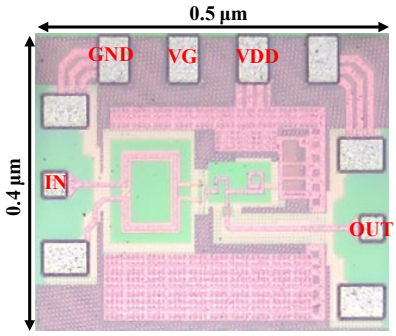


Fig. 4. Microphotograph of proposed frequency doubler.

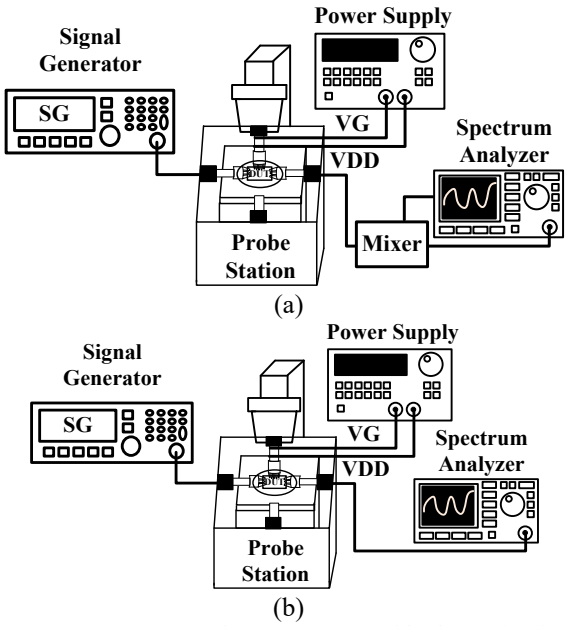


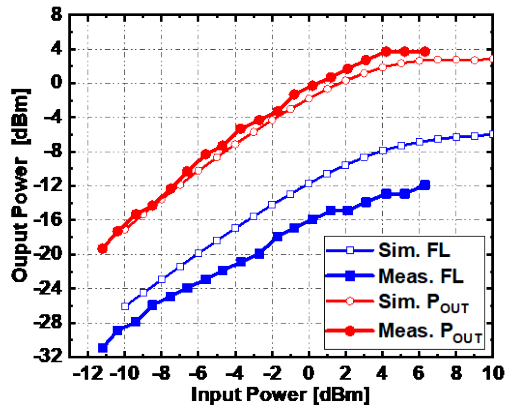
Fig. 5. Measurement set-up of (a) output power with a harmonic mixer and (b) fundamental leakage (FL).

III. EXPERIMENTAL RESULTS

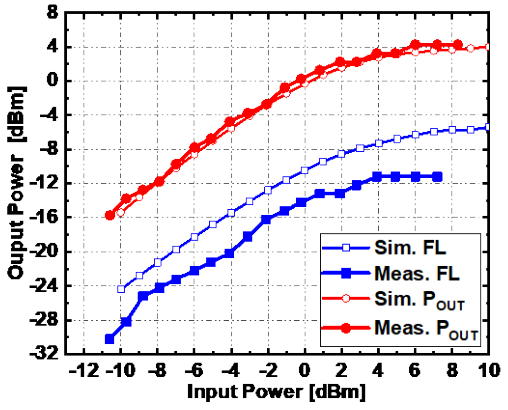
The proposed frequency doubler was implemented in a 65-nm CMOS technology. Fig. 4 shows the microphotograph of the frequency doubler. The chip size, including RF and DC pads, is 0.5 × 0.4 mm^2, while the core size without the pads is 0.295 × 0.17 mm^2. The frequency doubler consumes 12 mW from a supply voltage of 1 V. The frequency doubler is measured on-wafer using GSG probes.

Fig. 5 shows the measurement set-up for P_{OUT} and fundamental leakage (FL). The P_{OUT}, CG and FL were measured using a signal generator and a spectrum analyzer. All losses associated with the probe, cable and mixer were de-embedded from the measurement results.

Fig. 6 depicts the simulated and measured P_{OUT} and FL. The simulated and measured P_{sat} and saturated FL are shown in Fig. 7. The measured P_{sat} is larger than 3.7 dBm from 57 to 66 GHz. The measured peak P_{sat} is 5.65 dBm at 63 GHz. The measured FL is less than -8.6 dBm from 57 to 66 GHz. Therefore, measured FR is larger than 12.75 dB from 57 to 66 GHz. The measured FL and FR are limited due to imperfect balun performance of TF_1, which has a phase error of 22.9 ° and an amplitude error of 3.8 dB in the simulation.



(a)



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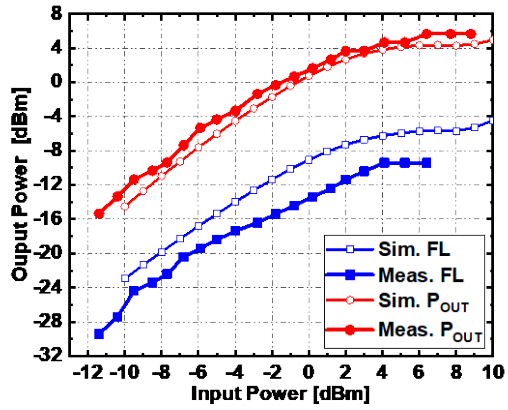
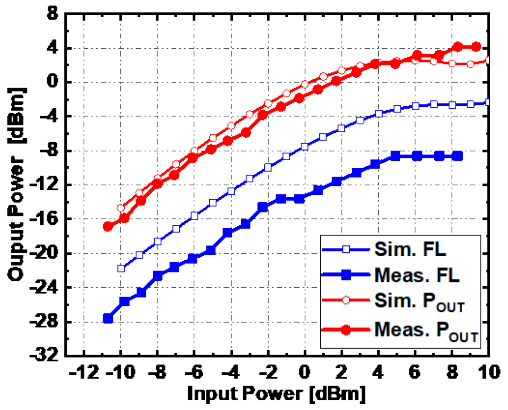


(c)



(d)

Fig. 6. Simulated and measured P_{OUT} and FL versus the input power at (a) 57 GHz, (b) 60 GHz, (c) 63 GHz and (d) 66 GHz.

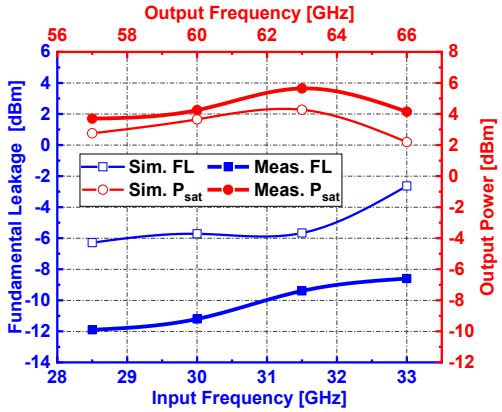


Fig. 7. Simulated and measured results of P_{sat} and FL versus input frequency at an input power of 6dBm.

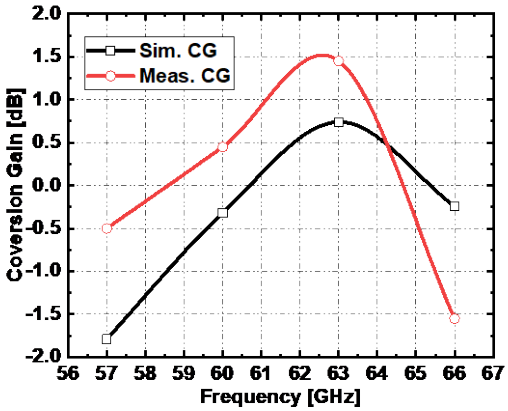


Fig. 8. Simulated and measured CG versus output frequency at an input power of 0 dBm.

The measurement results of P_{sat} and FL are better than the simulation results due to the larger DC power consumption in the measurement and imperfect modeling of active and passive components.

Fig. 8 illustrates the simulated and measured CG. The measured maximum CG is 1.45 dB at 63 GHz, and the CG is more than -1.6 dB from 57 to 66 GHz. The 3-dB bandwidth of the CG is 8.9 GHz from 57 to 65.9 GHz.

Fig. 9 shows the measured CG and η versus input power. At an input power of 0 dBm, the maximum CG is -0.5, 0.45, 1.45 and -1.55 dB at 57, 60, 63 and 66 GHz, respectively. The peak η is 11.2%, 9.4%, 11.26% and 6.2 % at 57, 60, 63 and 66 GHz, respectively. At the input power of 0 dBm, the η is 7.75%, 8.18%, 9.11% and 4.37 % at 57, 60, 63 and 66 GHz, respectively. The proposed doubler consumes 12 mW and 26 mW at input power of 0 dBm and 7 dBm, respectively, at 66 GHz.

Table I summarizes the performance the comparison with state-of-the-arts. The proposed frequency doubler achieves the highest CG of 1.45 dB at an input power of 0 dBm, high P_{sat} of 5.65 dBm and the smallest chip size of 0.2 mm^2.

IV. CONCLUSION

In this letter, we present the V-band frequency doubler. The optimum transistor size and gate bias voltage are studied

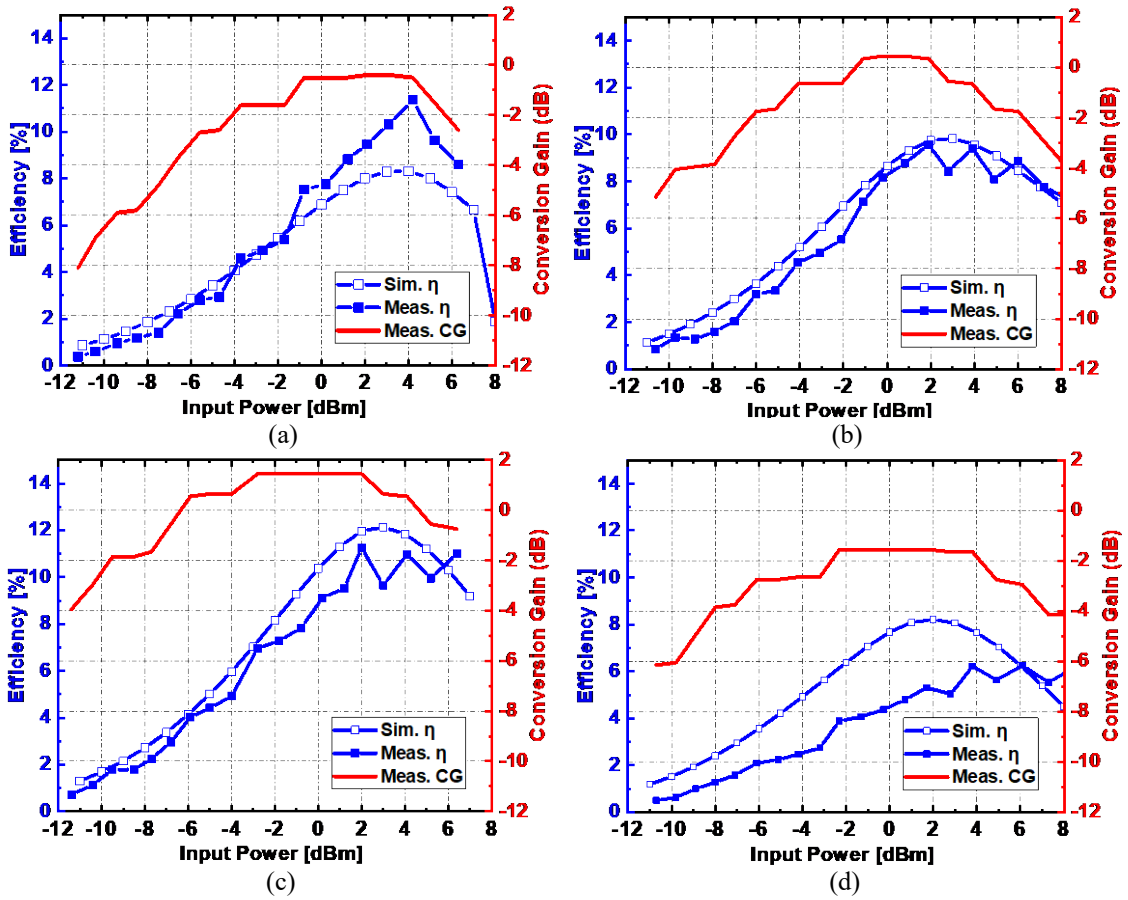


Fig. 9. Measured CG and simulated/measured DC-to-RF efficiency (η) versus input power at (a) 57 GHz, (b) 60 GHz, (c) 63 GHz and (d) 66 GHz.

TABLE I
Performance Comparison with Various V-band Frequency Doublers

Ref.	Tech.	Output Buffer	P_{IN} (dBm)	V_{DD} (V)	BW_{3dB} (GHz)	P_{sat} (dBm)	Peak *η (%)	**FR (dB)	CG_{peak} (dB)	Area (mm^2)	P_{DC} (mW)
This work	65nm CMOS	No	-10 ~ 8	1	57-65.9	5.65	11.26	>10.8	1.45	0.2	12
[6]	65nm CMOS	No	0 ~ 12	0.6	45.5-67	8	22.2	>26	-3.2	0.95	12-15
				1		10.1	21.88	>33	-1.8		26-32
[7]	65nm CMOS	No	-8 ~ 8	1	62-90	-1~2	9.7	>20	-5.5~ -2.5	0.27	9-14
[8]	65nm CMOS	Yes	-10 ~ 7	1	55-77	5.7	19.5	>30	0.8	0.33	14

*η (%) = $P_{OUT}/(P_{IN}+P_{DC})*100$ **FR : Fundamental rejection

to achieve high output power, high conversion gain and high efficiency. Implemented in a 65-nm CMOS technology, the frequency doubler achieves a P_{sat} of 5.65 dBm, a peak CG of 1.45 dB and peak η of 11.26 % at 63 GHz. The 3-dB CG bandwidth is 8.9 GHz. At an input power of 0 dBm, P_{DC} is 12 mW from a supply voltage of 1 V.

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His research interests include millimeter-wave integrated circuit design.

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Chul Woo Byeon received his Ph.D. degree in Electronic Engineering from KAIST, Deajeon, Korea, in 2013. His doctoral research focused on low-power millimeter-wave/RF integrated circuit, antenna, and package design.

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