The Closed-Loop Neural Interface Available Simultaneously Recording and Stimulation Using Fast Convergence Stimulation Artifact Removal

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***Abstract* - The closed-loop neural interface is an actively researched field with broad applications. However, it has a serious issue in that stimulation itself makes huge artifacts (~mV) in the recording system saturating the amplifier, contaminating bio-signal (~ 50μV) and the post-analysis during a disturbed period. Several stimulation artifact removal (SAR) techniques were presented but have trade-offs between conversion time and algorithm accuracy. Here, we suggested a closed-loop neural interface with a fast convergence SAR algorithm while sustaining adequate removal accuracy. The amplifier-free ADC-direct 2nd-order continuous delta-sigma modulator recording stage is adopted to provide ~15 μV_{rms} input-referred integrated noise from 5Hz to 5kHz which is adequate to record bio-signal. Also, it succeeds in recording ~10mV signals about the size of the stimulation artifact. The fast-convergence SAR module provides stable accuracy under the versatile recording environment. The chip is designed using the TSMC 65-nm CMOS process. The chip is composed of 18 input channels, 2 SAR blocks, one stimulation channel, and 2 CIC filters for down-sampling. The entire chip area is 1mm^2.**

***Keywords*—Closed-loop neural interface, Stimulation artifact removal, Fast convergence, On-chip processing**

I. INTRODUCTION

Neuromodulation has gradually attracted attention to relax and cure incurable diseases. Some devices already target tremor suppression (Cala Health), rheumatoid arthritis (Galvani Bioelectronics), Parkinson's disease (Medtronic, Abbott Laboratories), and hearing loss (Cochlear Americas). In addition, neuromodulation is showing the possibility of vision damage [1] and recovery of consciousness in a vegetative state [2]. However, the majority of currently available neuromodulation devices are adopting open-loop control systems that stimulate the target regardless of the current state. Since excessive stimulation can cause side effects [3], it needs to be adjusted in real-time according to the user's condition and desired purpose using a closed-loop control system.

One of the biggest problems of this method is the strong interference (~10) that occurs due to stimulation having more than 1000 times larger size than the size of the real bio-signal (~10) [4]. Since the stimulation artifact frequency range could be overlapped with the bio-signal band, this can′t be removed by simple frequency filtering (Fig. 1). It saturates the recording stage, disturbs signal processing, and leads to malfunctioning of closed-loop control. As a solution to this issue, we present the high dynamic range input stage and the advanced stimulation artifact rejection technique.

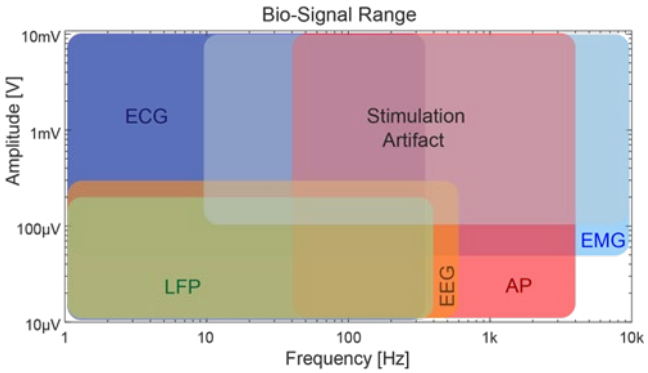

Fig. 1. Bio-signal range in frequency and amplitude. Stimulation artifacts could overlap almost all bio-signals in the frequency range [4-7].

The stereotype recording stage consists of an amplifier (AMP) and Analog to Digital Converter (ADC). Each part has an affordable input range (normally less than the supply voltage level). Since AMP increases the signal size and sends it as ADC input, AMP works like reducing input range by its voltage gain. Our previous work [8] succeeded in solving this problem by utilizing ADC-direct topology which tackles this problem by eliminating AMP and using noise shaping to deal with the problem of increased quantization noise by disappeared AMP gain.

After the signal is recorded correctly, the next problem is bio-signal contamination due to stimulation artifacts. For closed-loop processing, it is necessary to identify the physical condition in real-time and appropriately control the stimulus, but when the bio-signal is contaminated by a huge stimulation artifact, the signal processing process is hindered, making it difficult to perform accurate operations. To

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remove the artifact, several methods were suggested from simple linear interpolation [9] to complex active filter methods [10]. The interpolation method replaces the data in the contaminated section with fake signals, resulting in information loss. The active filter method can minimize information loss by removing only artifacts information, but it takes a long learning time to achieve optimal performance, which is a major disadvantage in a continuously changing bio-environment. Here, we present a fast and accurate active filter method to create the artifact template using the weighted average technique [11]. Depending on the current accuracy state variable, the filter is configured to convert the algorithm to a method with high accuracy/long learning time and a method with low accuracy/fast learning time so that it can respond quickly to artifact changes. On-chip feature extraction module calculates the spectral power and sends a feedback signal to the stimulator and the Cascaded Integrator-Comb (CIC) filter is used for down-sampling and low-pass filtering.

II. DESIGN METHODOLOGY

A. Circuit Design and Implementation

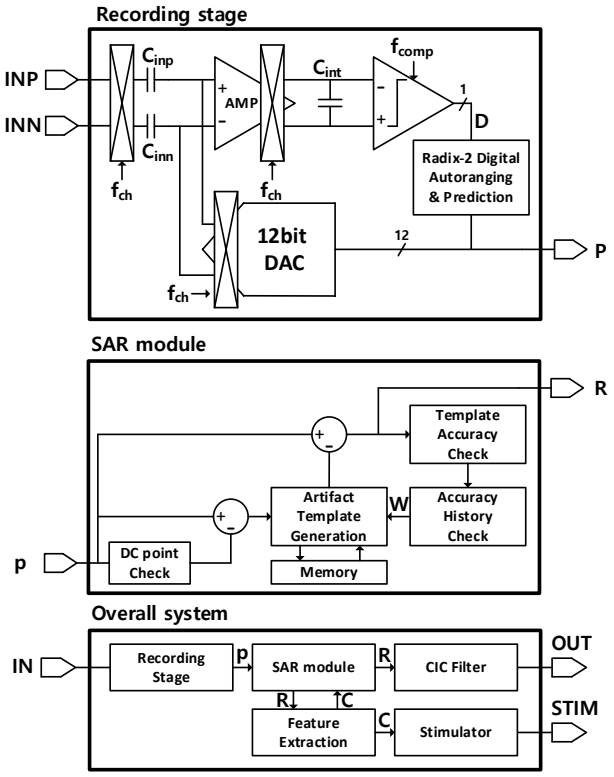

Fig. 2. Entire circuit implementation. The upper shows the detailed design of one input channel, the middle shows the data flow of SAR logic and the bottom shows the overall composition of the chip.

Fig. 2 shows the overall chip configuration. The upper part of Fig. 2 shows one input channel configuration. Details have already been illustrated in our previous work [12]. Each input channel has a dedicated 2nd-order Delta-Sigma Modulator (DSM) in an ADC-direct configuration. The input is chopped at fch to segregate flicker noise from the input signal band. A 1-bit quantizer compares integrated errors at fchop. Using the output of the quantizer (D), the digital auto-ranging and prediction module controls the size of the LSB of the quantizer and predicts the input signal (P). P is chopped and fed backed to the input side through a 12-bit Capacitive Digital to Analog Converter (CDAC). The error signal re-enters the analog integrator and cycles through the feedback loop.

The predicted signal (P) enters the SAR module to remove the stimulation artifact. P is DC-canceled and weighted averaged to generate an artifact template based on the weighting factor (W). The contaminated prediction signal (P) is subtracted by the template signal and produces a recovered clean signal (R). By checking R, the template accuracy check module determines the size of the residue artifact, and controls W for the next learning cycle. R is passed through the CIC filter for down-sampling and low-pass filtering to make the final output.

R is also entered into the feature extractor to determine the current state. The feature extractor calculates spectral power to check the current target state and turns the stimulator on or off based on a threshold. The stimulation control signal (C) provides feedback to SAR logic to indicate when the stimulation is activated.

The stimulator is designed based on an H-bridge circuit which has an advantage in charge-balancing between anodic and cathodic phase stimulation. After each stimulation phase, a discharge switch is turned on to quickly solve residual charges at the stimulation electrode.

The CIC filter is first simulated using MATLAB Simulink to find the proper parameters to cancel the noise-shaped high-frequency noise of the 2nd-order DSM. In the Fig. 3, the top plot shows input data characterizing 20dB/dec increasing noise of the delta-sigma ADC output. The middle plot shows FFT plots of CIC outputs in different order from 0 (down-sampling only) to 3. The bottom plot is an overlay plot of the middle. It shows that after the 2nd order, the noise performance starts to saturate. Since a higher order CIC filter needs more bits ($\log_2(OSR)$) and stages, the 2nd order CIC is selected.

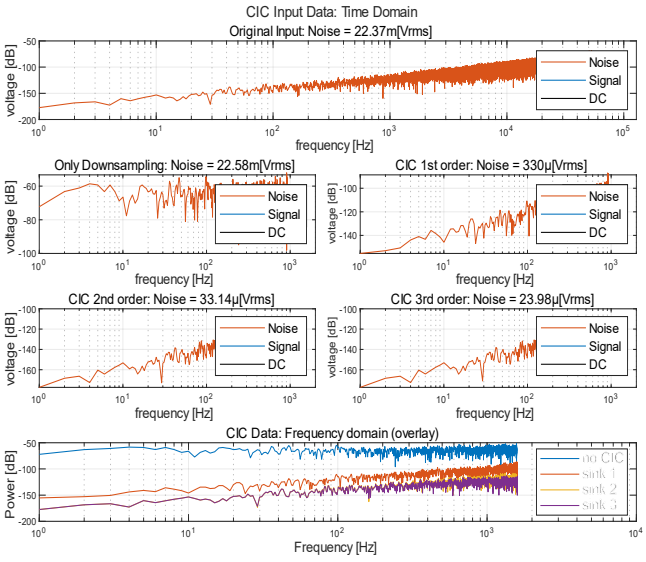

Fig. 3. MATLAB CIC simulation test result.

B. Chip Design Considerations

It is important to create the artifact template as quickly as possible to deal with the dynamically changing environment of biosystems. DC fluctuations are clearly distinct from the stimulation artifact frequency. At the same time, DC fluctuations could contain valuable information. By separating DC fluctuations only during the template generation phase, we can preserve all frequency ranges of the bio-signal, including DC.

Updating the weighting factor based on current stimulation template accuracy is important to ensure a high-quality output signal and later signal processing stage. Fig. 4 shows how stimulation artifact rejection delay is changed based on the weight factor updating policy. A fixed factor shows slow convergence. If the factor changes in the range of high accuracy mode, it shows almost similar changes in fixed mode. The best performance was conducted when factor changes in full range and achieved < 15 cycles delay.

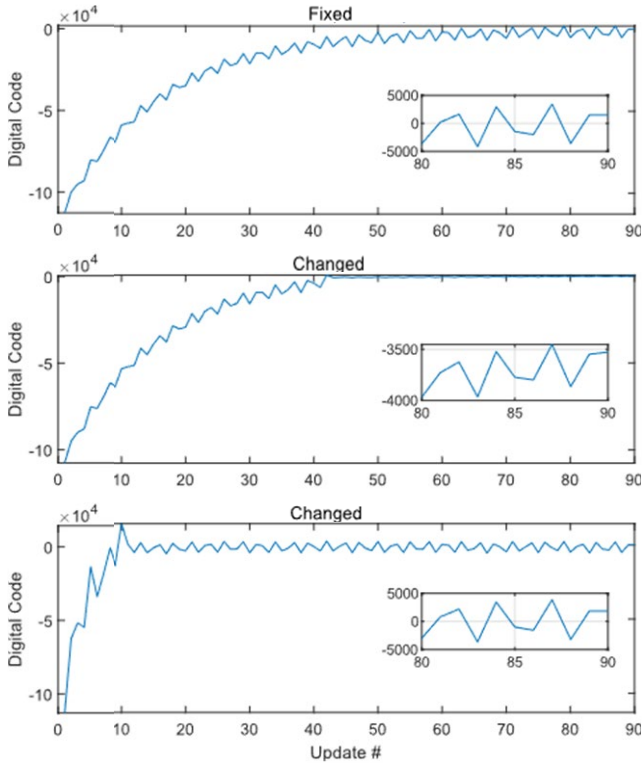

Fig. 4. The simulation result of the stimulation artifact rejection learning delay. The upper one fixes the weighting factor, the middle one changes the weighting factor in the range of the high accuracy mode, and the bottom one changes the weighting factor in the full range.

However, some abrupt changes occur only one time and if utilized in the template, could degenerate template quality. Therefore, the accuracy check module looks up the checking result history and changes weight only when the change shows a constant tendency. Since this adds a new updating delay, the overall simulation artifact rejection delay is less than 1s for 100Hz stimulation. It also prevents the module from exceeding the boundary conditions of each weighting factor.

The stimulator switch controls the highest current in the designed chip. Also, the stimulator output is directly connected to the outer environment. This leads to the need for high compliance voltage compared with the other chip components. Therefore, the stimulator is designed to handle a voltage range twice as large by using a separate power source. To control this high voltage stimulation system with a low voltage control system. The level shifter is needed to handle signals between the two systems (Fig. 5). The level shifter is composed of two stages: one for transitioning the high-level voltage of the input signal and the other for transitioning the low-level voltage of the input signal.

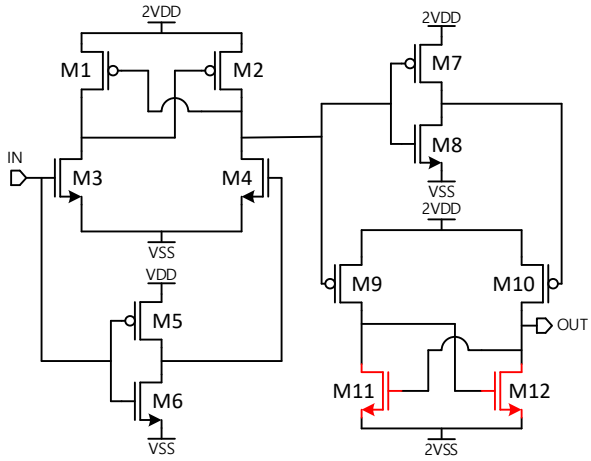

Fig. 5. Level shifter design. The first stage is for the transition of high-level voltage and the second stage is for transition of low-level voltage.
Red MOS denoted deep n-well MOS. The MOS sizes (W/L in μm) from M1 to M12 are 4/0.26, 4/0.26, 12.8/0.26, 12.8/0.26, 12/0.26, 12/0.26, 4/0.26, 4/0.26, 8/0.26, 8/0.26, 0.8/0.26, 0.8/0.26 respectively.

The stimulator controls the largest current among the chip blocks. The switch controlling the current path of the H-bridge stimulator needs to have as low a resistance as possible to prevent loss. "Therefore, the stimulator has larger switches compared to other components and requires a gate driver to control them properly. Fig. 6 shows the simulation data of the gate driver. Each stage is designed to have less than 1ns delay and an equal total delay for each path from the controller to the stimulator. If H-bridge switching is slow or has overlap due to a delay mismatch between PMOS and NMOS gate, the direct current path could be made.

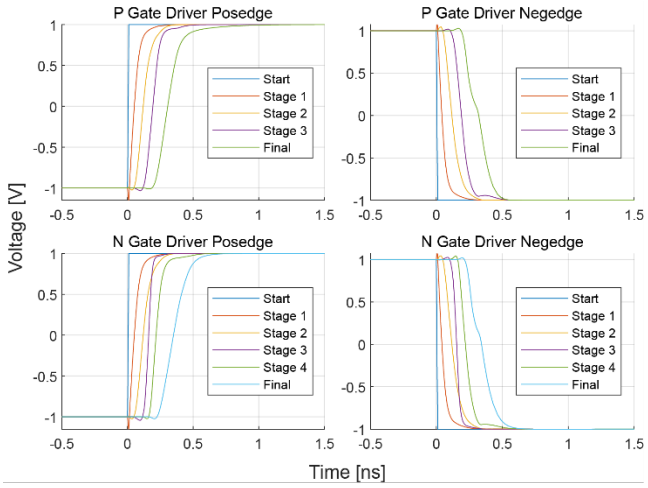

Fig. 6. Cadence simulation data for gate driver. Each path has less than 1ns transition delay and an equal total delay from input to output. Stage 1, 3 of P/N gate driver output, and final of N gate driver output is plotted inversely for easy comparison.

III. RESULTS AND DISCUSSIONS

Fig. 7 shows the test bench for electrical characteristics. A custom shielding box is used to prevent interference from the external noise sources. Power is supplied by an external power supply (Keysight, E36311A) and then regulated to the appropriate voltage by an LDO (Texas Instruments, LMH6624) on the PCB test board. Test signals are sourced by an external function generator (Teledyne, T3AFG120).

The chip′s input-referred noise is tested using a low-noise 1mVpp 316Hz sine wave signal (Fig. 8). The calculated noise is about 15 from 5Hz to 5kHz range which is enough to record bio-signal. This shows that the designed IC succeeds in recording ~mV range signal under that noise condition and is possible to record stimulation artifacts and bio-signals at the same time.

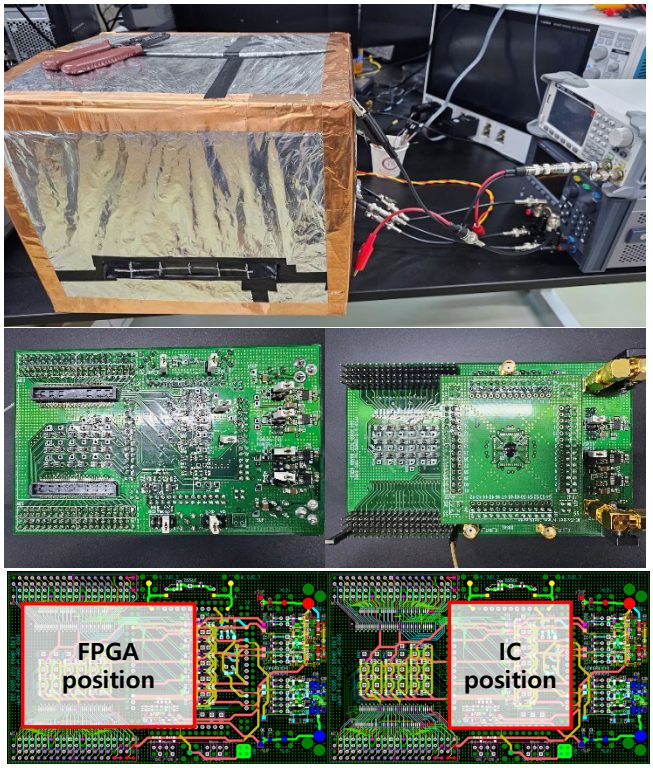

Fig. 7. The upper shows the overall test bench. A chipboard is placed inside the box to prevent interference from outer noise. Middle shows the PCB chip board. The left shows the FPGA connector part, and the right shows the IC connector part. Each part is on the opposite side of the one PCB. The bottom shows the PCB layout of the middle one.

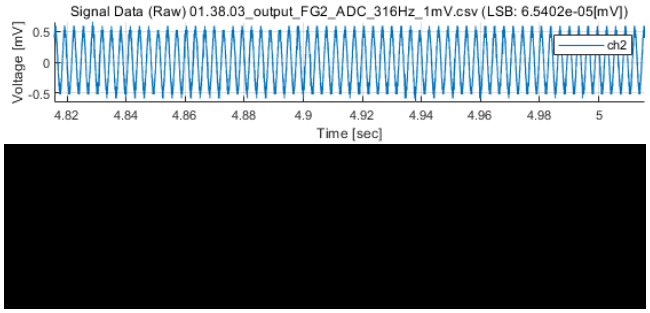

Fig. 8. Input referred noise test using 1mVpp 316Hz sine wave. The sine wave is generated by a function generator (Teledyne, T3AFG120). The calculated noise level is 14.84 from 5Hz to 5kHz range.

To test the SAR function fake stimulation artifact data is injected using the SPI module inside the chip. Fig. 9 shows that approximately -60dB of stimulation artifact power is reduced by about -120dB, achieving about 60dB rejection quality, while maintaining the recording data.

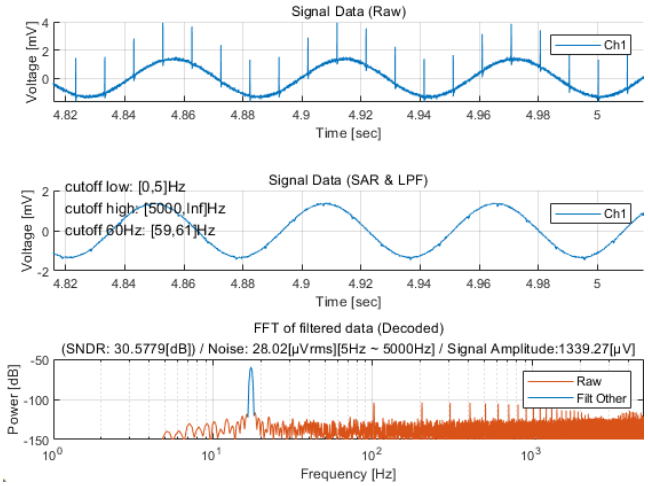

Fig. 9. The SAR function test uses fake stimulation artifact data. Signal data and artifact data are intended to have the same amplitude in the original data. SAR could reject about ~60dB of stimulation artifact while maintaining signal data.

To test the stimulator function generated stimulus signal is connected to 1kΩ registers (Fig. 10, Fig. 12) or 200Ω register and 220nF capacitor series (Fig. 11.). Figs. 10 and 11 show the stimulation length control test results. The signals are then recorded using an oscilloscope (Tektronix, Mixed Signal Oscilloscope 4 series). The stimulation signal is composed of three phases: one for the anodic phase, another for the interphase, and the last for the cathodic phase. The minimum length of each phase is 62.5 for 64kHz sampling and the interphase period is fixed at half of the others′ period.

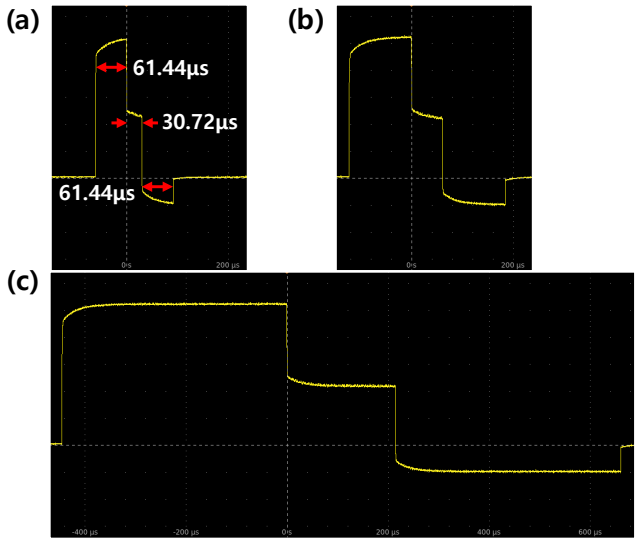

Fig. 10. Stimulation length control test. The minimum setting under the sampling rate of 65.104kHz is 61.44**μs**. (a) shows the minimum setting, (b) shows double, (c) shows seven times longer settings each.

While testing the sampling rate is set to 65.104kHz; therefore, the minimum period is 61.44. Fig. 10(a) shows the result when the setting is at the minimum period. Fig. 10(b) is set to double the minimum period, and Fig. 10(c) is set to seven times longer than the minimum period. The time scale in each figure is matched. It shows that stimulation length control operated as designed. Fig. 11 shows the same length settings as Fig. 10(a) and Fig. 10(b). A 1mA current flowing through the electrode-tissue modeling circuit (series R (200Ω) and C (220nF) made about a 200mV jump between phases and charging and discharging behavior during the anodic and cathodic phases.

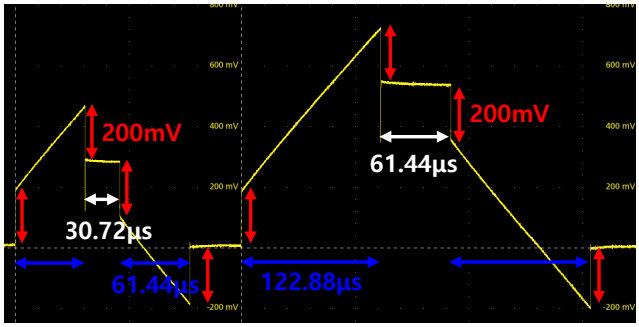

Fig. 11. The stimulation length control test with 200Ω and 220nF series. The left waveform shows the minimum length setting, and the right waveform shows double the length setting.

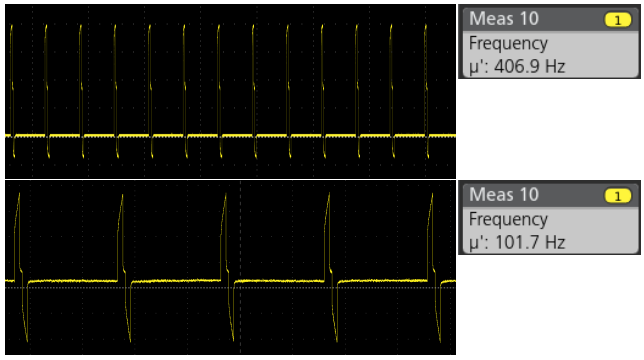

Fig. 12. The stimulation frequency control test. Upper shows setting of 400Hz, bottom shows setting of 100Hz.

TABLE I. Performance Comparison

Performance	This work	[13]	[14]
Process	65nm CMOS	65nm CMOS	Sub-µ CMOS
Supply voltage (V)	1 / 2	1.2 / 2.5	5.25
Artifact Suppression (dB)	60	60	100
Input referred noise (nV/√Hz)	296.8	126.9[2]	144.6
Artifact rejection delay	< 1s [1]	< 2s	-[3]

[1] At 100Hz stimulation frequency
[2] Calculated from table in [13]
[3] Conducted on external device

IV. CONCLUSION

In this circuit design, the overall system can show its ability to record bio-signal and stimulation artifacts simultaneously, to reject stimulation artifacts from recorded data while preventing distortion of the other signal in all frequency ranges, and to stimulate based on parameter setting. The 2nd-order DSM ADC-direct recording stage shows 15 from 5Hz to 5kHz frequency range which is enough to record various bio-signals like LFP (~500Hz signal band), and action potential (~ 5kHz signal band) when chopped. It can record the ~mV level of the signal in which the size of the stimulation artifact is positioned. The SAR module can reject about 60dB of stimulation artifact and the stimulator can produce a 100Hz to 400Hz range of stimulation which the current closed-loop neuromodulation system targeted. This design can be used to modulate neural systems in various areas.

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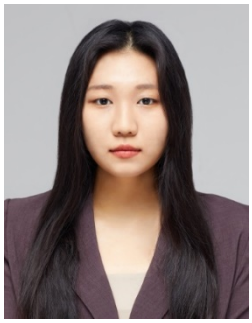

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