Performance Improvement Analysis of fNIRS IC

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***Abstract* – A Receiver (RX) for functional near-infrared spectroscopy (fNIRS) IC was previously designed to obtain hemodynamics of the human brain, requiring high SNR measurements. It is largely composed of TIA, PGA, and OTA-C-based matched filters, along with a single-slope ADC. However, a dead-zone problem arises in the conventional design, wherein an unstable voltage level appears in a specific section near 0V among signals measured using the IC system. This phenomenon persists despite offset calibration with its own current DAC, as each IC exhibits an inconsistent input offset value in the comparator. Revised IC is proposed to solve this problem.**

In this work, we address the issue by removing the current MSB detector and allocating a period for the ADC's comparator to verify the sign information of the PGA output. The dead-zone effect is mitigated by enhancing the system to provide discharge direction information and quantize it. Revised IC had a 0.48-bit ENOB enhancement in simulation domain, but failed to measure full scheme due to design-time issues.

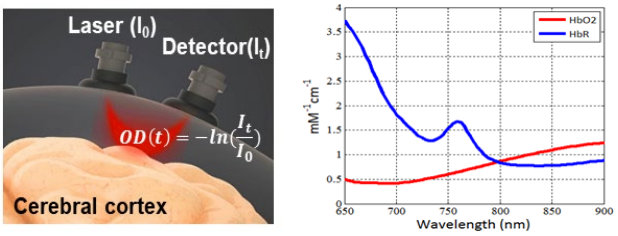
Keywords: Near-infrared spectroscopy, dead-zone, offset, comparator, charge extractor

I. INTRODUCTION

In an aging society, the number of people suffering from cerebrovascular or degenerative brain diseases such as stroke or Alzheimer's is rapidly increasing. Brain diseases progress slowly and recur frequently, necessitating continuous monitoring. However, devices such as fMRI or PET are expensive and not suitable for daily, continuous brain monitoring. Therefore, there is a need for a wearable brain monitoring system. Devices using functional near-infrared spectroscopy (fNIRS) ICs are highly portable compared to fMRI or PET.

fNIRS is a method of inversely estimating the concentration of oxy-hemoglobin and deoxy-hemoglobin in the bloodstream based on information about the intensity of light that is reduced when laser light arrives at a detector, using optical characteristics measured in the human body. This method is closely related to hemodynamics, which is the change in oxygen consumption of neurons and the concentration of oxy- and deoxy-hemoglobin in brain activity.

According to Fig. 1. (a), the intensity of light decreases exponentially, and the relative intensity of the incident light and the reflected light can be referred to as 'optical density (OD)' in a relational expression. Fig. 1. (b) can be applied to the equation of the Modified Beer-Lambert Law (MBLL) by utilizing the absorption coefficient information of chromophores, which varies depending on the wavelength. At least two equations are required to obtain the two chromophores, and the two wavelengths are selectively determined. The fNIRS IC selected wavelengths of 780nm and 850nm, which correspond to variations in the size of HbO2 and HbR around the 800nm wavelength, where absorption coefficients intersect. Since the main chromophores at the NIR (600nm~900nm) wavelength are HbO2 and HbR, HbR is large at 780nm and HbO2 is large at 850nm. Applying this information to MBLL can obtain the relative change in HbO2 and HbR for the time when light is incident and reflected. Through this, hemodynamic information can be determined.



(a) **(b)**

Fig.1 (a) Illustration of continuous-wave functional near-infrared spectroscopy (b) absorption coefficient spectra of chromophores

II. DESIGN METHODOLOGY

A. High SNR Measurement System of fNIRS IC

To observe brain activity, the source and the detector need to be approximately 4cm apart. However, due to the severe attenuation of light by the human head, which is 140 dB less than the nearest 4cm channel, the signal received is very weak. The fNIRS IC can achieve a high signal-to-noise ratio (SNR). It consists of a Transimpedance Amplifier (TIA) capable of increasing gain by 140 dB, a Programmable Gain Amplifier (PGA) that can further enhance gain by 66 dB, and an Operational Transconductance Amplifier (OTA) capable of adjusting gain by 8 dB (refer to Fig. 2).

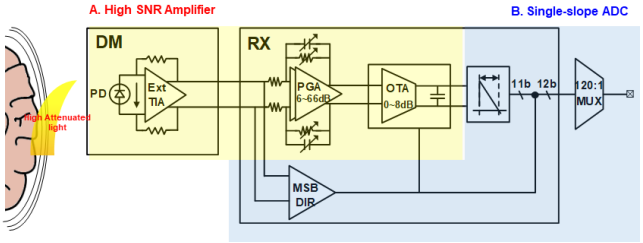


Fig. 2. Conventional fNIRS IC RX measurement unit

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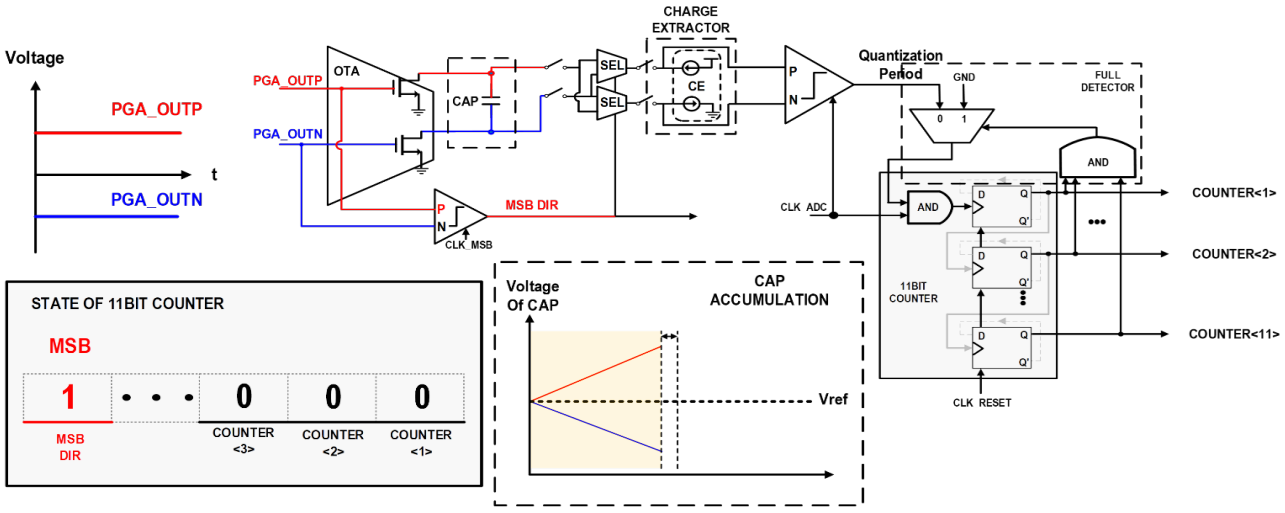


Fig. 3. Capacitor accumulation in Rx operation

The Rx (receiver) of the fNIRS IC converts the light intensity information received through the detector into voltage information using the Transimpedance Amplifier (TIA), and then amplifies it using the programmable gain amplifier (PGA). Subsequently, the process involves storing current information in the capacitor of the OTA-C based matched filter. This process is divided into two operations: quantization while discharging the charge stored in the capacitor for a certain period.

In Fig. 3, an example is illustrated where a value larger than that of PGA_OUTP is received. The charge accumulation operation proceeds with two paths: one where the OTA accumulates the differential voltage output of PGA in the capacitor for a certain period, and another path involving the comparator based Most Significant Bit (MSB) detector. This detector represents the output as P (1) or N (0) depending on the relative size between the two values. Since OUTP is larger than OUTN, it represents the output value of P. During this period, the 11-bit counter following the ADC does not operate.

When the capacitor is charged for a specific duration, the code information from the Most Significant Bit (MSB) detector is conveyed to the charge extractor. This information instructs the capacitor to discharge the charge in the opposite direction. The Analog-to-Digital Converter (ADC) quantifies the voltage of the capacitor from the start of discharge until it intersects the reference voltage, known as 'zero-crossing'. The quantization process entails incrementing the 11-bit counter by 1 each time the operation frequency is fed to the comparator following the capacitor while all values are zero. Once zero-crossing transpires, the value is no longer retained in the 11-bit counter, signaling the completion of the operation. The ADC generates the output result by multiplying the quantization period by the operation frequency (refer to Fig. 4). Furthermore, the primary source of noise affecting the Rx is thermal noise from the resistor in the TIA. Hence, it was designed with an OTA-C based matched filter structure.

N bits = Quantization period x CLK_ADC

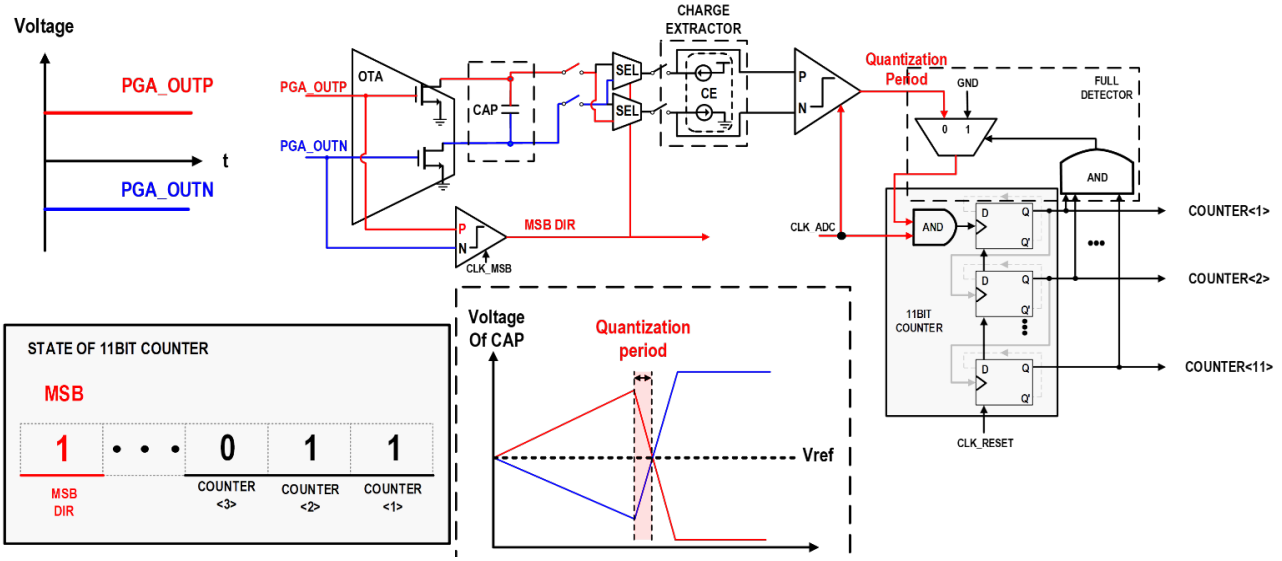


Fig. 4. Capacitor discharge in Rx operation

B. Signal Distortion in Dead-Zone

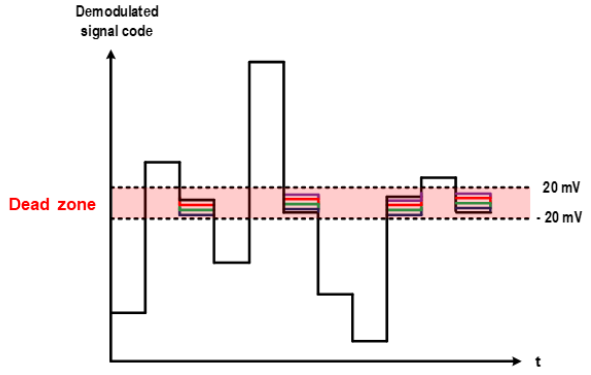


Fig. 5. Signal distortion in dead-zone.

A fundamental problem exists with the fNIRS IC as some signals measured by the IC become distorted. Through the fNIRS IC's transmitter (Tx), a known signal value is transmitted to the Rx, and the demodulation process results are depicted in Fig. 5. Signals within a specific range of -20 mV to 20 mV are not accurately measured, exhibiting unstable phenomena. This is attributed to the input offset voltage value of the comparator within the fNIRS IC, creating an unreliable section known as the dead-zone.

C. Comparator Shared Scheme for Dead-Zone Effect Minimization

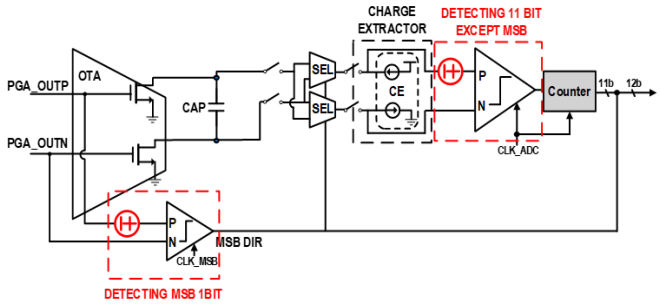


Fig. 6. Input offset voltage of two comparators in Rx.

The RX of the fNIRS IC incorporates a comparator for Most Significant Bit (MSB) tracking and another for 11-bit quantization with a charge extractor. Due to Process, Voltage, and Temperature (PVT) variations, an uncertain input offset voltage exists for each comparator. This uncertainty affects the MSB detection and the counting of Least Significant Bits (LSB) (refer to Fig. 6). Consequently, it becomes challenging to determine whether the MSB 1 bit of the output differential voltage of the quantified PGA and the remaining 11 bits are accurate 0s or 1s.

As a result, when sweeping the output voltage of the PGA, it remains unclear whether the measured values near 0V are positive or negative, defining this voltage interval as the dead-zone (refer to Fig. 7). One method to mitigate uncertainty involves utilizing a 6-bit current DAC to eliminate the input common mode voltage of each comparator. However, the offset voltage cannot be entirely eradicated due to the resolution limitations of each current DAC.

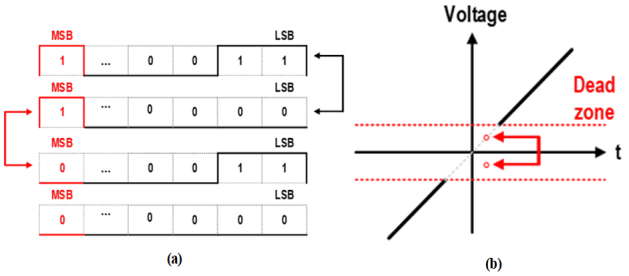


Fig. 7. (a) 12 bits of quantized differential voltage of PGA (b) Differential output voltage sweep of PGA

The uncertain input offset voltage of each comparator in the fabricated IC cannot be eliminated through fine-tuning. Therefore, to address this issue, it is necessary to reduce the number of comparators (refer to Fig. 8).

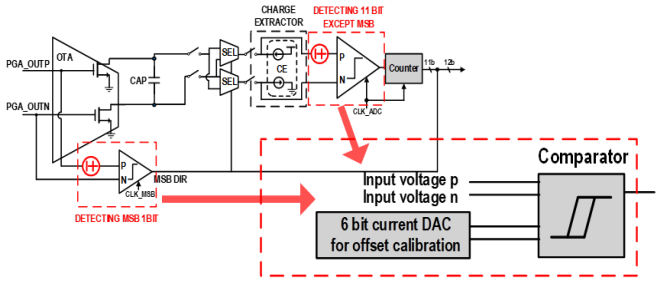


Fig. 8. Current DAC for offset calibration of two comparators.

To reduce the uncertainty of the MSB and LSB values, one block containing the comparator should be eliminated. Since the comparator following the charge extractor is crucial for quantization, the decision is made to remove the MSB detector.

Initially, the comparator following the charge extractor is activated, and the MSB signal information is outputted. This result is transmitted to the latch based MSB memory for storage. Subsequently, the switch is controlled based on the discharge direction information provided by the charge extractor. The 11-bit counter then operates, discharging the charge stored in the capacitor via the charge extractor, followed by the ADC performing the quantization operation (refer to Fig. 9).

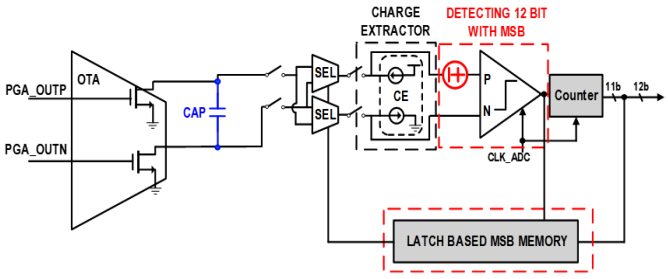


Fig. 9. Comparator sharing scheme for MSB detection in GM-C.

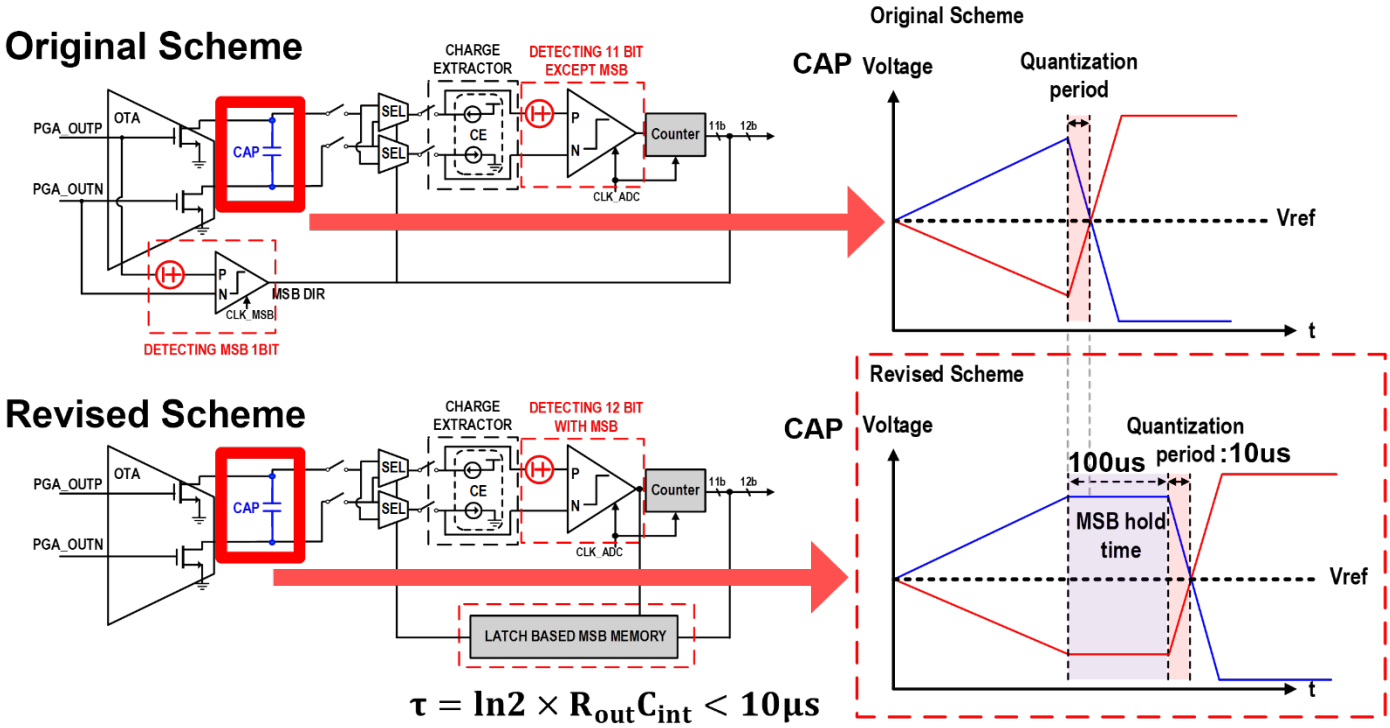


Fig. 10. Comparison of original scheme and revised scheme in Gm-C block.

The functionality of the original and revised schemes can be observed in Fig. 10. In the original setup, the charge is immediately discharged by the charge extractor after a certain period of capacitor charging. The path linked to the MSB detector communicates the discharge direction to the charge extractor. In contrast, the revised system lacks an MSB detector, thus no block exists to convey the discharge direction to the charge extractor.

To store the discharge direction in the latch based MSB memory, the minimum section required for the comparator preceding the existing counter to determine the MSB was designated as the MSB hold time. During this period, the differential voltage value of the 8pF MIM capacitor is maintained by keeping the charge open for a specific duration instead of discharging it [2]. Once the discharge direction information is stored in the MSB memory, the quantized information is stored in the capacitor like the original scheme. The MSB hold time is introduced, and the timing scheme is arbitrarily adjusted to approximately 100 us.

The input waveform and the waveform quantized by the revised IC are illustrated in Fig. 11. In the case of a properly functioning revised IC, it should quantize the input sine wave at the same frequency and amplify its amplitude to a specific value using the PGA. To minimize the impact of the dead-zone, the modified blocks were designed not to affect the operation of the existing IC, ensuring they perform the same operation.

However, during the actual verification of the IC on the test PCB, a pulse waveform with the same frequency as the input waveform was observed when the revised IC was operating incorrectly. These symptoms persisted even when the frequency and amplitude of the input sinusoidal wave were varied. When comparing the waveform output through the multiplexer with the quantized value of the IC, it was observed that all memories of the 11-bit counter were saturated. Consequently, it is currently not possible to assess the extent of the reduction in impact on the dead-zone in the revised IC.

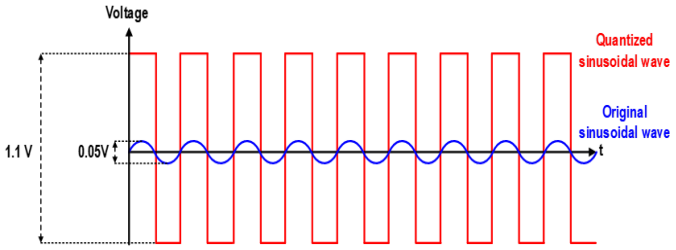


Fig. 11. Input and output waveforms of the revised IC.

D. Timing Scheme Modification of MSB Signal Hold Time

To diagnose the cause of the incorrect operation of the revised IC, verification using the PCB was halted, and the simulation results were re-evaluated. While the individual components of the revised IC, including the PGA, OTA-C based matched filter, and ADC, exhibited normal operation during simulation, discrepancies were noted when simulating the full block connecting all components. The output resembled the saturated waveform observed during PCB verification. The issue was identified by examining the differential output voltage of the PGA, the output waveform of the Gm-C block, and the quantized output value of the 11-bit counter.

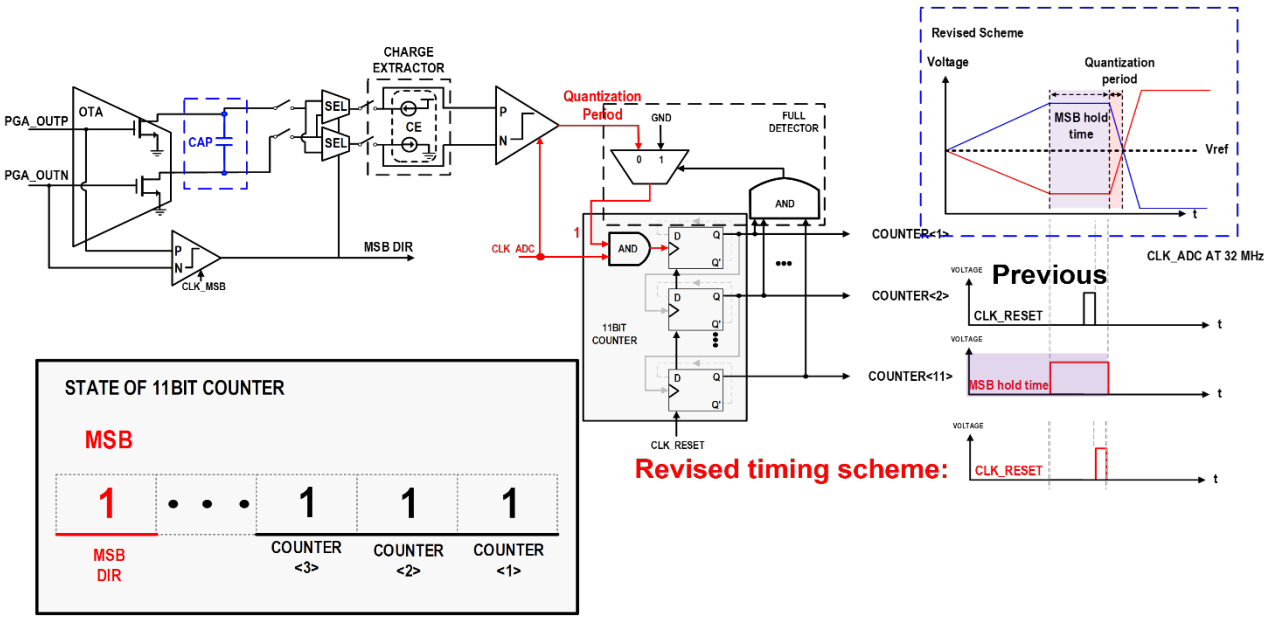


Fig. 12. Modified reset clock time scheme for 11-bit counter in Gm-C block.

The MSB hold time of the revised IC is intended as a period during which the charge of the capacitor is retained to ascertain the discharge direction of the charge extractor. During this interval, the comparator should not operate in count mode; rather, it serves solely to hold the directional information until it is stored in the MSB memory. However, it was observed that the comparator continued to operate at the operation frequency, leading to the count operation.

Consequently, the comparator's output was stored in the 11-bit counter without discharging the capacitor's charge, resulting in the 11-bit counter being saturated.

Two primary causes were identified for this phenomenon. Firstly, the MSB hold time setting was incorrect. The allocation of 100us for MSB detection time was not accurately configured. Secondly, the start time of the reset clock was erroneously set. This clock's initiation, crucial for storing quantized values in the 11-bit counter, was aligned with the original scheme, and not adjusted for the revised IC's 11-bit counter. The reset clock should have been initiated just before the charge extractor received MSB information to commence discharging and initiate the count operation. However, it was observed that the reset clock was initiated before the MSB hold time concluded, commencing earlier than the intended count operation start time, resulting in saturation of all memory within the 11-bit counter.

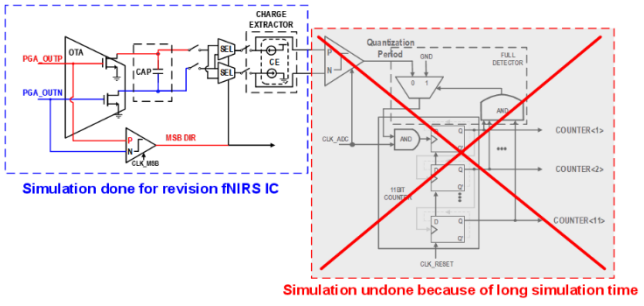


Fig. 13. Illustration of incorrect Gm-C operation of the revised IC

The cause of the incorrect operation of the revised IC is evident, as depicted in Fig. 13. The issue arises from the uncertainty surrounding the operation of the entire block, highlighted during the process of verifying the simulation results with the revamped scheme up to the front of the ADC. Notably, the frequency input to the comparator is set at 32 MHz, the highest value possible. Due to the time-consuming nature of simulating the process to check the result value of the 11-bit counter inclusive of this frequency, this step was omitted to expedite the confirmation process.

Consequently, it is deduced that the PCB test intended to ascertain whether the dead-zone impact had decreased was hindered by the inability to ascertain the accuracy of all timing schemes. Therefore, further attention is required to verify the accuracy of the timing schemes to properly evaluate the effectiveness of the revised IC in mitigating the dead-zone impact.

The block requiring improvement in the revised IC is the clock generator responsible for providing a reset clock to the 11-bit counter. This clock generator, which receives an external clock signal of 32 MHz, must be transformed into a digital block to ensure proper operation. Fig. 12 illustrates that the starting point of the reset clock has been delayed compared to the original scheme. Just before the MSB hold time concludes, the reset clock is injected to the 11-bit counter. Subsequently, the charge of the capacitor is discharged by the charge extractor, initiating the count operation (refer to Fig. 12).

E. Clock-Feedthrough Reduction in Comparator

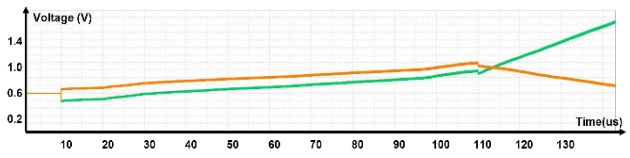


Fig. 14. Unstable capacitor voltage during MSB-hold time in Gm-C.

During the simulation process to confirm the operation of the revised IC, factors reducing the reliability of the result value were identified. Fig. 14 illustrates the output voltage of the capacitor during the MSB hold time. Notably, the output voltage of the capacitor does not remain constant but steadily increases, based on the reference voltage of 0.9V.

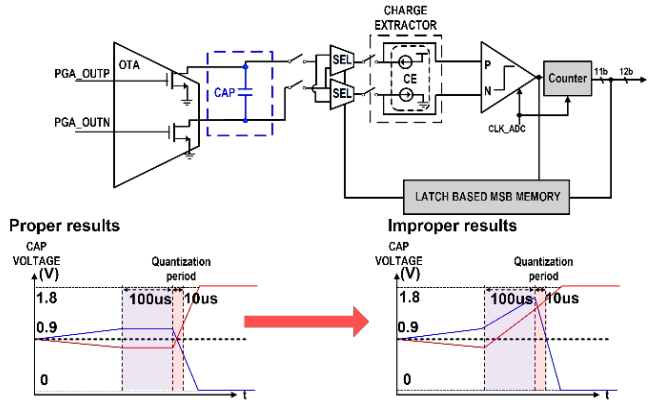


Fig. 15. Comparison of waveforms with and without ADC in Gm-C.

When the simulation is not checked with the entire block, the output voltage of the capacitor remains constant during the MSB hold time. However, abnormal increases occur in the simulation results of the entire block when the gain value of the Gm-C is changed to a switch, as depicted in Fig. 15. The key difference lies in whether the frequency of the comparator is input or not, indicating the importance of verifying the operation of the comparator.

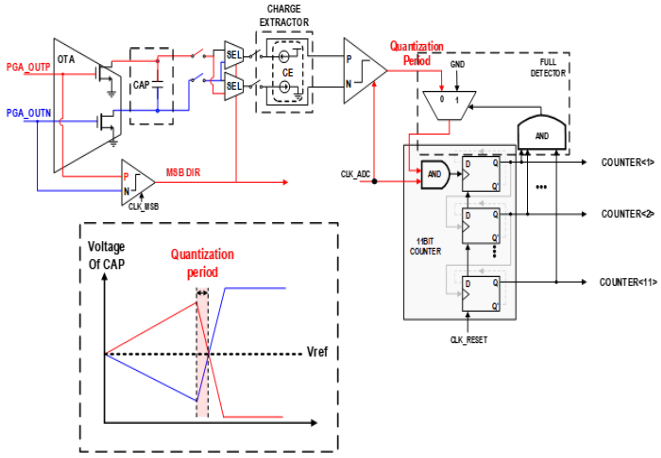


Fig. 16. Illustration in the original scheme in Gm-C.

The reason why it's impossible to detect symptoms of increasing capacitor voltage is because the charge extractor immediately discharges the capacitor after accumulating charge. Therefore, if the capacitor's charge isn't discharged, the symptom of increasing voltage cannot be identified. However, this doesn't affect the overall quantization operation and isn't considered a problem (refer to Fig. 16).

The increase in capacitor voltage is attributed to the operation of the comparator. For the comparator to function, there must be a Metal-Oxide-Semiconductor (MOS) where the clock is input. However, at the positive edge of the clock, there exists a parasitic capacitance which injects charge into other MOS devices unrelated to the clock. As a result, the capacitor voltage increases in addition to the charge from the capacitor connected to the output node of the previous block, OTA. This phenomenon is known as clock feedthrough and cannot be eliminated. To address this issue, dummy switches are added adjacent to clock switches placed in comparator (refer to Fig. 17).

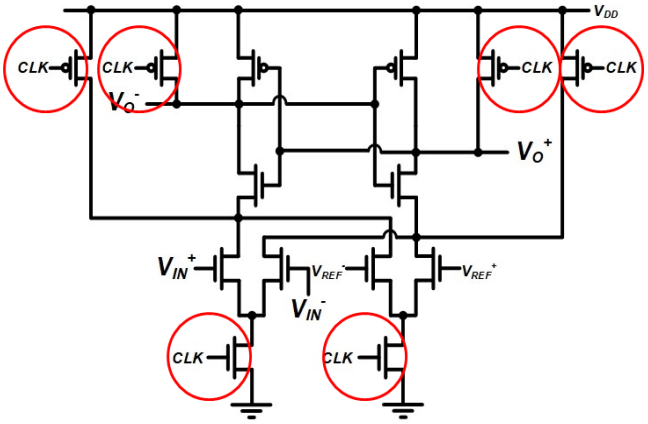


Fig. 17. Possible charge injection in CLK switches in comparator.

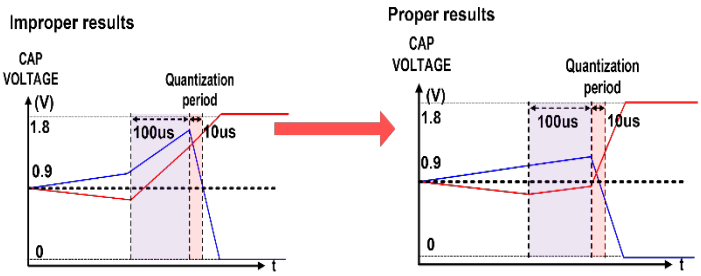


Fig. 18. Waveforms of revised scheme and final scheme.

Another approach is to halt the operation of the comparator during the MSB hold time. In both the original and revised schemes, the comparator receives a clock signal, leading to clock-feedthrough symptoms. While it's impossible to completely stop the comparator to track the MSB, this issue can be mitigated by modifying it to operate only for a portion of the MSB hold time. Therefore, by incorporating an additional dummy switch and adjusting the operation period of the comparator, it's possible to minimize the increase in capacitor voltage (refer to Fig. 18)

III. RESULTS AND DISCUSSIONS

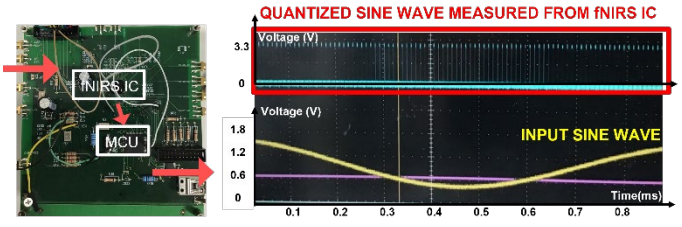


Fig. 19. Experimental setup and measurement result of revised IC.

The test chip was fabricated in TSMC 180nm process. In the simulation domain, the revised scheme showed 0.48-bit ENOB enhancement compared with the conventional scheme. Fig. 19resents the test PCB, system, and the resulting waveform for the verification of the revised IC. When a reference point of 0V and a sine wave are inputted, information from the Programmable Gain Amplifier (PGA) to the Analog-to-Digital Converter (ADC) of the fNIRS IC is quantized and outputted through the multiplexer. The 12-bit information, including the Most Significant Bit (MSB), is then conveyed to the Microcontroller Unit (MCU) and finally processed by communicating with an external PC via USB.

Through this process, the quantized value can be tracked to reconstruct frequency information and amplify amplitude information of the sine wave, which is the original waveform. On the PCB, this process is verified using a test pin to ensure the waveform outputs normally. However, as observed, any sine wave input appears to exhibit a saturated phenomenon.

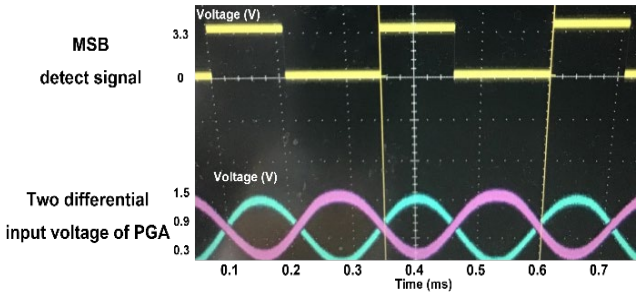


Fig. 20. Waveforms of two differential input voltage of PGA and MSB detecting operation of revised IC.

In Fig. 20 the results of measuring the MSB detect signal on the PCB are depicted to identify the problem with the revised IC. When compared to the two differential input line waves of the PGA, it's evident that the MSB is tracked normally. Therefore, it can be concluded that the MSB detection scheme is not the source of the problem.

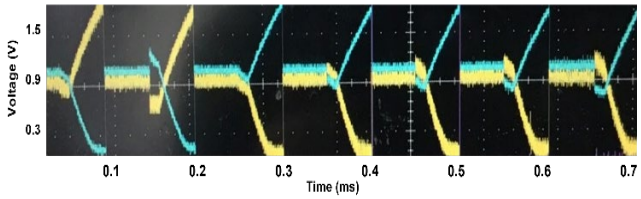
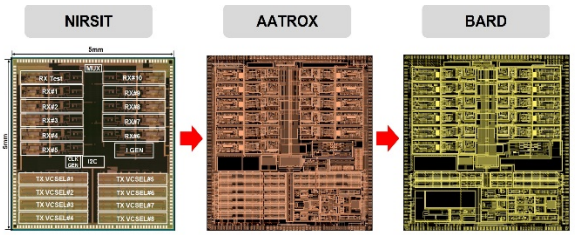


Fig. 21. Waveforms of capacitor during accumulation and discharge

The voltage of the capacitor was measured through a test pin (Fig. 21. The behavior of the charge extractor receiving MSB direction information and discharging is correct. However, the voltage of the capacitor must be kept constant during the MSB hold time, but it decreases. This can be seen as a problem with the PCB board itself along with the phenomenon caused by clock-feedthrough.

Table I outlines the project undertaken to identify and address each major issue found in the existing fNIRS IC [2] plagued by dead-zone problems

TABLE I. Tape-out History



Tape-out year	2015	2021	2023
Function	CWNIRS	CWNIRS + FDNIRS	CWNIRS + FDNIRS
Main Issue	Dead-zone	MSB hold timing	Unstable common-mode voltage

During the verification process, it was observed that several waveforms overlapped, and the amplitude appeared small when analyzing various MUX output waveforms with a test pin. No issues were detected in the schematic, making it challenging to identify the underlying problem. It was suspected that there might be an issue with the I/O pads that could not be discerned from the layout alone as depicted in Fig. 22. Additionally, due to the IC being molded onto the PCB, it was difficult to identify any problems visually. Consequently, an x-ray examination was conducted, revealing wires in contact with each other, and a lack of power supply to the digital I/O pad. The full x-ray image of the PCB for verification is depicted in Fig. 23.

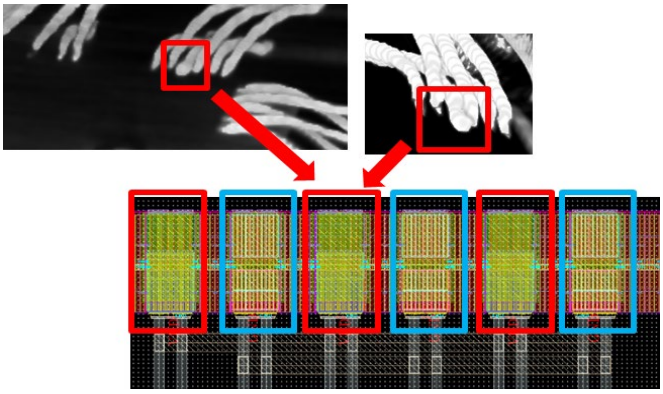


Fig. 22. X-ray image of wires and I/O pads layout

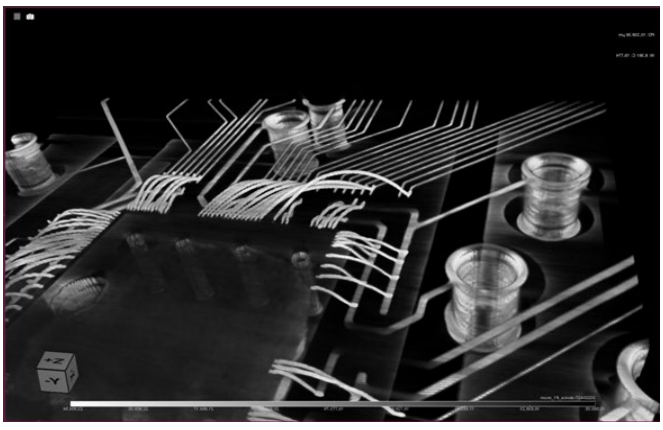


Fig. 23. X-ray image of test PCB

IV. CONCLUSIONS

To address the critical dead-zone problem inherent in ICs for fNIRS, which necessitate high SNR measurements, the MSB detection block between the two comparators was removed and replaced with a scheme utilizing a single comparator. To verify the reduction in the dead-zone's impact in the modified scheme, it was determined that the IC should be re-manufactured after identifying and resolving another issue discovered during the verification process via the PCB.

ACKNOWLEDGMENT

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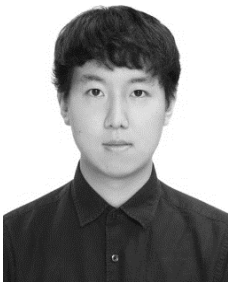

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