Beamforming Transmitter IC for Far-Field Wireless Charging

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Abstract **– This paper presents a wireless power transfer (WPT) system designed specifically for far-field charging scenarios, utilizing advanced beamforming technology. The system consists of a phase-shifting phase-locked loop (PLL) and a robust dual-band power amplifier (PA) capable of delivering high power with high efficiency. The PLL is engineered to synchronize with a reference clock frequency of 50 MHz and operates at frequencies of 5.8 GHz and 4.8 GHz, ideal for beamforming applications, particularly in the context of IoT devices. The PA architecture comprises two stages, integrating interstage and output baluns to optimize power matching. It directly amplifies the output from the 5.8 GHz PLL and boosts the 4.8 GHz PLL output by dividing it by two and then amplifying the resulting 2.4 GHz signal. This system is implemented using a 130-nm CMOS process, achieving VCO gains (KVCO) of 141.72 MHz/V and 83.5 MHz/V at 5.8 GHz and 4.8 GHz, respectively. Current consumption is measured at 281.4mA and 513.8mA at a 1.2V supply voltage for 5.8 GHz and 2.4 GHz, respectively. The PLL allows for a phase shift of 5.625° across the entire 360° range at frequencies of 5.8 GHz and 4.8 GHz, while the PA achieves output powers of 25.41dBm and 24.48dBm, respectively.**

Keywords— **Wireless Power Transfer(WPT), Beamforming, Phase-Locked Loop(PLL), Phase Shifting, Dual-Band Power Amplifier(PA), High Power, Balun Transformer**

I. INTRODUCTION

As the wireless charging market continues to grow, attention is shifting towards long-range wireless charging technology, which complements the existing short-range solutions. Short-distance wireless charging methods face challenges such as constraints imposed by wired charging and the complexities of magnetic resonance, limiting their ability to efficiently charge multiple devices simultaneously within a confined area.

In this paper, we introduce a beamforming transmitter integrated circuit (IC) designed to address the shortcomings of conventional slow beam scanning techniques and facilitate efficient beamforming. As shown in Fig. 1, beamforming is a signal processing technique

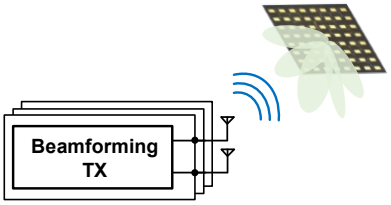

Fig. 1. Beamforming TX application.

used in communications and radar systems to focus transmitted or received signals in specific directions. Our aim is to develop a high-power transmitter featuring a beamforming architecture that can effectively transmit energy while providing flexibility in power adjustment.

The structure proposed in this study offers enhanced flexibility in phase shifting for phase-locked loops (PLLs). Unlike conventional PLL designs, our approach integrates phase-shifting capabilities directly within the PLL, eliminating the need for additional phase shift components. The operational process is streamlined: two phase frequency detectors (PFDs) receive divider output signals with consistent delay intervals as inputs. The phase shift is then controlled by the charge pump (CP) current, which is supplied based on the delayed signal received by the PFD. This precise control of CP current allows for desired phase shifts without the need for extra components.

Following the PLL, the dual-band power amplifier (PA) amplifies the output from the voltage-controlled oscillator (VCO) and transmits it to the antenna for full amplification. Our proposed PA structure for 2.4GHz and 5.8GHz employs interstage and output balun transformers to achieve efficient power matching and enhance output power at the antenna.

II. PROPOSED STRUCTURE

A. TX Top Block Diagram

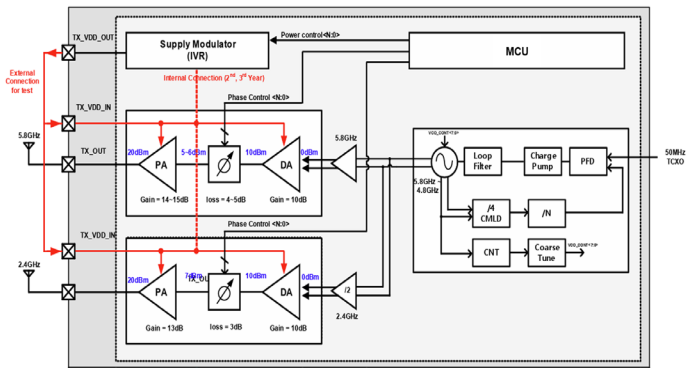

Fig. 2. Top Block Diagram of Proposed Beamforming TX.

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Fig. 2 shows the top-level block diagram of the beamforming transmitter. This transmitter emits signals with controlled phase shifting to precisely locate the receiver. Upon the initial signal emission, it continuously transmits until it receives an acknowledgment (ACK) signal from the receiver. The phase-locked loop (PLL) is engineered with a resolution of 5.6 degrees per bit and a 64-bit control scheme, ensuring coverage of the full 360-degree range.

B. PLL Top Block Diagram

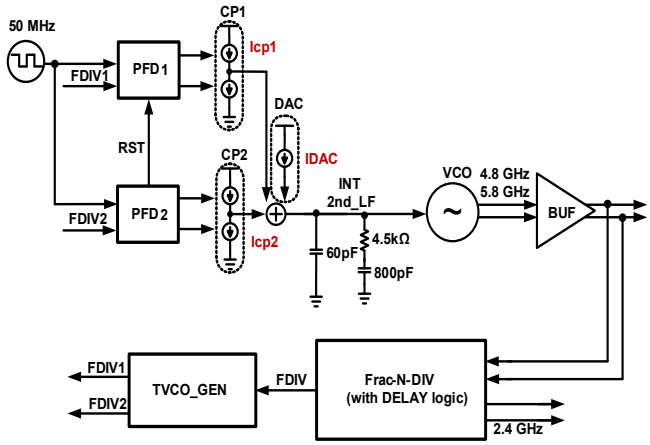

Fig. 3. Top Block Diagram of the Proposed PLL.

Fig. 3 shows the top block diagram of the proposed structure of the PLL. Incorporating phase-shift capabilities into the PLL setup uses integrating an extra phase frequency detector (PFD), an additional charge pump (CP), and another TVCO_GEN cell. The TVCO_GEN cell consist of a logic gate capable of generating two signals with a consistent delay equivalent to the period of the VCO output (TVCO).

The PLL, as shown in this paper, functions with a 50 MHz reference clock and aims at frequencies of 5.8 GHz and 4.8 GHz. PFD1 and PFD2 share a common structure, with PFD2 supplying a reset (RST) signal to PFD1. CP1 accepts the generated signal and acts as input for CP2. The combined charge pump current, comprising CP1's current (Icp1) and CP2's current (Icp2), is set at 320uA. The loop filter (LF) is furnished with a DC current for phase adjustment, ensuring stability in the locked state. As the PLL operates in integers, a secondary LF configuration is considered adequate. LF parameters entail a C1 value of 60 pF, a C2 value of 800 pF, and an R2 value of 6 kΩ for 5.8 GHz operation. This LF setup yields a bandwidth of 309 kHz and a phase margin of 48.92 degrees for 5.8 GHz, and a bandwidth of 197 kHz and a phase margin of 56.42 degrees for 4.8 GHz.

The Fractional-N Divider is achieved through a divider chain comprising a current-mode logic (CML) divider, a true-single-phase-clock (TSPC) divider, and a programmable divider dividing the VCO output signal by 116.

C. Principle of Phase Shifting

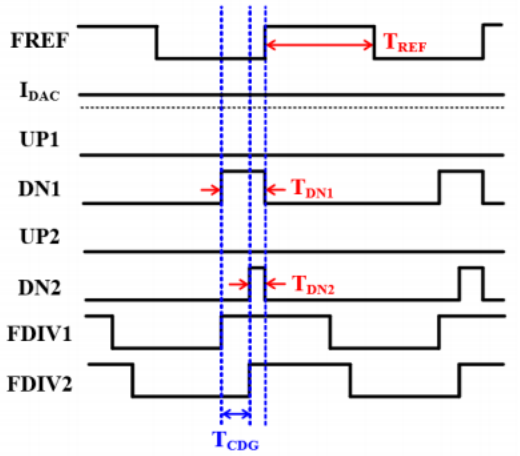

Fig. 4. Timing Diagram of the Phase-Shifting PLL.

$$T_{REF} \times I_{DAC} = T_{DN1} \times I_{CP1} + T_{DN2} \times I_{CP2} \quad (1)$$

$$T_{DN1} \times I_{DN1} = T_{DN2} \times I_{DN2} \quad (2)$$

$$I_{CP} = I_{CP1} + I_{CP2} \quad (3)$$

Fig. 4 shows the timing diagram of the phase shift-PLL in its locked state, indicating the process of phase shifting. When the PLL is locked, the total charge entering the loop filter (LF) must be balanced, maintaining an equilibrium of zero. This equilibrium is mathematically described by the following equation:

"TREF" refers to a single cycle of the reference clock, while "IDAC" represents the DAC current responsible for generating solely the Down (DN) signal from the PLL. "TDN1" denotes the duration of the DN signal from CP1, "ICP1" represents the current of CP1, "TDN2" corresponds to the duration of the DN signal from CP2, "ICP2" represents the current of CP2, and "ICP" denotes the reference current of CP. Let's define "TVCO" as the difference between TDN1 and TDN2, which signifies the disparity between FDIV1 and FDIV2, thereby indicating the variation between TDN1 and TDN2.

$$T_{VCO} = T_{DN1} - T_{DN2} \quad (4)$$

Substituting equations (2), (3), and (4) into equation (1), we get:

$$T_{DN1} = \frac{I_{DAC} \times T_{REF}}{I_{CP}} + \frac{I_{CP2} \times T_{VCO}}{I_{CP}} \quad (5)$$

Given that the initial term in equation (5) remains consistent throughout the phase shift, we can define the time resolution ($T_{Resolution}$) of the shift as follows:

$$T_{Resolution} = \frac{I_{CP2}}{I_{CP}} \times T_{VCO} \quad (6)$$

To attain a high-resolution phase shift, characterized by a low $T_{Resolution}$, minimizing T_{VCO} and controlling CP current bits precisely is essential.[2]

D. LC Voltage-Controlled Oscillator(LCVCO)

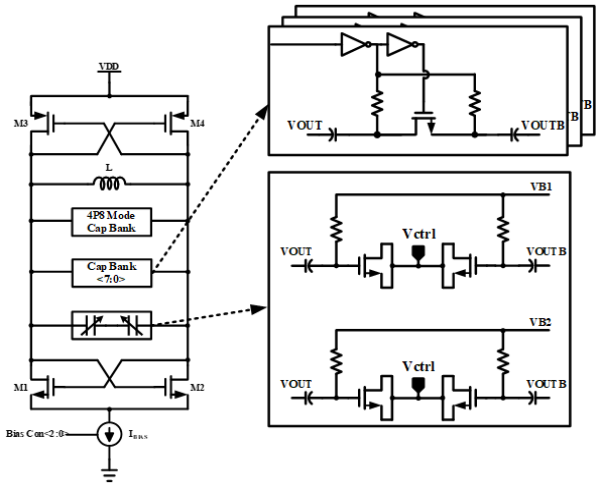

Fig. 5. Schematic of LCVCO.

Fig. 5 shows the designed voltage-controlled oscillator (VCO), which employs the fundamental LCVCO structure. By using the linear section of the varactor capacitance, the bias voltage is set at the terminal varactor node on the VCO output side using four varactors. Additionally, it integrates a discrete capacitor bank controlled through digital bits to effectively increase the total capacitance. To ensure coverage of the frequency range up to 5.8 GHz despite process, voltage, and temperature (PVT) variations, a capacitor bank is devised, necessitating the addition of one digital bit and one capacitor bank.

E. Charge Pump with IDAC Cell Attachment

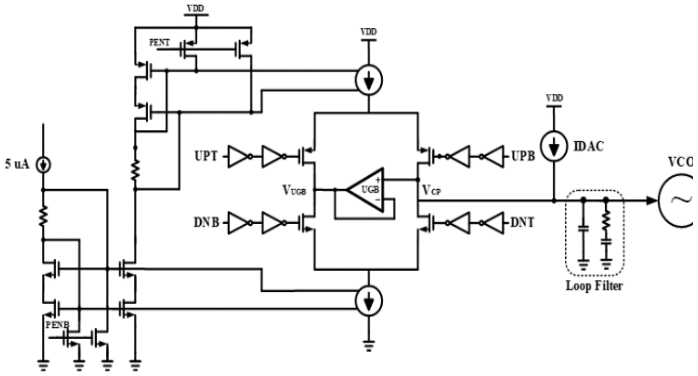

Fig. 6. Schematic of Charge Pump with IDAC Cell.

The PLL employs two identical charge pumps, each designed according to the configuration depicted in Fig. 6. Each charge pump incorporates a switch utilizing a current mirror and a unity-gain buffer (UGB), with a bias current of 5uA supplied to the current mirror. The UGB ensures constant voltages at the V_{CP} and V_{UGB} nodes, minimizing current discrepancies.

IDAC cells are integrated to generate exclusively DN signals after the PLL is locked. These cells are configured using the current mirror cell, with 3 control bits allocated for adjustment.

F. Frequency Divider with TVCO GEN cell

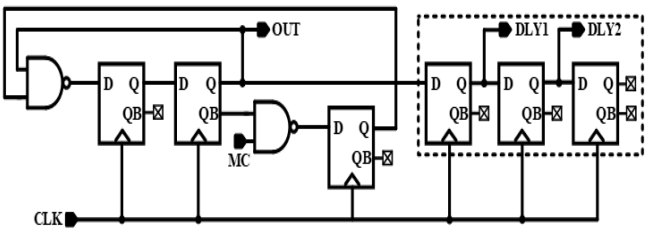

Fig. 7. Schematic of Dual-Modulus Divider.

Fig. 7 shows a schematic diagram demonstrating a dual-modulus divider configuration. Initially, three D flip-flops are linked to the output of the dual-modulus divider. The CLK signal, driving these flip-flops, originates from the VCO output signal, specifically the frequency of the TVCO signal. Consequently, the time delay between the DLY1 and DLY2 signals equals TVCO. Ensuring that the setup time and hold time of the D flip-flop generating the DLY2 signal are satisfied ensures a consistent time interval with the DLY1 signal. The final D flip-flop serves as a load to synchronize the initiation time of the DLY1 and DLY2 signals.

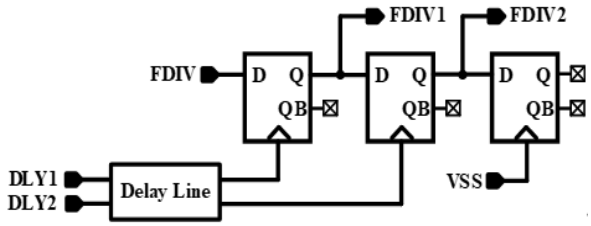

Fig. 8. Schematic of T_{VCO} Generator.

DLY2 signals is equivalent to TVCO.[5] Ensuring that the setup time and hold time of the D flip-flop generating the DLY2 signal are met guarantees a constant time interval with the DLY1 signal. The final D flip-flop acts as a load to synchronize the initiation time of the DLY1 and DLY2 signals.[6]

Subsequently, by incorporating the TVCO GEN cell depicted in Figure 8, we introduce phase-shifting capabilities into this PLL. This cell is engineered to produce two signals, FDIV1 and FDIV2, with a fourfold delay difference compared to the TVCO, while maintaining the same waveform as the FDIV signal. To accomplish this, two input signals, DLY1 and DLY2, are utilized with a fourfold delay difference for a D flip-flop clock.[7]

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G. PA (Power Amplifier)

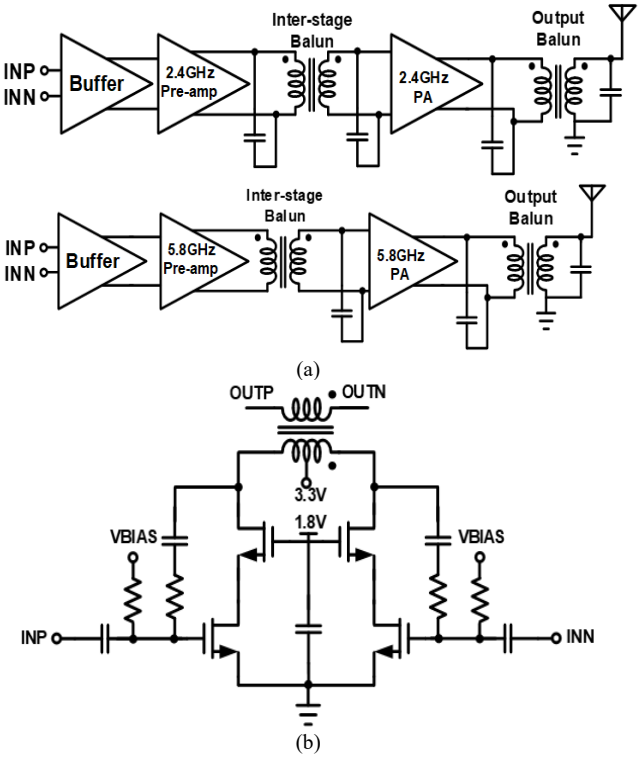


Fig. 9. (a) 2.4GHz/5.8GHz Dual-Band PA Top Diagram (b) Schemetic of Pre-Amp and PA Core.

Fig. 9 shows a dual-band power amplifier operating at 2.4 GHz and 5.8 GHz, designed to transmit output power from a transmitter to an antenna. To achieve a robust output power of 20 dBm or higher, a 2-stage PA structure is employed in the circuit implementation. The Multi-Stage design is structured in a Cascade arrangement to maximize gain. High linearity and gain are achieved through the utilization of a differential cascode structure. This configuration, employs a differential cascode amplifier to efficiently amplify the output signal while suppressing common-mode signals, thereby minimizing power loss. The amplifier is engineered to operate seamlessly at both 5.8 GHz and 2.4 GHz frequencies, with the aim of delivering an output power exceeding 20 dBm, enabling effective beam formation at distances exceeding 2 meters.

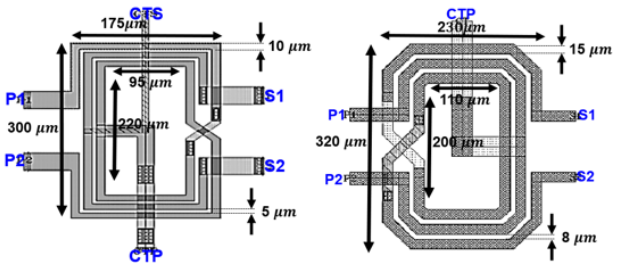


Fig. 10. 2.4GHz/5.8GHz Balun Transformer in PA Design (a) Interstage Balun (b) Output Balun.

The transformation process is facilitated by employing dual-center tapped balun Transformers, which are equipped with high Q inductors. These transformers are strategically positioned to ensure efficient signal transfer with minimal power losses between stages and to deliver the differential signal to the output antenna as a unified signal. Both the interstage balun and output balun, essential components located between the amplifiers at the output stage, are illustrated in Fig. 10 (a) and Fig. 10 (b), respectively, both featuring a spiral structure.

Spiral baluns, known for their compact size, especially when integrated into circuits, are selected for their excellent common-mode noise suppression capabilities. This feature makes them well-suited for integration within this power amplifier design, functioning as a differential amplifier, effectively suppressing common-mode noise and facilitating high-quality signal transmission.

The adjustment of each balun's parameters to achieve optimal performance was determined through impedance matching using load-pull tests. These tests are validated based on power matching criteria, ensuring high output power exceeding 20 dBm. Notably, each primary center tap (CTP) within the baluns serves as a conduit for supplying a 3.3V supply voltage to both the Pre-amp and PA. Additionally, the secondary center tap (CTS) in the interstage balun functions as a pathway for supplying bias voltage to the PA. The parallel capacitors in front of and behind the 2.4 GHz PA and the 5.8 GHz PA shown in Fig. 9 (a) ensure that the PA appears to have the optimal impedance, which is a compromise between the top of the power contour and the top of the power added efficiency(PAE) contour, when impedance matching is performed through load-pull testing and SP simulation, respectively. The balun transformer alone does not perfectly approach the optimal impedance on Smith chart, but by adding a shunt capacitor, it shifts the impedance point enough to move it towards the optimal impedance calculated by the load pull test.

III. Results and Discussion

A. Simulation Results

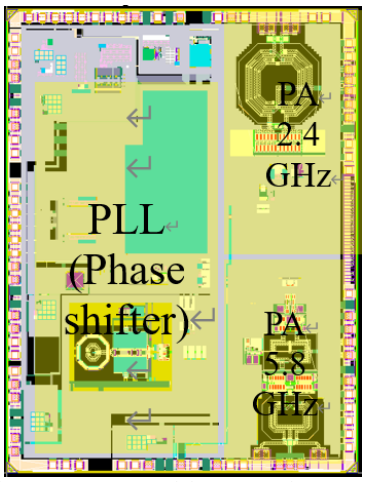


Fig. 11. Top Layout of the Proposed System.

Fig. 11 shows the layout of the proposed top PLL design, realized using a 130nm CMOS process. The layout occupies a total area of 2.63mm * 4mm.

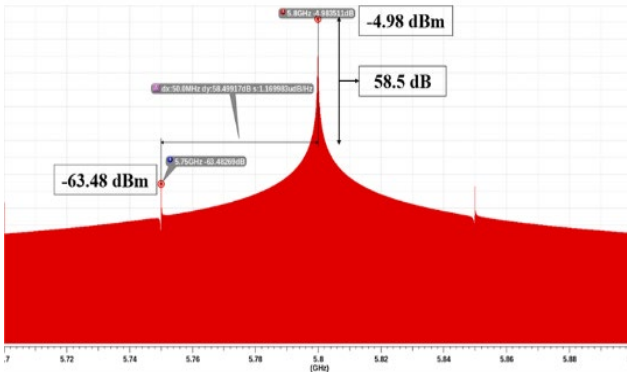


Fig. 12. FFT Simulation Results

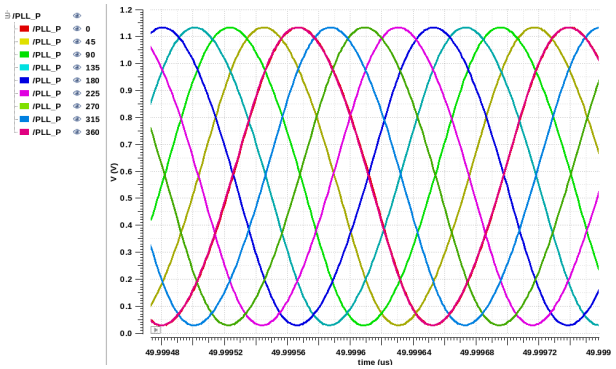
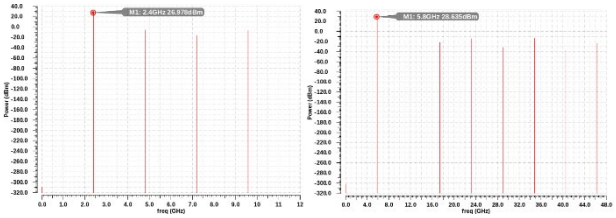


Fig. 13. Shifted Phase of the PLL Output.

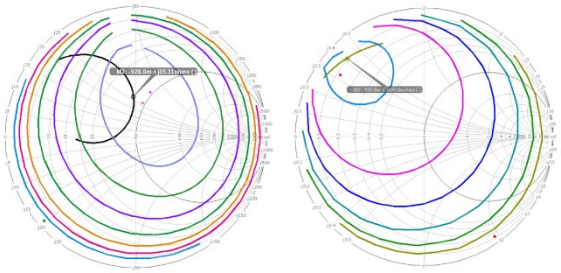
In Fig. 12, the outcomes of the fast Fourier transform (FFT) simulation performed on the proposed PLL Top are presented. The PLL achieves lock-in at 5.8GHz with a power level of -4.98dBm. The power difference between the target tone and the reference spur is measured at 58.5dB.

Fig. 13 showcases the simulation results of the phase shift PLL, conducted with phase shift of 45 degrees.



(a) (b)

Fig. 14. Harmonic Balance Simulation Results of (a) 2.4GHz (b) 5.8GHz PA.



(a) (b)

Fig. 15. Load-pull Power Contour of (a) 2.4GHz (b) 5.8GHz PA.

In Fig. 14, the designed power amplifier's output power is illustrated in the frequency domain through harmonic balance simulation, we begin with a reference input power of 5 dBm, yielding 26.98 dBm / 28.64 dBm at the fundamental frequency of 2.4 GHz / 5.8 GHz, respectively.

Fig. 15 illustrates the load pull simulation employed during the PA design phase. The objective is to align the peak of the power contour on the Smith chart, ensuring that the practical load impedance point at 2.4 GHz (or 5.8 GHz) was closely matched. This design approach was chosen to achieve both high output power and high power added efficiency (PAE). When calculating PAE with the Tx power from the simulation, 2.4GHz PA had a PAE of 48.51% and 5.8GHz PA had a PAE of 42.47%.

B. Measurement Results

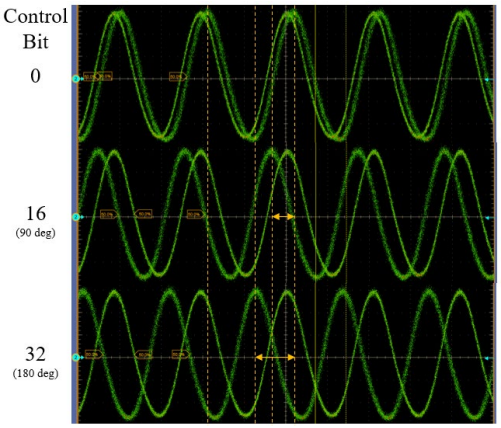
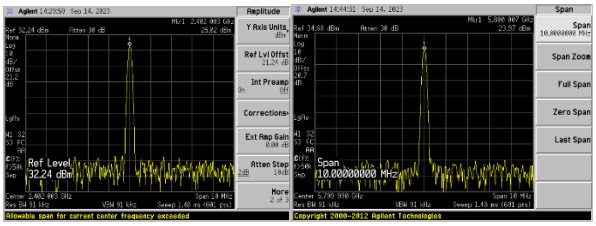


Fig. 16. Measurement of Phase Shifting PLL.

Fig. 16 shows the measurement waveforms of phase shifting PLL. Two Tx chips are measured simultaneously with high-speed oscilloscope. When the control bit is equal to zero, there is some phase offset between two output waveforms. And then, each increment of 16 control bits results in a 90 degree phase shift.

Fig. 17 showcases the measurement results of the Tx output power from the dual-band PA when the input power of the PA is 5 dBm from the PLL VCO output. At 2.4 GHz, it demonstrates an AC output power of 25.31 dBm. At 5.8 GHz, it exhibits 24.48 dBm. When calculating the PAE from the measured data, it was found that the 2.4 GHz PA exhibited a PAE of 32.66%, whereas the 5.8 GHz PA demonstrated a PAE of 16.10%. Measurement results include the cable loss and the loss of the external balun for measurement.



(a) (b)

Fig. 17. Measurement of Tx Output Power (a) 2.4GHz (b) 5.8GHz PA.

TABLE I. Design Implementation Summary

Parameter	Value
Operating Frequency	2.4GHz, 5.8GHz
Output Power	25.31dBm, 24.48dBm
Phase Shifting Resolution	5.625°
Reference Frequency	50MHz
Current Consumption	311mA / 521mA
Process	130 nm CMOS
Area	2.63 mm × 4 mm

TABLE I summarizes the characteristics of the designed circuit. The Tx is designed with 130 nm CMOS process, and the layout size is 2.63 mm × 4 mm.

IV. CONCLUSIONS

This paper introduces a wireless power transfer (WPT) system designed for far-field charging applications in IoT contexts. The system features a self-phase-shifting phase-locked loop (PLL) and a dual-band power amplifier (PA), showcasing remarkable adaptability.

The PLL within this system is capable of phase shifting by 5.625 degrees across a full 360-degree range. Complementing this, the dual-band power amplifier delivers 25.31 dBm at 2.4 GHz and 24.48 dBm at 5.8 GHz, providing substantial power output. Moreover, the current consumption of this setup is recorded at 311mA / 521 mA at the fundamental frequencies of 2.4 GHz / 5.8 GHz respectively.

Furthermore, employing this system allows for heightened efficiency, resulting in minimized power loss and interference, particularly beneficial in wireless power transfer (WPT) and beamforming applications.

ACKNOWLEDGMENT

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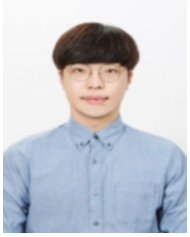

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