An 8G Hz SST Transmitter with Adjustable FIR and Pre-Emphasis Logic in 65nm CMOS

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***Abstract* – In response to the escalating demands for high-speed communication and the necessity for effective channel loss compensation, this study introduces an advanced transmitter (TX) system with enhanced adaptability. This system integrates a sophisticated TX architecture, augmented by a pre-emphasis logic, and a three-tap Finite Impulse Response (FIR) filter, using TSMC's 65nm process technology. The core of the pre-emphasis architecture is a Voltage-Mode Driver topology, serving both as the primary driver and emphasis cell, supplemented by an additional logic to modulate the FIR's first tap. This modulation facilitates varied emphasis states, enabling tailored compensation for diverse channel losses. The FIR, realized through Current-Mode Logic (CML), optimizes power efficiency, while the driver configuration, composed of Source Series Termination (SST) drivers, ensures a robust output swing. Incorporating SST drivers' ushers in a hybrid impedance control approach, merging conventional analog-loop control with impedance regulation via the SST driver slices. Simulation results show that the system achieves speeds of up to 8GHz and an output swing of 1.2V while maintaining an eye width of 0.8 Unit Intervals (UI).**

***Keywords*—Pre-emphasis system, Adjustable, Impedance Control, Finite Impulse Filter (FIR), TX**

I. INTRODUCTION

In recent years, advancements in communications, big data analytics, and machine learning have significantly escalated the demand for high-speed, low-power data transmission solutions. Conventional transmitter (TX) architectures often face limitations in accommodating high-speed data inputs while maintaining power efficiency. Furthermore, existing equalization technologies for TX systems predominantly rely on complex architectures, thereby increasing both system complexity and power consumption. (Fig. 1)

In high-speed digital communication systems, channel bandwidth limitations and attenuation often result in degraded signal quality at the receiver end. To address this challenge, designers commonly employ pre-emphasis techniques to improve the quality of the transmitted signal. However, fixed pre-emphasis solutions frequently fall short in adapting to varying channel conditions and data rates, thereby impacting system performance.

To solve this problem, there is a need for a flexible, low-power, and easily accessible pre-emphasis solution. Moreover, as data rates continue to escalate to 8 Gbps or beyond, traditional pre-emphasis approaches may become unsuitable or result in excessive power consumption and complexity.

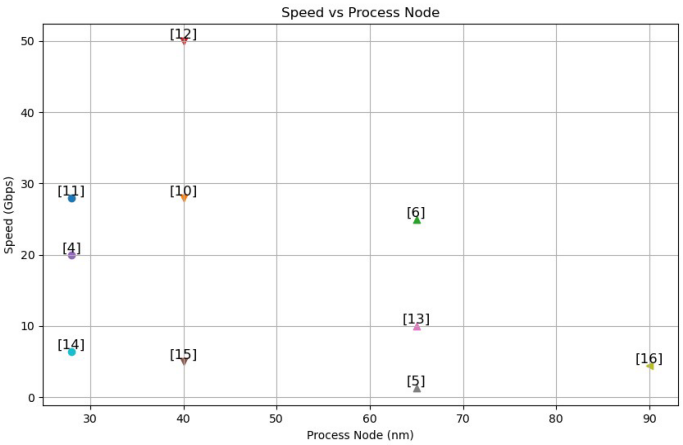

Fig. 1. Past technique process (Ref [4, 5, 6, 10, 11, 12, 13, 14, 15, 16]) compared with input speed.

Table I proposes a comparison between the design requirements specified in LPDDR4 [1] and LPDDR5 [2] technical files and this work design requirement. In LPDDR4, the maximum data rate is 4.2Gb/s with a power supply of 1.1V. In contrast, LPDDR5's maximum data rate reaches 6.4Gb/s and requests a higher power supply voltage of 1.8V. With the increase in data rates, there is a higher demand for power supply as well as a higher signal quality requirement. Signal quality can be reflected in the eye diagram open width and height. For eye opening height, a trend from 0.55V(LPDDR4) to 0.72V(LPDDR5). While the eye-opening width is from 0.45UI to 0.75UI which reflects the demand for time. Consequently, this work design target has been settled as a maximum data rate of 8 Gb/s for the future possible demand in LPDDR5 and power supply has been settled as 1.8 V for enough power

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efficiency. At the same time, eye diagram open width and height have been settled as 1.2V and 0.8 UI which can give a margin for future improvements in technology.

TABLE I. Design Requirement of LPDDR4, LPDDR5 and this work

	LPDDR4	LPDDR5	This work
Maximum data rates (Mb/s)	4200	6400	8000
Power supply(V)	1.1	1.8	1.8
Eye opening height(minimum)(V)	0.55	0.72	1.2
Eye opening width (UI)	0.45	0.75	0.8
Time jitter(maximum)(UI)	N/A	0.017	0.017

Against this backdrop, we introduce an innovative pre-emphasis method named 'Emphasis-Logic,' which allows for dynamic and adaptive adjustment of pre-emphasis levels. This approach employs an adjustable transmitter (TX) architecture and features an output swing of 1.2V and an input data rate of 8 GHz. Through the incorporation of Emphasis-Logic, this design can be applied based on various channel conditions and requirements. The proposed TX system diagram is shown in Fig.2. The TX system is made up of 2 differential input paths, each path has an 8 to 1 MUX, a pre-driver, main driver, impedance control and FIR logic.

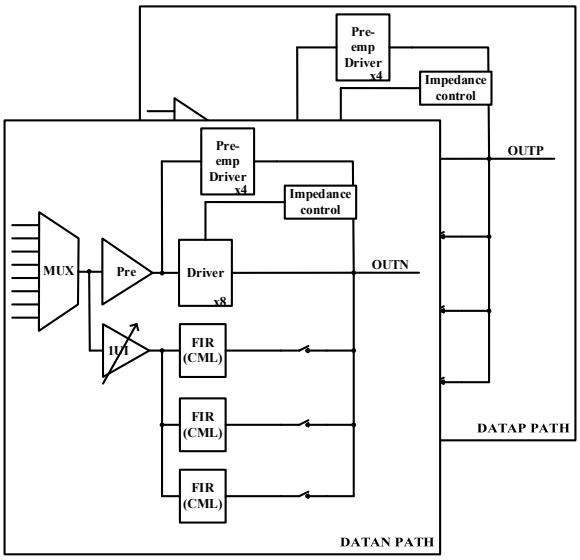

Fig. 2. Proposed differential pre-emphasis SST driver with 1-tap adjustable FIR.

II. DESIGN METHODOLOGY

A. Adjustable Current-mode Logic FIR filter

When a signal is transmitted over a long distance in a channel, there is a loss for Inter Symbol Interference (ISI), which causes some distortion or loss of the signal, and the result is that it is difficult to recognize the signal when it reaches the receiver part. There are two main sources of signal loss in a channel, one of them is the skin effect, and the other is dielectric loss. To compensate for the loss of signal in transmission, several steps are usually taken in advance at the transmitting end (TX) to compensate for possible loss in the signal, such as pre-emphasis, or Finite impulse response (FIR) filter, or at the receiver side, the signal that has already changed is processed by applying some equalizers such as Infinite impulse response (IIR) or Continuous Time Linear Equalization (CTLE). This work is designed on the TX side, so the proposed techniques are based on the TX equalization techniques.

There are two main techniques proposed for TX side, one of them is pre-emphasis and the other one is employing FIR filters. This system is a hybrid system that applies both pre-emphasis and FIR.

The pre-emphasis technique uses the method in ref [5], which utilizes the XOR gate to input the original data and delayed data by 1UI, respectively. The purpose of the pre-emphasis logic module is to add a short pulse at every transition of the main signal to boost its high-frequency transitions, which results in a shorter rise and fall time. Since this approach only partially offsets the channel loss, FIR is also used for equalization.

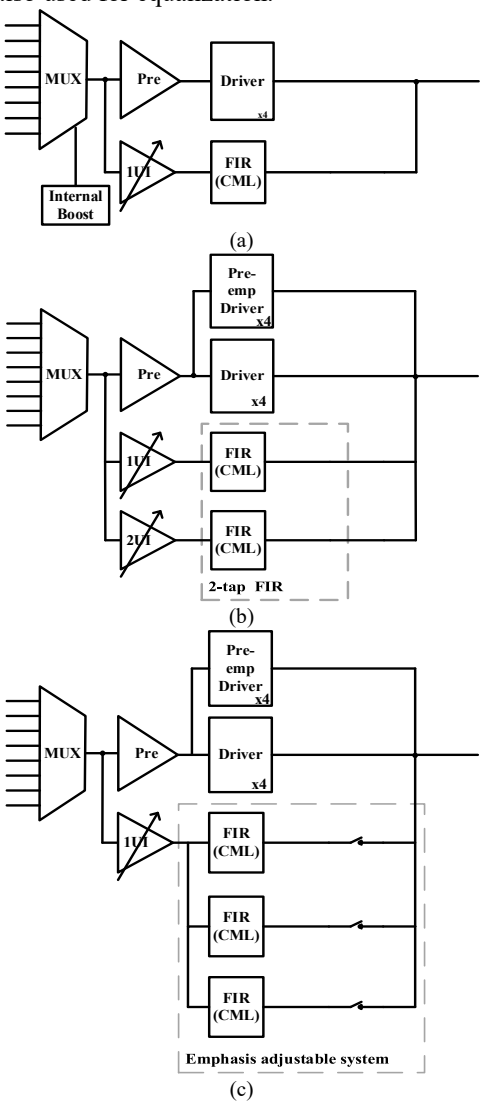

Fig. 3. Pre-emphasis TX topology: (a) conventional pre-emphasis topology, (b)2-tap FFE pre-emphasis topology, (c) Proposed adjustable pre-emphasis TX topology.

FIR is used to remove the effect of the remaining ISI on the overall signal. However, FIR sometimes comes at the cost of reducing the amplitude of the signal. Therefore, to ensure a high swing, a CML (Current-mode logic) structure is used to implement the FIR (Fig. 4).

TABLE II. Enable emphasis logic block

ENABLEA	ENABLEB	STATE
0	0	No emphasis
0	1	Emphasis1
1	0	Emphasis2
1	1	Emphasis3

Unlike the traditional 1st tap, 2nd tap FIR in Fig. 3(a) [3] and Fig. 3(b) [5], the FIR in this paper (Fig. 3(c)) adopts a FIR that can be adjusted by two enable signals. A logic cell consisting of logic gates is introduced to achieve the FIR by inputting a signal. The logic cell consists of NAND gate and OR gate, which are introduced to achieve the purpose of control by input signals ENABLEA and ENABLEB. According to the input signal ENABLEA and ENABLEB, LOGICA, LOGICB, and LOGICC can be presented in 0 or 1, respectively, thereby realizing the switching control on the Current-Mode Logic (CML) part in the system (Table II).

Ordinary FIR (Fig. 3. (a), (b)) will be realized by CML and directly connected in series at the TX output, but the CML proposed in this paper adds two switches at the series end, and the connection of the switches determines whether the corresponding FIR filter is connected to the overall system circuit or not. It is only necessary to control the switching of the three switches by controlling the two inputs, ENABLEA and ENABLEB, to access one 1st tap FIR or two 1st tap FIR or three 1st tap FIR simultaneously. This controls the number of CML LOGIC connections, as shown in Fig.4.

B. Hybrid Impedance Control

The impedance control can be performed based on the driver topology. The driver topology used in this paper is based on the SST driver, and the traditional analog based impedance control is difficult to accomplish all the impedance matching, so the hybrid impedance control is used. [7] The impedance control is done by using analog-loop based loop and through the number of SST slices.

The initial adjustment is managed by selectively enabling and disabling driver slices, which constitutes the course tuning mechanism. Subsequently, to account for the finer variations in NMOS/PMOS impedances, in passive resistance, an analog loop for impedance control is employed, ensuring precise fine tuning. This analog impedance control loop is adept at also correcting for discrepancies between PMOS and NMOS impedances, ensuring balanced and accurate impedance matching across the circuit.

Fig. 4 presents the detailed circuit and connectivity for the entire transmission (TX) system. A pair of differential paths are employed for the signal route for enhanced signal integrity. Each pathway receives a 1GHz input, capable of amplifying up to 8GHz at the multiplexer (MUX) output. Additionally, a pre-emphasis mechanism is incorporated and facilitated through dual pathways. Beyond the conventional referenced output signal, the terminal of each pathway features a trio of current-mode logic (CML) finite impulse response (FIR) circuits. The resultant outputs can be checked at the OUTN and OUTP terminals.

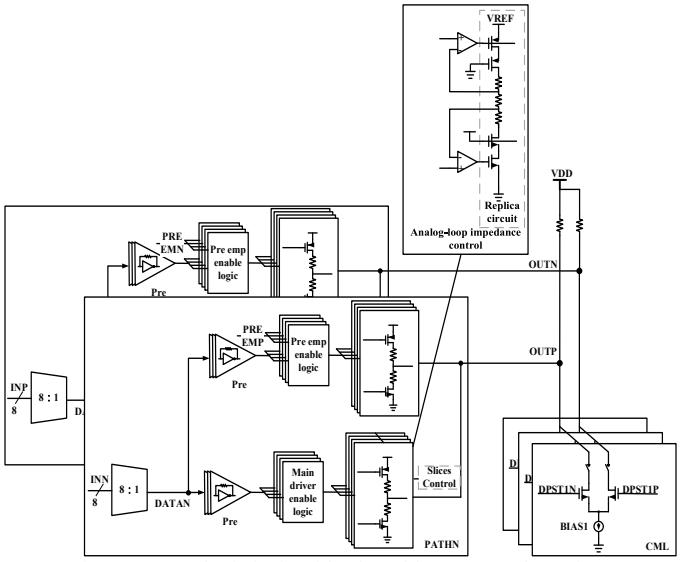

Fig. 4. Pre-emphasis logic with adjustable FIR top schematic.

III. RESULTS AND DISCUSSIONS

To ensure the integrity of the signal transmission and immunity to interference, the system selects the differential signal transmission structure, which is sent by 2 adjacent channels, so that the signals at the receiving end can also be detected individually and a higher output swing can be realized, so the matching transmission channel is also two channels. A pair of differential output signals from the TX side reaches the receiver side after passing through a channel. This work utilized an FR4-based microstrip line with a length of 8m as the transmission channel model. The channel has a 10dB loss at 8GHz. Fig. 5 shows the frequency response of the proposed channel model.

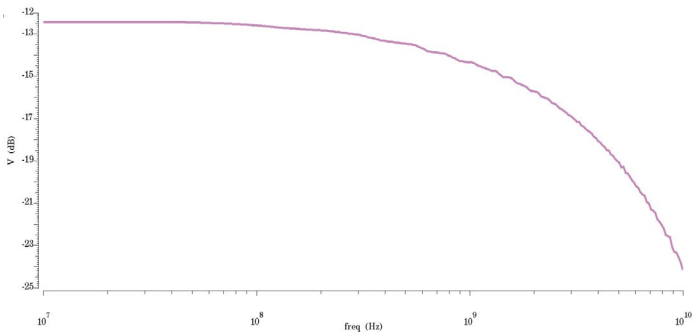

Fig. 5. 8m microstrip FR4 channel model frequency response.

The effectiveness of the equalization techniques in part II

can be checked at the receiving end (RX) by using the eye diagram. Before measuring the equalization result, the emphasized signal can be obtained from the differential output of the TX. The overall signal swing is higher than that of the TX with only the CML driver due to the hybrid topology of the SST driver and the FIR CML. Fig. 9 shows the output of the emphasized differential signal in emphasis state 3 at 8G Hz. As depicted in Fig. 6, the actual output swing of the signal is in the range of -1.2V ~ + 1.2V, and the output result of the adjusted emphasis part is in the range of -1.4V ~ +1.4V. In 8GHz, the output differential signal's rising edge and falling edge have been minimized to decrease the time jitter because of the employment of pre-driver.

Also, the four states that can be controlled by emphasis logic can be identified in Fig. 7. According to the input of [0,0], [0,1], [1,0], [1,1] for ENABLEA and ENABLE B respectively, the four states of LOGICA, LOGICB, LOGICC can be derived, and the outputs of these four states are [0,0,0], [0,0,1], [0,1,1]. [1, 1, 1], corresponding to no access to the CML logic (no emphasis state), access to a CML logic (emphasis 1), access to two CML logic (emphasis 2) and access to three CML logic (emphasis 3).

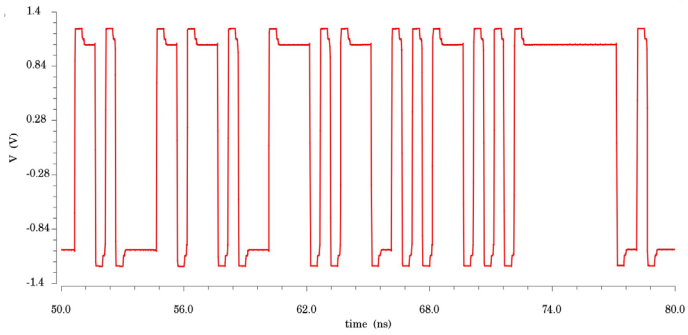

Fig. 6. Differential output signal swing at emphasis state 3.

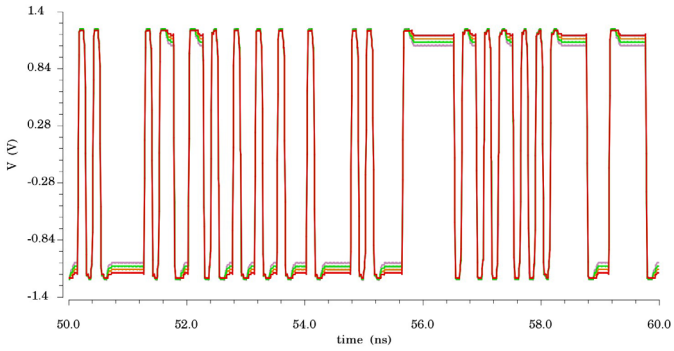

Fig. 7. 4 emphasis state differential output signal at TX.

Therefore, the actual output of the emphasis can be confirmed by comparing the differential output signal of the TX output. To compare the three states, the role of pre-emphasis in the system has been dropped when comparing the four states. In Fig.7, the red line, orange line, green line and purple line represent four states, which are no emphasis state, emphasis 1, emphasis 2 and emphasis 3, respectively. In the case of no 1-tap FIR and only SST driver, the output swing can reach 1.3V, and with the increase of the number of accessed CMLs, the magnitude of the emphasis gradually becomes greater, which is around 53mV, 110mV and 180mV, respectively. According to Fig. 7, it can be seen that at 8G Hz, the overall signal has been equalized to different degrees, corresponding to different channel losses.

Fig. 8 shows the result of differential output signal at transmitter and receiver after both pre-emphasis logic and FIR adjustable system are applied. Because of the high amplitude output, the signal at the receiving end maintains -500mV ~ +500mV even after channel transmission.

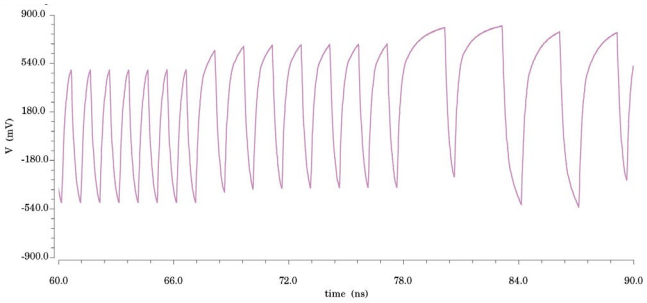

Fig. 8. Differential output signal after channel.

Fig. 9 shows the pre-emphasis part pre-layout simulation result and post-layout simulation result. Compared with pre-layout simulation result (Fig. 9), the post-layout simulation result has a delay at the rise time and fall time. Also, because of the use of rf model, the guard ring has been arrayed in the top schematic layout (Fig. 10), the comparison between the pre-layout and post-layout simulation results reveals that the delay time at 8GHz is minimally affected. Furthermore, the emphasis on the voltage level is maintained at approximately 200mV.

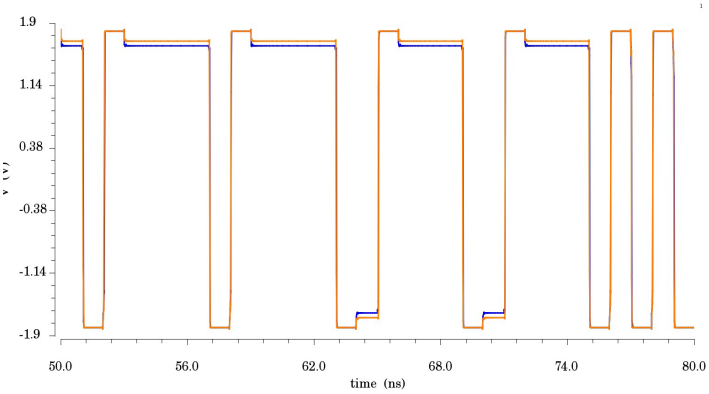

Fig. 9. Pre-emphasis part pre-layout simulation result (Orange line) and post-layout simulation result (Blue line).

Fig. 10 shows the layout of proposed TX system top schematic layout, which has an area of 76.5um * 185um.

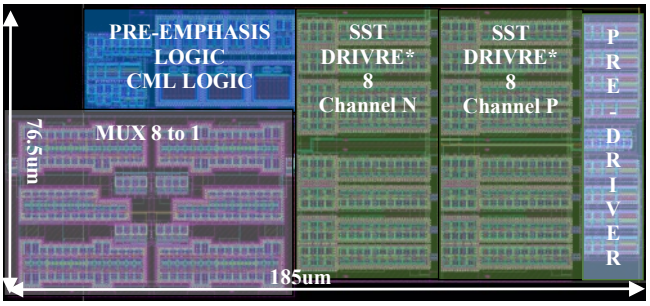

Fig. 10. Top schematic layout.

TABLE III. Comparison table with other paper

	[5]	[6]	[7]	[8]	[9]	This Work (Simulation)
Process(nm)	65	40	16	65	40	65
Driver topology	Hybrid CML + SST	VM SST	VM SST	VM SST	VM	Hybrid CML + SST
Power supply(V)	1.2	1.1	1.2	1.2	1	1.8
TX FEE tap	3-tap	3-tap	3-tap	2-tap	N/A	3-tap
TX swing (Vpp)	1.1	210m	900m	300m	400m	1.2
Data rates (Gbps)	1.28	50	28	20	5	8
Channel loss at Nyquist(dB)	13-25	5.2	5	6.02	5-10	10
Eye Width (UI)	0.6-0.78	N/A	N/A	N/A	0.32	0.75
Eye height(mV)	81-278	N/A	N/A	160	110	500

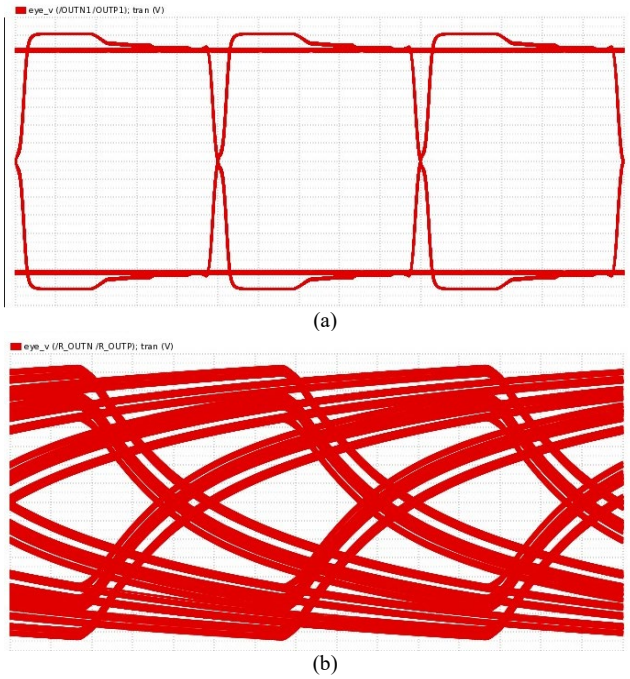

Fig. 11. Emphasis state 3 output eye diagram comparison through channel (a)before channel (b)after channel.

Fig. 11 shows the eye diagram results of the signal before and after the input channel. In Fig. 11(a), the eye diagram has not yet been influenced by channel frequency response and there is a pre-emphasis part in each UI that also preserves a low time jitter. After the channel transmission (Fig. 11(b)), the eye diagram can be opened up to about 0.75UI.

Comparison of Table III with [5], [6], [7], [8], [9] and Fig. 11 shows that the system has the advantage of high swing with a swing of 1.2 V. At the same time, it can realize a larger eye width, 0.75 UI, and higher eye height (500 mV) than the similar hybrid structure system at a higher frequency of 8 GHz. At the same time, hybrid impedance control is applied to realize the data jitter control within 5ps.pp range.

IV. CONCLUSION

This system proposes a hybrid transmitter and driver using SST topology in Volage-mode, as well as hybrid equalization using pre-emphasis logic and FIR CML hybrid form. In the CML structure, four states of emphasis that can be controlled are proposed to achieve equalization under different channel conditions. Due to the use of an SST driver, a high swing output signal, which can reach about 1.2V, was obtained. Meanwhile, due to the hybrid equalization, the eye open width is improved to reach 0.75UI. A good hybrid impedance control is also proposed in this paper, which utilizes SST slices and an analog replica loop for hybrid impedance control. Finally, the system achieves an eye opening of 0.75UI and an eye height of 500mV at 8GHz with a channel loss of 10dB.

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