A Current-Mode VCSEL Driver for Short-Range LiDAR Sensors in 180-nm CMOS

Xinyue Zhang[1,2], Yeojin Chon[1,2], Shinhae Choi[1,2], Sung Min Park[1,2,a]
[1]Department of Electronic and Electrical Engineering, Ewha Womans University
[2]Graduate Program in Smart Factory, Ewha Womans University
E-mail: zhangxinyue@ewhain.net , smpark@ewha.ac.kr

***Abstract* -This paper presents a current-mode VCSEL driver (CMVD) implemented in a 0.18-µm CMOS technology for the applications of short-range LiDAR sensors, where a current-steering logic is exploited to deliver the modulation currents (from 0.1 to 10 mA_{pp}) and the bias current of 0.1 mA to the VCSEL diode simultaneously. For simulations, the VCSEL diode is modeled as a 1.6-V forward bias voltage with a 50-Ω series resistor. The post-layout simulations of the proposed CMVD demonstrate vividly large output pulses and clean eye-diagrams. The chip consumes a maximum of 44 mW from a 3.3-V supply and the core occupies the area of 0.1 mm^2.**

***Keywords*—current-mirror, current-mode, current-steering logic, LiDAR, VCSEL.**

I. INTRODUCTION

Recently, light detection and ranging (LiDAR) sensors have been utilized in various fields, such as advanced driver assistance systems for unmanned vehicles, remote sensing detection and navigation systems for robots, and indoor-monitoring systems [1,2]. LiDAR sensors exploit the pulsed time-of-flight (ToF) measuring mechanism, hence ensuring successful operations of scanning. Fig. 1 depicts the block diagram of a typical short-range LiDAR sensor, where the transmitter equips a laser diode driver to emit light pulses to targets. The reflected light pulses can be detected by the receiver that comprises an optical detector, a transimpedance amplifier (TIA), a single-to-differential (S2D) converter, a post-amplifier (PA), and a time-to-digital converter (TDC).

Typically, laser diodes are bi-directional and costly. Also, they require large bias voltages, depending upon the specific target applications (e.g., for high-speed optical interconnects). To the contrary, vertical cavity semiconductor emitting laser (VCSEL) diodes are unidirectional and operate with a relatively lower bias voltage. This characteristic renders VCSEL diodes more suitable for low-cost low-power short-range LiDAR sensors. However, the inevitable bond-wire between the optical device and the integrated circuit (IC) causes various problems that include the notorious voltage headroom issue, especially in the architecture of DC-coupled laser diode drivers [3]. In addition, on-chip electro-static discharge (ESD) protection diodes should be employed to avoid damage from the off-chip ESD, which may shrink the receiver bandwidth by the increased parasitic capacitance.

Previously, a number of research have been conducted to develop high-speed laser diode drivers that were implemented in bulk CMOS processes for optical interconnects [4-9]. Especially for long-range LiDAR sensors in autonomous vehicles, costly laser diodes have been exploited to emit narrow pulses. But, for short-range LiDAR sensors in indoor monitoring applications, rather low-cost VCSEL diodes can be more suitable, particularly for the fall detection of dementia patients at home [2,3]. It is well known that a VCSEL diode mandates a forward voltage above 1.5 V for light emission. Therefore, its supply voltage (VDD) must be set high enough to ensure the robust operations of VCSEL diodes [5]. Among the two types of VCSEL diode drivers, i.e., common-cathode and common-anode, the common-anode VCSEL allows the supply voltage (VDDL) of the chip to be effectively reduced by externally biasing the VCSEL diode with an elevated voltage (VDDH). Thereby, this configuration may reduce power consumption substantially, presenting a more efficient method for driving VCSEL diodes. Nonetheless, it's crucial to indicate that the adoption of common-anode VCSEL diodes demands the incorporation of an additional supply voltage. Hence, a common-cathode VCSEL diode driver still tends to be preferred due to its compatibility with prevailing requirements and constraints [4,5].

Section II describes the operations of the proposed current-mode VCSEL driver (CMVD) circuit. Section III presents the layout of the CMVD and its simulation results. Then, a conclusion is followed.

II. ARCHITECTURE

Fig. 2(a) illustrates a voltage-mode laser diode driver (VMLD) based on the push-pull inverter scheme, where a current signal is injected into the VCSEL diode through either the pull-up (PMOS) or the pull-down (NMOS) transistor. This type of VMLD has been exploited for optical transmitters due to the simple architecture.

a. Corresponding author; smpark@ewha.ac.kr

Manuscript Received Jan. 18, 2024, Revised Feb. 28, 2024, Accepted Mar. 14, 2024

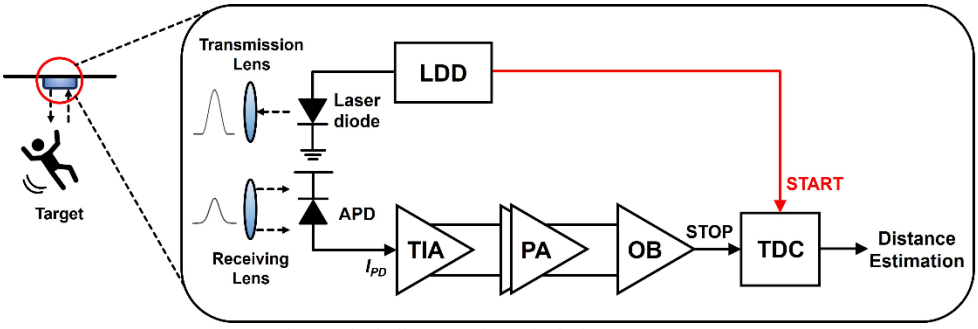


Fig. 1. Block diagram of a typical LiDAR sensor.

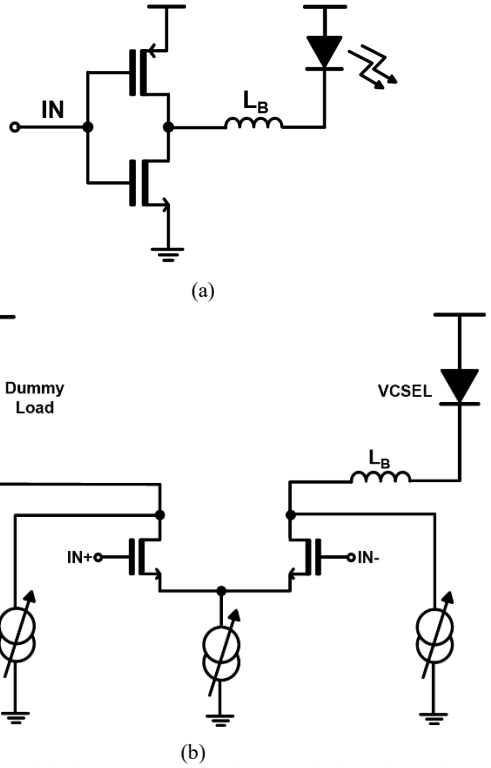


Fig. 2. (a) Simplified inverter-based voltage-mode laser diode driver, (b) its differential structure.

Typically, differential structures are preferred for low common-mode noises due to their symmetry, as shown in Fig. 2(b). However, they mandate either an additional laser diode that should be connected via a bond-wire for symmetry or an on-chip dummy load that mimics the electrical model of a laser diode (i.e., a forward bias voltage with a series resistance and a bond-wire inductance). Nonetheless, the former raises the manufacturing costs considerably, while the latter deteriorates the symmetry, hence resulting in the undesired asymmetric output waveforms.

Besides, the modulation currents in this type of VMLD are generated by varying the gate voltages of the current source in the differential pair, which however is quite difficult to control the precise amplitudes of the output waveforms. Also, the bias control path should be separately equipped to supply the DC bias currents to the laser diode, which leads to unnecessarily extra chip area. Moreover, it is very likely to occur relaxation oscillations in the output waveforms if this bias control malfunctions.

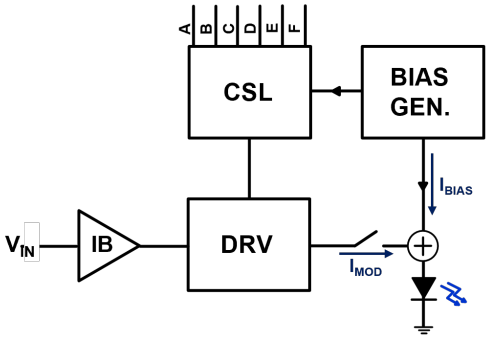


Fig. 3. Block diagram of the proposed CMVD.

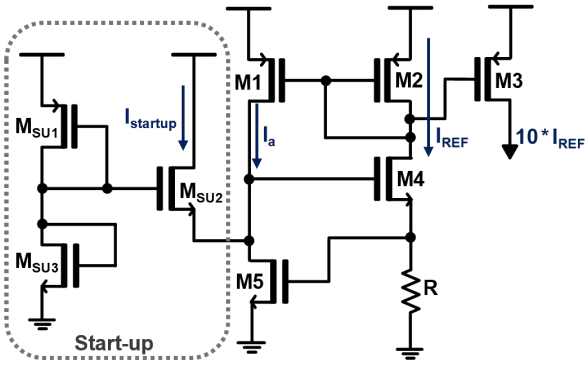


Fig. 4. Schematic diagram of the BIAS circuit.

In this paper, a current-mode VCSEL diode driver (CMVD) is suggested to overcome the aforementioned issues. First, the bias current control path is merged with the modulation current control path, thereby reducing the chip area and facilitating the stable operations of the VCSEL diode. Second, a current-steering logic is proposed to supply various modulation currents to the VCSEL diode, therefore enabling to control the amplitudes of the modulation currents more facilely than the VMLDs. Third, the architecture of the proposed CMVD is very simple. However, there is still a disadvantage in this structure that is single-ended, which is prone to common-mode noises such as power supply noise. This problem can be discarded considerably by utilizing an off-chip voltage regulator on a testing PC-board.

Fig. 3 shows the block diagram of the proposed CMVD, which consists of an input buffer (IB) for the isolation from the preceding stage, a driver circuit (DRV) for passing through the bias and modulation currents to the VCSEL diode, a bias circuit for the generation of the bias currents, a current-steering logic (CSL) for the supply of the varying modulation currents via a 6-bit control digital-to-analog converter (DAC), and a VCSEL diode.

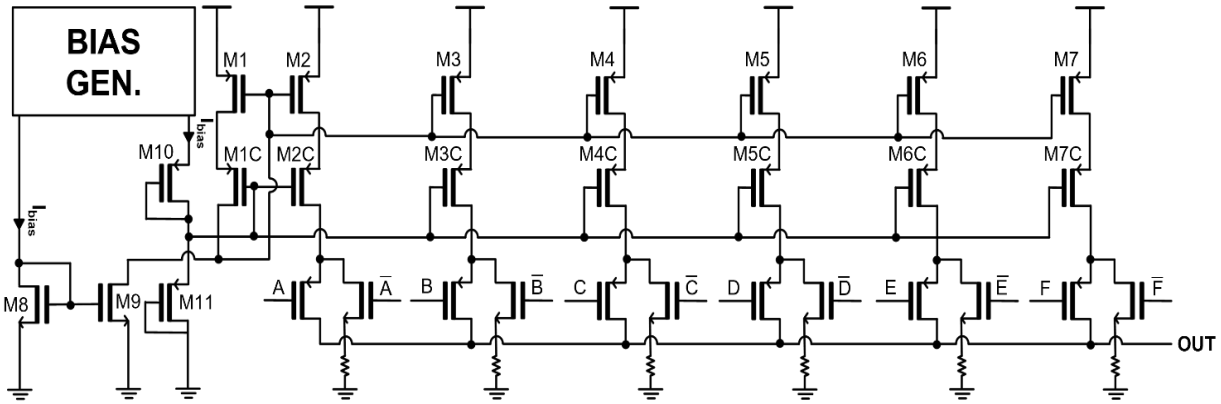


Fig. 5. Schematic diagrams and the specific parameters of CSL blocks.

Fig. 4 depicts the schematic diagram of the bias current control circuit, where the start-up circuit initiates the operations. Then, two currents I_a and I_{REF} can be identical by the action of current mirrors formed by the PMOS transistors (M_1 and M_2). Since the current (I_{REF}) flows through a resistor R, a voltage-drop of I_{REF} * R occurs and is equal to the gate-source voltage V_{GS5} of M_5. Therefore, I_{REF} varies barely with the supply voltage, hence providing good stability, provided that the equilibrium point of the bias circuit is settled. Afterwards, a stable reference current (i.e., 1 mA in this work) is supplied with the aid of another PMOS (M_3) to the following CSL circuit and VCSEL diode. The NMOS (M_4 and M_5) function as a regulated cascode to stabilize the bias current by the feedback mechanism.

Fig. 5 shows the schematic diagram of the CSL circuit, where the bias current is inserted to the NMOS (M_8 and M_9) current mirror, and then mirrored by the PMOS current mirrors (M_1~M_7 and M_{1C}~M_{7C}) that can be either turned-on or turned-off by using the six switches (A to F). The diode connected PMOS transistors (M_{10} and M_{11}) set the DC voltages of the PMOS current mirrors. It is noted that the DC currents of the PMOS current mirrors pass through to the VCSEL diode under the condition that the gate voltage is lower than the threshold (i.e., VDD – $|V_{THP}|$), where V_{THP} represents the threshold voltage of a PMOS transistor.

The PVT variation simulations of the proposed CSL circuit confirm that the modulations currents alter 20 % in maximum for the worst case of SS with the supply voltage of 2.97 V at the temperature of 125 ºC. This reveals that the CSL block provides rather stable operations against the considerable PVT variations.

III. LAYOUT & SIMULATION RESULTS

Fig. 6 depicts the layout of the proposed CMVD, where the chip core occupies the area of 0.1 mm^2. Post-layout simulations were conducted by using the model parameters of a standard 180-nm CMOS technology. DC simulations yield that the chip dissipates 44 mW from a 3.3-V supply.

Fig. 7 compares the simulated pulse responses of a conventional voltage-mode VCSEL driver and the proposed CMVD with the variations of the modulation currents from 0.1 mA_{pp} to 10 mA_{pp} for the narrow pulse width of 5 ns. It is clearly seen that the output pulses of the proposed CMVD are linearly generated even with the large variation of modulation currents. Yet, the peaking at the rising edges might be attributed to the total capacitance at the output node that includes the parasitic capacitance of the VCSEL diode and the CSL circuit.

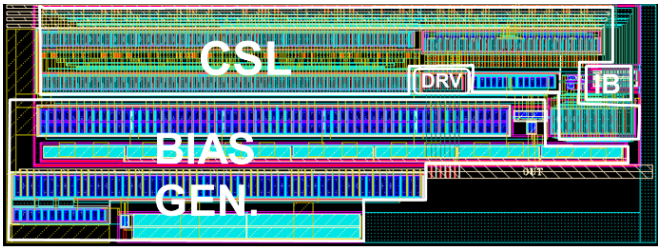
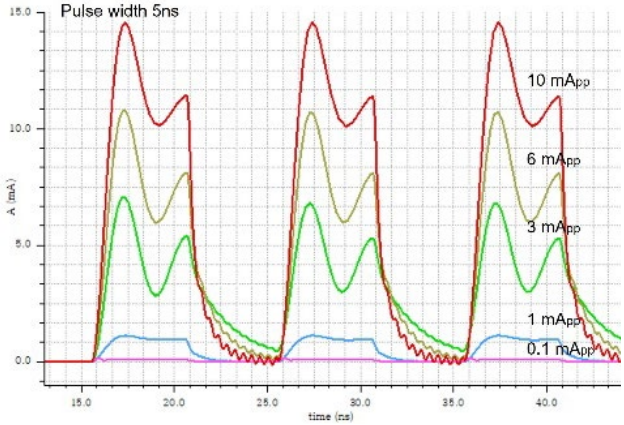
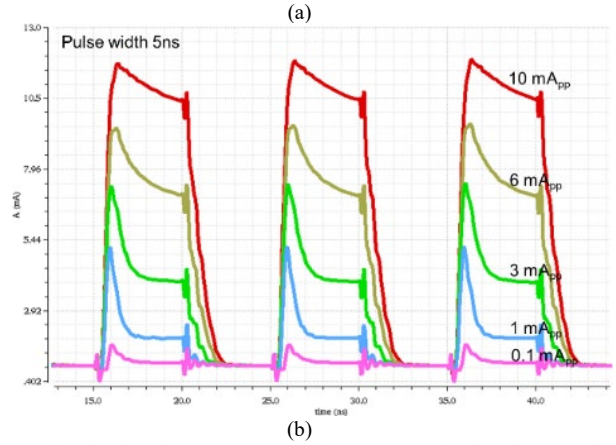


Fig. 6. Chip layout of the proposed CMVD.

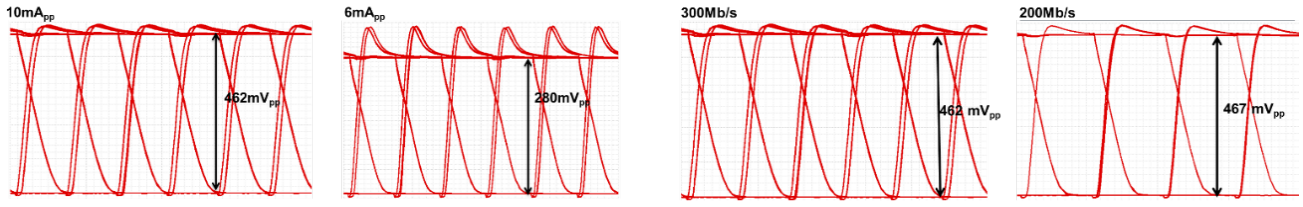


(a)



(b)

Fig. 7. Simulated pulse responses of (a) a conventional voltage-mode VCSEL driver, and (b) the CMVD with 1~10 mA_{pp} modulation curr ents for the narrow pulse width of 5 ns.



(a) (b)

Fig. 8. Simulated eye-diagrams for (a) 10 mA$_{pp}$ and 6 mA$_{pp}$ modulation currents at 300 Mb/s, and (b) 10 mA at 300 Mb/s and 200 Mb/s.

TABLE I. PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED CMOS LASER DIODE DRIVERS.

PARAMETERS	[6]	[7]	[8]	[9]	**This work**
CMOS technology (nm)	65	180	180	180	**180**
Supply (V)	1.2/2.5	1.8/3.5	1.8	1.8/3.3	**3.3**
Laser diode	VCSEL	laser diode	laser diode	VCSEL	**VCSEL**
Configuration	voltage-mode	voltage-mode	voltage-mode	voltage-mode	**current-mode**
Output signaling	single-ended	differential	differential	differential	**single-ended**
Driver type	common-cathode	common-cathode	common-anode	common-anode	**common-cathode**
Modulation current (mA$_{pp}$)	6	2~14	1~16	2~12.5	**0.1~10**
Bias current (mA)	2	-	1~10	-	**1**
Core area (mm^2)	3.2 (chip)	0.12 (1 ch.)	0.13 (1 ch.)	0.21	**0.1**

Fig. 8(a) shows the simulated eye-diagrams of the CMVD at 300 Mb/s for the different input currents of 10 mA$_{pp}$ and 6 mA$_{pp}$, respectively, where the output amplitudes are almost linearly amplified with respect to the modulation currents. Fig. 8(b) depicts the simulated eye-diagrams at the same input current levels of 10 mA$_{pp}$ for the different speed of 300 Mb/s and 200 Mb/s, confirming the wide and clean eyes with the almost identical amplitudes.

Table I summarizes the performance of the CMVD with the previously reported CMOS VCSEL drivers. In this work, we have proposed a novel single-ended CMVD with stable bias currents by exploiting the regulated cascode current-mirror circuitry and with the novel CSL to provide variable modulation currents up to 10 mA$_{pp}$.

IV. CONCLUSIONS

We have presented a current-mode VCSEL driver by utilizing a 180-nm CMOS process, in which a current-steering logic circuit was employed to facilely deliver the modulation currents from 0.1 mA$_{pp}$ to 10 mA$_{pp}$ with PMOS current mirrors. Also, the bias current generator using a regulated cascode circuit was exploited to provide stable DC bias currents against the notorious PVT variations. Conclusively, the proposed CMVD can be a highly efficient solution for the applications of short-range LiDAR sensors.

ACKNOWLEDGMENT

This research was supported by the MSIT (Ministry of Science and ICT), Korea, under the ITRC (Information Technology Research Center) support program (IITP-2020-0-01847) supervised by the IITP (Institute for Information & Communications Technology Planning & Evaluation). The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

REFERENCES

[1] T. Raj et al., "A Survey on LiDAR Scanning Mechanisms," ***Electronics***, vol. 9, no. 5, pp. 741, Apr. 2020.

[2] D. Yoon, J. -E. Joo, and S. M. Park, "Mirrored Current-Conveyor Transimpedance Amplifier for Home Monitoring LiDAR Sensors," ***IEEE Sensors J.***, vol. 21, pp. 5589-5597, Mar. 2021.

[3] J. -E. Joo et al., "An Indoor-Monitoring LiDAR Sensor for Patients with Alzheimer Disease Residing in Long-Term Care Facilities," ***Sensors***, vol. 22, no. 20, pp. 1934, Oct. 2022.

[4] H. Choi et al., "A 35-Gb/s 0.65-pJ/b Asymmetric Push-Pull Inverter-Based VCSEL Driver with Series Inductive Peaking in 65-nm CMOS," ***IEEE Trans. on Circuits and Systems II***: Express Briefs, vol. 65, no. 12, pp. 1824-1828, Dec. 2018.

[5] K. T. Ng, Y. B. Choi, and K. C. Wang, "A 25Gb/s Common-Cathode VCSEL Driver," in ***IEEE CSIC Symp.***, pp. 1-4, 2014.

[6] D. Guo et al., "Developments of two 4 × 10 Gb/s VCSEL array drivers in 65 nm CMOS for HEP experiments," ***J. of Instrumentation***, vol. 12, no. 2, pp. C02065, Feb. 2017.

[7] C. Yingmei, Z. Dawei, Z. Li, and L. Wei, "A four-channel parallel 40 Gb/s laser diode voltage driver in 0.18-μm CMOS," ***Microwave &Optical Tech. Lett.***, vol. 55, no. 7, pp. 1540-1543, Jul. 2013.

[8] L. Wenyuan, C. Sun, Q. Zhao, and W. Xiong, "Design of 12-channel 120Gb/s laser diode driver array in 0.18μm CMOS technology," ***Inter. Conf. on ATC***, Hanoi, Vietnam, pp. 27-31, 2014.

[9] Y. Chen et al., "Low power 13 Gbit/s VCSEL current driver in 0.18μm CMOS for optical interconnection," ***J. of China Universities of Posts and Telecommunications***, vol. 20, no. 2, pp. 125-128, Apr. 2013.

Xinyue Zhang received the B.S. degree in electronic information science and technology from Linyi University, Shandong, China, in 2021, and the M.S. degree from Ewha Womans University in 2024. Her current research interests include silicon photonics, and CMOS optoelectronic integrated circuits and architectures for short distance optical systems and sensor interface IC designs.

Yeojin Chon received the B.S. degree in electronic and electrical engineering from Ewha Womans University, Korea, in 2022. She is currently working toward the MSc degree in the analog circuits and systems lab. at the same university. Her current research interests include silicon photonics, and CMOS optoelectronic integrated circuits and architectures for short distance optical systems and sensor interface IC designs.

Shinhae Choi received the B.S. degree in electronic and electrical engineering from Ewha Womans University, Korea, in 2023. She is currently working toward the MSc degree in the analog circuits and systems lab. at the same university. Her current research interests include silicon photonics, and CMOS optoelectronic integrated circuits and architectures for short distance optical systems and sensor interface IC designs.

Sung Min Park received the B.S. degree in electrical and electronic engineering from KAIST, Korea, in 1993. He received the M.S. degree in electrical engineering from University College London, U.K., in 1994, and the Ph.D. degree in electrical and electronic engineering from Imperial College London, U.K., in May 2000. In 2004, he joined the faculty of the Department of Electronics Engineering at Ewha Womans University, Seoul, Korea, where he is currently a professor.