Ka-band CMOS Power Amplifier with Self-Biasing-Resistor

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***Abstract* - In this paper, a CMOS power amplifier using a Self-Biasing-Resistor transistor for Ka-band is proposed. Generally, when designing a power amplifier with a cascode structure, a structure connecting the source and body of the transistor is used. This changes the inter-cascode voltage depending on the output of the common-source stage, which changes the body voltage of the common-gate stage, ultimately changing the I-V curve. Therefore, by inserting a large resistor between the body and the source, parasitic capacitors are used to split the RF signal swing in the body and compensate for voltage changes. As a result, AM-AM and IMD3 have been improved, and it has a linear output power of 13.1dBm and a linear PAE of 22.6% at a supply voltage of 2.4V.**

***Keywords*—AC Dividing, AM-AM, Cascode, CMOS, Ka-band**

I. INTRODUCTION

In the case of a CMOS power amplifier, distortion of communication signals occurs due to parasitic capacitance of the CMOS device. To improve the distortion of these signals, digital pre-distortion (DPD) and analog linearization techniques are used. Large linearity improvements can be achieved using DPD techniques. However, it is unsuitable for IoT because of its complex implementation and power consumption. Therefore, research on small size analog linearization circuits with low-power-consumption is needed for the RF CMOS PA for IoT.

In previous studies, analog linearization techniques have been implemented by adding additional circuitry. However, because they have smaller size and lower power consumption compared to a power amplifier, there is a lack of research on the optimization of the circuit [1~5]. Although this may be less effective than a power amplifier, it is important in terms of implementing a power amplifier for IoT, where miniaturization and low power consumption are very important. Therefore, in this paper, we proposed a self-biasing linearization technique that can improve the linearity of a power amplifier without additional area and power consumption by using a simple resistor.

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Manuscript Received Nov. 24, 2023, Revised Jan. 31, 2024, Accepted Mar. 6, 2024

II. PA WITH SELF-BIASING-RESISTOR (SBR) TECHNIQUE

CMOS power amplifiers typically feature a low breakdown voltage and lack a ground via, requiring grounding through bonding wire or metal lines. To address these challenges, they are often designed with both a differential structure and a cascode structure. When a differential structure is used, a virtual ground can be created and used. A Transmission Line Transformer (TLT), which can act as a balun, is used to convert single and differential signals. The TLT can also be used to match the impedance of the input and output. To match through an effective impedance matching network, the output TLT uses a broadside coupling method and has a size of 145um x 100um. The input TLT uses the edge coupling method and has a size of 160um x 60um. The TLT used in the proposed power amplifier is shown in Figure 1.

A gate width of 256um was determined and used for M1, M2, M3, and M4 transistors of the common-source (CS) and common-gate (CG) stages. In addition, to address the issue of gain reduction due to negative feedback from the transistor's parasitic capacitor, a cross-coupled capacitor was used in the CS stage and used as positive feedback to increase the gain.

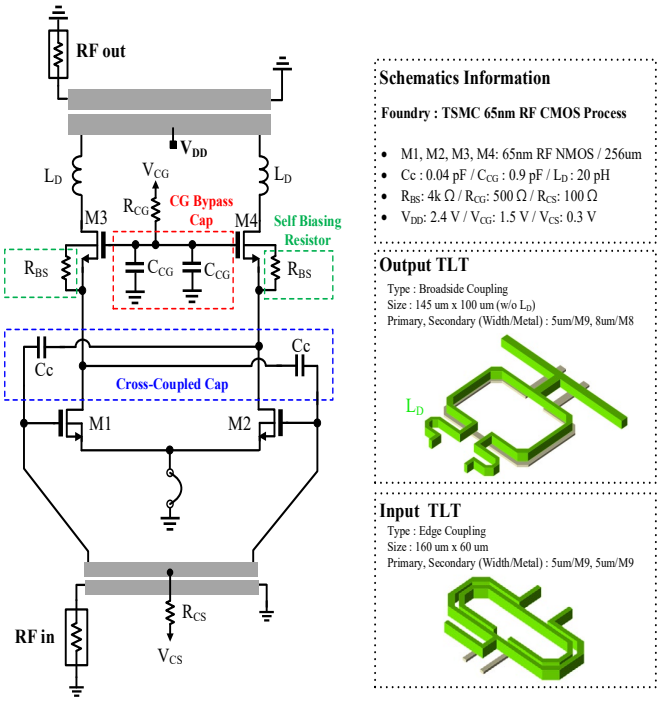


Fig. 1. Schematic of the proposed CMOS power amplifier.

When a cascode structure is used, a CS stage and a CG stage are used. The body and source of a CG transistor are connected in a general power amplifier. In the proposed power amplifier, a Self-Biasing-Resistor (SBR) technique has been proposed in which a resistor of several kOhm is inserted between the body and source of the CG transistor, as shown in the schematic in Figure 1.

A. Analysis of cascode power amplifier with transistor body-source connection

CMOS power amplifiers generally use a method of connecting the body and source of a transistor. The effect of this structure is that the body and source have the same DC voltage. However, this structure has problems due to the threshold voltage of the transistor.

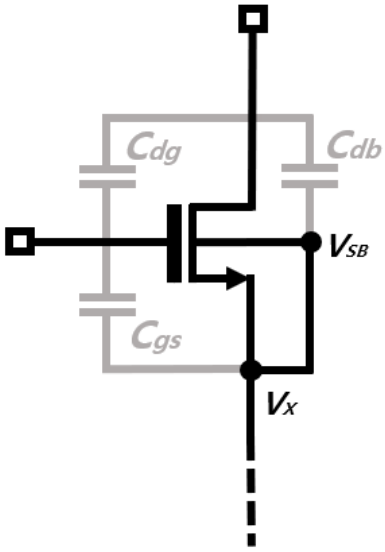


Fig. 2. CG transistor connecting body to source.

Figure 2 is a CG transistor with a structure where the body and source are connected. When the body and source are connected, V_X, the inter-cascode voltage connecting the CS stage and the CG stage, has the same voltage as V_{SB}. Therefore, the threshold voltage V_{TH} remains constant according to equation (1).

$$V_{TH} = V_{T0} + \gamma(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{2\phi_F}) \quad (1)$$

In equation (1), V_{TH} is the threshold voltage. $2\phi_F$ is the surface potential, V_{SB} is the source to body bias, V_{T0} is the threshold voltage for the zero body voltage, and γ is the body effect parameter [6].

However, the transistor operates in the triode region and turns off when the RF signal swing is large. In addition, the transistor behaves as a resistor in the CS stage due to the RF signal swing. As the transistor spends more time in the triode region, both the R_{ds} resistance and the inter-cascode voltage V_X increase. Therefore, as V_X increases, the operating I-V curve of both the CS and CG transistors changes. It also increases the probability of the breakdown of the CS transistors.

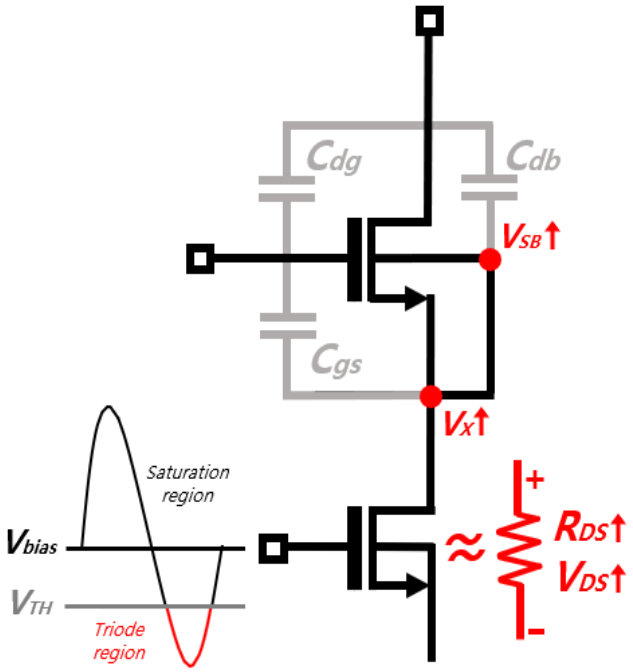


Fig. 3. Cascode structure of transistor connected to body source.

B. Analysis of cascode power amplifier with the proposed Self-Biasing-Resistor technique

There was a problem with the breakdown voltage occurring in the cascode power amplifier where the body and source were connected. Therefore, we propose a SBR technique that inserts resistors into the body and source.

Figure 4 shows a CG transistor using the proposed SBR technique. The parasitic capacitor C_{bs} was not present when the body and source were connected without resistors. However, because a large 4000 Ohm resistor R_{DS} is inserted, the parasitic capacitor C_{bs} is visible. As shown in Figure 5, the impedances of the parasitic capacitors C_{db} and C_{bs} are generated. As shown in equations (2) and (3), an AC voltage swing is divided and applied to V_{SB} due to the impedance of Z_1 and Z_2.

$$Z_1 = Z_{Cdb} \quad (2)$$

$$Z_2 = Z_{Cbs} \,//\, Z_{Rbs} \quad (3)$$

The RF signal swing applied to the V_{SB} changes according to the operating range of the CS transistor. Figure 6 shows the voltage variation of V_X as a function of the RF signal swing applied to the gate. When a positive voltage is applied to the CS gate, a negative voltage is applied to the inter-cascode voltage V_X and the body voltage V_{SB} decreases. Then, the threshold voltage V_{TH} of the CG stage decreases and V_X operates in the direction of increasing the voltage. Therefore, the decreasing voltage of V_X can be compensated.

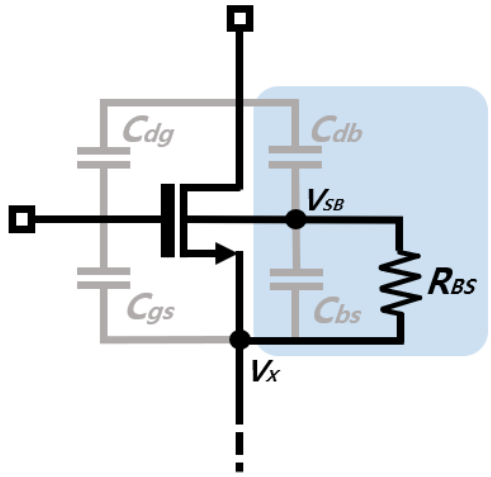


Fig. 4. CG transistor with resistance inserted between body and source.

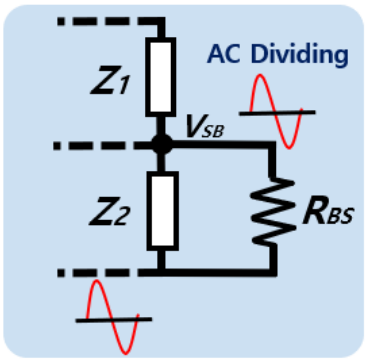


Fig. 5. AC Dividing.

When a negative voltage is applied to the gate of the CS transistor. Contrary to the case when a positive voltage is applied, a positive voltage is applied to V_X and the body voltage V_{SB} increases. The threshold voltage V_{TH} of the CG transistor increases and V_X operates in the direction of decreasing the voltage. It, therefore, compensates for the increasing V_X voltage.

Figure 6 shows the AC voltage swing applied to V_{SB} when using the SBR technique. We have confirmed that the AC voltage swing is in the range of approximately -0.5V to 0.2V.

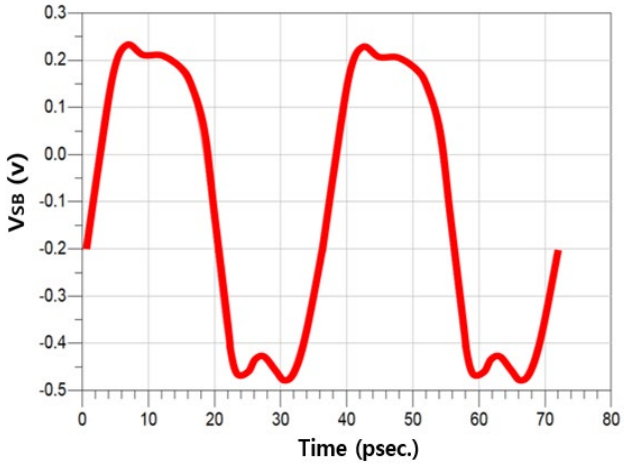


Fig. 6. AC voltage swing of V_{SB}.

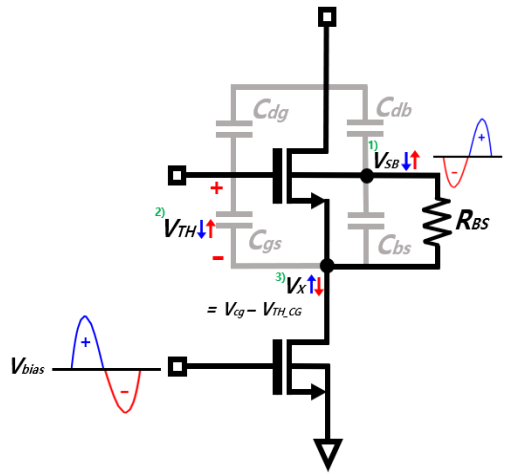


Fig. 7. V_X voltage due to CS transistor operation.

As above, the voltage V_X is determined by the negative and positive voltages applied to the CS transistor, and the voltage of V_X is kept constant. Therefore, a constant I-V curve is obtained regardless of the output of the CS transistor.

Figure 8 shows the voltage applied to the inter-cascode voltage V_X. We have seen that the voltage applied is constant using the SBR technique.

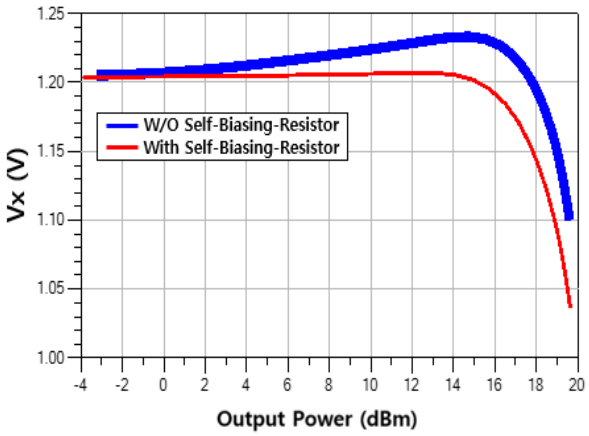
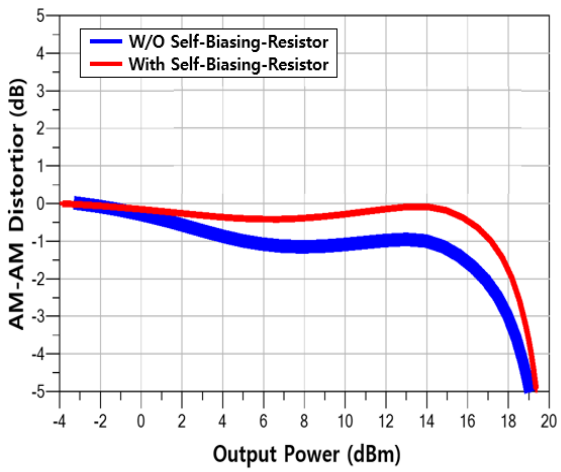
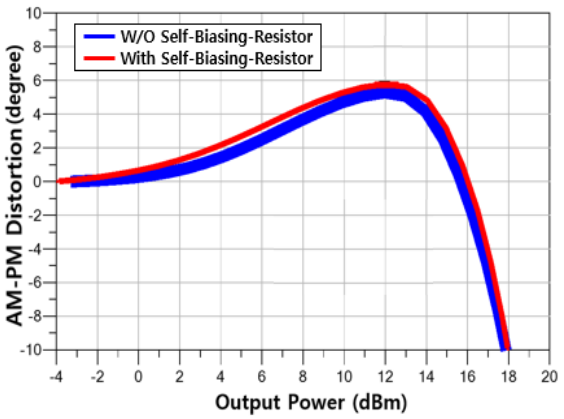


Fig. 8. Inter-cascode voltage V_X.

C. Simulation results



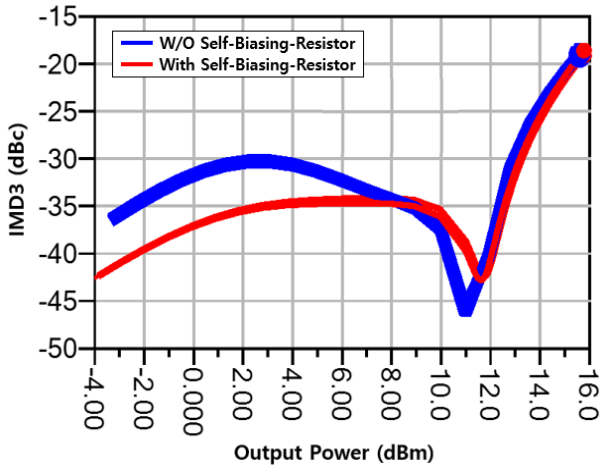
(a)



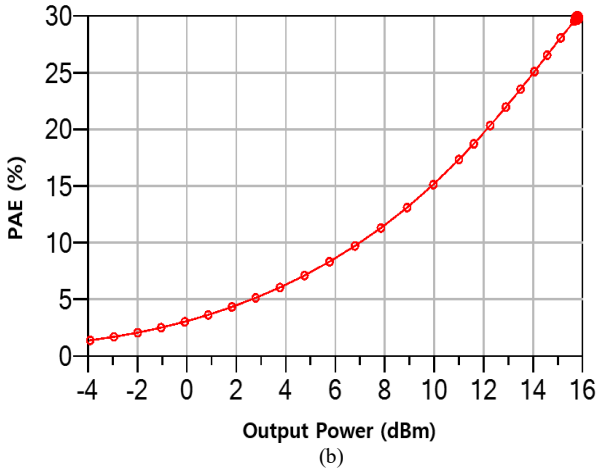
(b)

Fig. 9. 1-tone simulation results of (a)AM-AM and (b) AM-PM.

Figure 9 shows the AM-AM and AM-PM distortion results confirmed by a 28GHz 1-tone simulation of the proposed power amplifier. It can be seen that the AM-AM distortion is improved when the SBR technique is used.



(a)



(b)

Fig. 10. 2-tone simulation results of (a)IMD3 and (b)PAE.

As shown in Figure 10, a power added efficiency (PAE) of 22.64% at an output power of 13.1 dBm based on IMD3 -30dBc was confirmed using a 2-tone simulation with a center frequency of 28 GHz and a tone spacing of 160MHz.

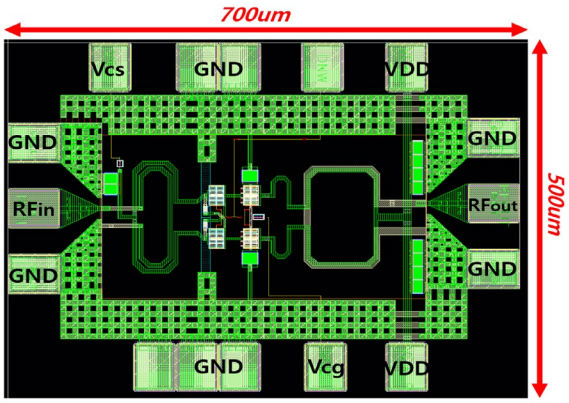


Fig. 11. Proposed CMOS Power Amplifier layout

TABLE I.
COMPARISON WITH RECENTLY REPORTED CMOS POWER AMPLIFIERS

Reference	Frequency (GHz)	CS / CG TR Gate width (um)	V_{DD} (V)	Psat (dBm)	P_{linear} (dBm)	Linear PAE (%)	Config.	Process
2021 Wonho Lee	28	192 / 192	2.4	19.1	11.9	16.8	DCC, BCI	65nm
2016 ISSCC S.Shakib	30	384 / -	1.15	15.3	5.3	9.6	CS	28nm
2017 RFIC Yang Zhang	27	178 / -	1	18.1	8.4	8.8	CS	40nm
2019 MWCL Seungkyeong Lee	28	112*4 / 112*4	2.2	18.5	7.5	6.2	PCC	65nm
This Work (Simulated)	**28**	**256 / 256**	**2.4**	**19.6**	**13.1**	**22.6**	**Self Biasing Resistor**	**65nm**

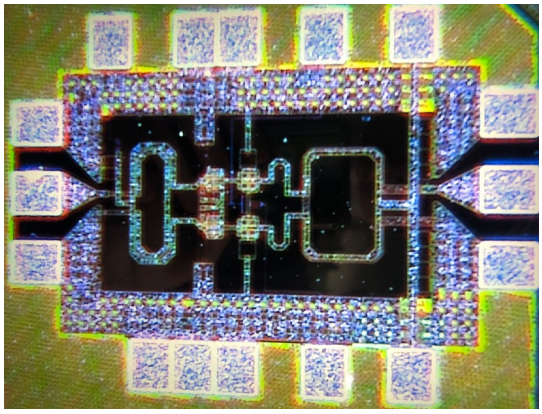


Fig. 12. Microphotograph of the proposed CMOS PA.

When using the SBR technique, we confirmed that linearity was improved. Detailed simulation results and comparison tables are given in Table 1. Figure 11 shows the proposed CMOS power amplifier layout and Figure 12 is a microphotograph of the proposed CMOS power amplifier.

III. CONCLUSION

In this paper, we propose a CMOS power amplifier using the SBR technique. It operates at a frequency of 28GHz and has a supply voltage of 2.4V. As a result of the simulation, a saturated output power of 19.6dBm and a peak PAE of 37.49% are obtained. Additionally, AM-AM distortion has been improved to achieve a linear output power of 13.1dBm at IMD -30dBc, and 22.6% PAE at that output power.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

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