Application of Current Mode Signal Processing: ADC

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***Abstract* - In this paper, a low power current mode 12-bit ADC (Analog to Digital Converter) is proposed to mix digital circuits and analog circuits with the advantages of low power consumption and high speed operation. The proposed 12 bit ADC is implemented by using 4-bit ADC in a cascade structure, so its power consumption can be reduced, and the chip area can be reduced by using a conversion current transfer circuit. Error of the reference current, which is caused by the current mismatch in the reference current transfer and the conversion current transfer is about 4.19 μA. The proposed 12-bit ADC is implemented with SK Hynix 350nm 5metal 1poly process, and post-layout simulation is performed using Cadence MMSIM. It operates at a supply voltage of 3.3V and the area of the proposed circuit is 318µm × 514µm. In addition, the ADC shows the possibility of operating with low power consumption of 3.4mW average power consumption in this paper.**

***Keywords*— ADC, Cascade structure, Current-mode, Low power consumption, Voltage swing**

I. INTRODUCTION

Conventional processors use digital circuits to process signals. However, when the digital circuit is used, the dynamic power consumption increases in proportion to the frequency as shown in Equation (1).

$$P_D = \alpha f C {V_{DD}}^2 \quad (1)$$

Therefore, unlike conventional processors, we can replace the digital circuit with an analog circuit, which can operate with a lower power consumption. As a result, power consumption can be reduced as a combined analog and digital processor [1]-[2]. The merging of the two circuits also increases the processor's performance by using the digital circuit in the part of the processor where the digital circuit is most efficient and using the analog circuit in the part of the processor where the analog circuit is most efficient.

Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are essential to selectively use the advantages of analog and digital. However, the power consumption of previous ADC technologies is about hundreds to thousands of mW [3]-[4], which can be very expensive due to the high cost of designing new processor architectures [5]. At high cost, high-consumption ADCs can limit the number of ADCs required for a processor architecture, limiting the need for low-power operation to other circuitry in the chip. Therefore, in this paper, we propose a current-mode 12-bit ADC that significantly reduces power consumption by connecting 4-bit ADCs in cascade.

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II. LOW POWER CIRCUIT IMPLEMENTATION

A. Possibility of Low Power Operation in Current Mode Circuits

The power consumption in a CMOS circuit may be divided into dynamic power generated by a transition signal of the circuit and static power, which is the power consumption when the signal of the circuit is a stationary signal. Therefore, low power circuits can be designed in two aspects to reduce the power consumption of analog circuits, dynamic power and static power.

When the input signal changes with time, the instantaneous voltage is as shown in equation (2), so the rate of change of the instantaneous voltage with time is as shown in equation (3).

$$V_{out}(t) = V_\infty - (V_\infty - V_{0+})e^{-\frac{t}{RC}} \quad (2)$$

$$\frac{dV_{out}(t)}{dt} = \frac{1}{RC}(V_\infty - V_{0+})e^{-\frac{t}{RC}} \quad (3)$$

The voltage V_{0+} represents the initial voltage, and V_∞ represents the voltage after the change.

At this time, since the instantaneous power is the product of V_{DD} and the instantaneous current, Equation (4) is obtained.

$$P(t) = CV_{DD}\frac{dV_{out}(t)}{dt} = \frac{1}{R}V_{DD}(V_\infty - V_{0+})e^{-\frac{t}{RC}} \quad (4)$$

Therefore, the average power during the changed time T is given by Equation (5).

$$P_{avg} = \frac{CV_{DD}(V_\infty - V_{0+})}{T}\left(1 - e^{-\frac{t}{RC}}\right) \quad (5)$$

This represents dynamic power since it is consumed when the transition signal occurs. Therefore, in order to reduce power consumption at a given power supply voltage V_{DD}, the channel width of the CMOS transistor should be shortened to reduce the value of the capacitor (C), or the difference between the initial voltage V_{0+} and the voltage V_{∞}, which is the voltage swing, should be reduced.

This paper aims to design a small dynamic power by adjusting the voltage variation instead of reducing the value of capacitor (C).

The analog signal is divided into a voltage mode signal and a current mode signal. When the current signal in the saturation region of the MOSFET transistor is used, the voltage swing can be lower than that of the voltage signal [6]. This is because the voltage in the saturation region $V_{OV} = V_{GS} - V_T$ has a property proportional to the square root of the current as shown in Equation (6).

$$V_{GS} - V_T = \sqrt{\frac{2i_D}{k_{n,p}}} \quad \left(k_{n,p} = \mu_{n,p} C_{ox} \frac{W}{L}\right) \tag{6}$$

For example, in the case of an N-bit voltage mode ADC, when the input signal $x \cdot V_{LSB} (0 \le x < 2^N)$ changes to $(x + \Delta x) \cdot V_{LSB}$, the voltage swing is shown in Equation (7).

$$V_{\infty} - V_{0+} = \{(x + \Delta x) - x\} V_{LSB} = \Delta x \cdot V_{LSB} \tag{7}$$

Here, because V_{LSB} is a constant, the voltage swing is proportional to Δx.

On the other hand, in the case of the current mode N-bit ADC, when the input signal changes from $x \cdot I_{LSB}$ to another current $(x + \Delta x) \cdot I_{LSB}$, the initial voltage V_{0+} of the voltage V_{OV} may be $\sqrt{\frac{2xI_{LSB}}{k_{n,p}}}$, and the voltage V_{∞} after the change may be represented by $\sqrt{\frac{2(x+\Delta x)I_{LSB}}{k_{n,p}}}$. Therefore, in the current mode ADC, the voltage swing can be expressed as Equation (8).

$$V_{\infty} - V_{0+} = \sqrt{\frac{2I_{LSB}}{k_{n,p}}} \left(\sqrt{x + \Delta x} - \sqrt{x}\right) \tag{8}$$

At this time, since $\sqrt{\frac{2I_{LSB}}{k_{n,p}}}$ and x are constants with respect to Δx, the voltage swing is proportional to the parallel movement of the square root of Δx by $-x$ on the Δx axis and $-\sqrt{x}$ on the voltage swing axis.

Figure 1 is a graph showing the voltage swing according to the signal change of voltage mode and current mode ADC. In voltage mode ADCs, the maximum voltage change is V_{ref}. In current mode ADCs, the maximum voltage change is $\sqrt{\frac{2I_{ref}}{k_{n,p}}}$. In general, the maximum voltage V_{ref} of the voltage mode ADC is V_{DD}, so the maximum voltage swing in the voltage mode corresponds to several V [7]. The maximum voltage swing in the current mode with $50\mu A$ of I_{ref} corresponds to several tens of mV assuming that the electron mobility μ_n is $480\,\mathrm{cm}^2/V \cdot s$, the hole mobility μ_p is $1350\,\mathrm{cm}^2/V \cdot s$, oxide capacitance C_{ox} is $8.6 \times 10^{-3} F/m^2$, and $\frac{W}{L} = \frac{10\mu m}{0.35\mu m}$ [8].

Therefore, since the voltage swing is smaller in the current mode ADC than in the voltage mode ADC, the use of the current mode signal increases the possibility of low power.

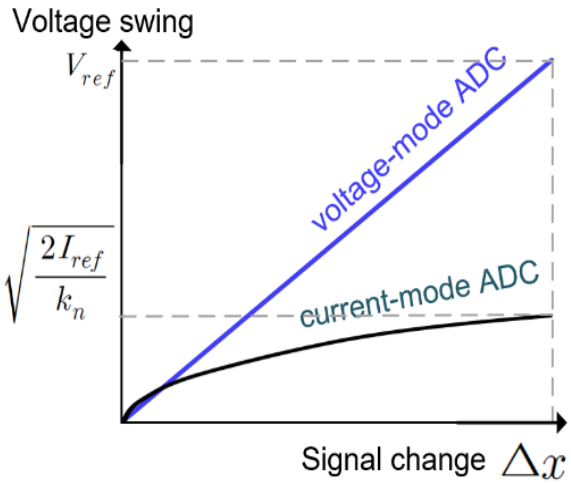


Fig. 1. Voltage swing of voltage-mode ADC and current-mode ADC at different input signals $(x \rightarrow x + \Delta x)$

B. Current Mode Power Consumption Evaluation

The power consumption of the current mode ADC can be determined by inputting the maximum static current I_{ref} to the current mode ADC and comparing the sum of the static powers of a certain pattern. Figure 2 shows the circuit block diagram at the k-th bit of a typical current mode ADC [9]-[10]. $I_{i,k}$ represents the analog input current at the k-th bit, and $I_{ref,k}$ represents the reference current of the k-th bit. The comparison stage compares the current input from the k-th bit with the reference current of the k-th bit and outputs a digital operation result. The calculation stage receives the digital output from the comparison stage and enables the next comparison stage to be performed.

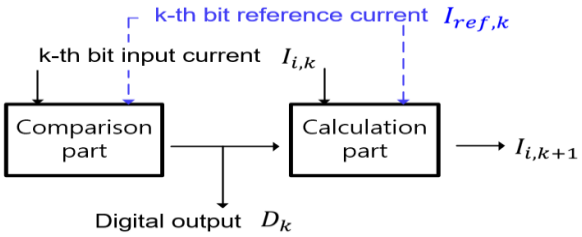


Fig. 2. Block diagram of k-th bit at basic current-mode ADC

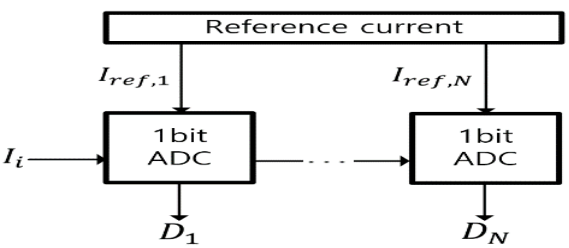


Fig. 3. Circuit block diagram of basic current-mode N-bit ADC

Figure 3 shows a circuit block diagram of a typical current mode *N*-bit ADC [10]. The 1-bit ADC in Figure 2 is cascade-connected. The current output from one bit of the calculation stage becomes the input current of the next 1-bit ADC, and the total *N*-bit digital output is determined sequentially

In this ADC, there are two main blocks to consider static power consumption: a comparison stage comparing input current and reference current, and a calculation stage calculating a current signal to convert the next bit. The power consumption due to the input current is excluded from the power consumption calculation because the input current is very small. In addition, the bias current input to the current source to supply the reference current is also excluded from the calculation of power consumption because it is a very small amount of current. Therefore, the criterion for determining power consumption is defined as 'SP_{max}', and the expression can be expressed as shown in Equation (9).

$$SP_{max} = P_{comparison} + P_{calculation} \tag{9}$$

The power of the *k*-th comparison stage is the part comparing the *k*-th input current and the *k*-th reference current, so it is expressed as the product of the *k*-th reference current $I_{ref,k}$ and the power supply voltage V_{DD}. And the power consumption of the *k*-th calculation part can be defined as the product of the *k*-th input current $I_{i,k}$ and V_{DD}, because there is a *k*-th output current, which is the *k+1* -th input current. Therefore SP_{max} can be expressed like Equation (10). SP_{max} is used to determine the power consumption of the current-mode ADC.

$$SP_{max} = V_{DD}\left(\sum_{k=1}^{N} I_{ref,k} + \sum_{k=1}^{N} I_{i,k}\Big|_{I_i=I_{ref}}\right) \tag{10}$$

III. LOW-POWER CURRENT-MODE 12-BIT ADC DESIGN

A. ADC Reference Current Setting

In the comparison stage of the current mode ADC proposed in this study, the reference current is compared with the input current and output as digital 0 or 1, so the reference current must be set separately. In the *N*-bit ADC, the reference current of the *k*-th bit can be expressed as shown in Equation (11).

$$I_{ref,k} = \frac{1}{2^k} I_{ref} \quad (k = 1, 2, \dots, N) \tag{11}$$

Figure 4 shows the circuit design of "reference current transfer" of the *N*-bit ADC using a cascode PMOS current mirror. The bias current I_{BIAS} is the current input to supply the reference current of each bit operation.

The channel width of the reference current doubles each time the bit approaches MSB, as shown in Figure 4, so as the resolution of the ADC increases, the channel width that sets the reference current increases exponentially. This will occupy a considerable area.

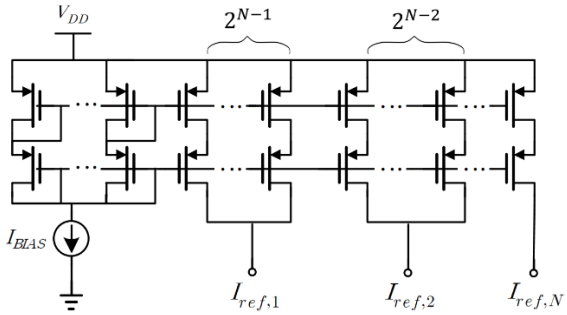


Fig. 4. Reference current transfer of *N*-bit ADC (cascode PMOS current mirror)

Figure 5 shows the "conversion current transfer" used to improve this. After a certain bit, the area can be reduced by resetting the channel width.

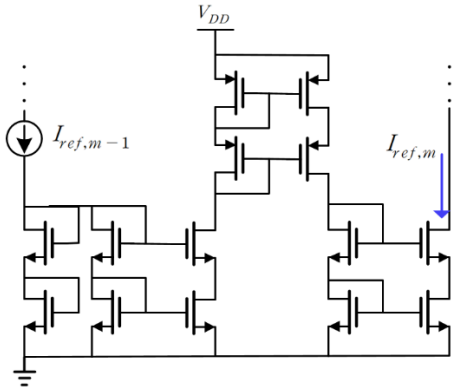


Fig. 5. Conversion current transfer

In this paper, three reference current transfers and two conversion current transfers are used to set the reference current of the 12-bit ADC.

B. Current Mode ADC Operation and Algorithm

Figure 6 shows the operation of the proposed current mode 12-bit ADC. When four digital data are output after going through the comparison stage in one stage 4-bit ADC, current is obtained by subtracting the reference current according to the digital output of each bit from the input current of that stage through the resetting current part $I_i - \left(D_1 I_{ref1} + D_2 I_{ref2} + D_3 I_{ref3} + D_4 I_{ref4}\right)$, which is the input current of the next 4-bit ADC.

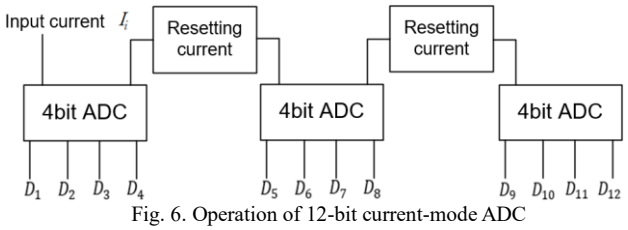


Fig. 6. Operation of 12-bit current-mode ADC

Figure 7 is the proposed 4-bit ADC circuit. I_i is compared with $\frac{1}{2} I_{ref}$ and if I_i is bigger, then the digital output D_1 is 1. In the next bit, D_1 is received as the input

for the NMOS acting as a switch, and I_i is compared with $\frac{1}{2}I_{ref}+\frac{1}{2^2}I_{ref}$ and if I_i is smaller, then D_2 becomes 0. Likewise, the next bit receives D_1 and D_2 as inputs for switches and I_i and $\frac{1}{2}I_{ref}+\frac{1}{2^3}I_{ref}$ is compared. In this way, at the k-th bit, the input current is represented by equation (12) and the reference current is expressed by equation (13).

$$I_{i,k} = I_i \tag{12}$$

$$I_{ref,k} = \frac{1}{2^k}I_{ref} + \sum_{m=2}^{k} D_{m-1}\cdot\frac{1}{2^{m-1}}I_{ref} \tag{13}$$

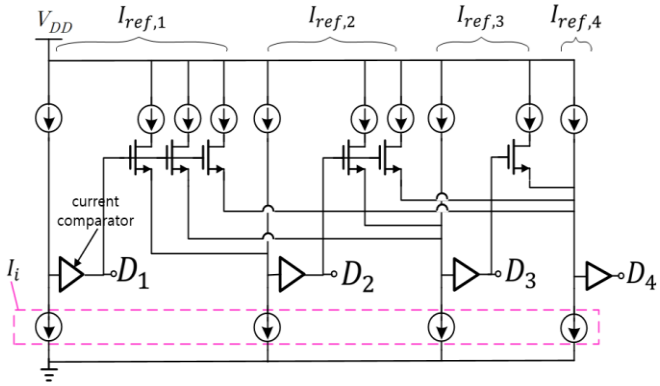


Fig. 7. Circuit diagram of 4-bit ADC

C. Low-Power Design of Current-Mode ADC

In the proposed 4-bit ADC, the input current does not change, only the reference current changes, so no calculation stage is required. Therefore, static power consumption of the first 4-bit ADC, $SP_{max,4b}$, can be expressed as shown in Equation (14).

$$SP_{max,4b} = \sum_{k=1}^{i}\left(\frac{1}{2^k}+\frac{1}{2^{k-1}}+\frac{1}{2^{k-2}}+\cdots+\frac{1}{2}\right)I_{ref}V_{DD}$$
$$= \left(4+\frac{1}{2^4}-1\right)V_{DD}I_{ref} \tag{14}$$

In the second 4-bit ADC, the analog maximum input current $(I_{i,4})$ is $\frac{1}{2^4}$ times I_{ref}, so the static power consumption of the second 4-bit ADC is reduced to $\frac{1}{2^4}$ times that of the first 4-bit ADC. Similarly, the third 4-bit ADC is also significantly reduced by $\frac{1}{2^8}$.

The resetting current part for resetting the input current corresponds to the calculation stage for converting to the input current of the next 4-bit ADC. These operations are only necessary when changing from 4 bits to 5 bits and from 8 bits to 9 bits. Therefore, $P_{calculation}$ (power consumption of resetting current) can be expressed as in Equation (15).

$$P_{calculation} = V_{DD}(I_i + I_{i,4}) \tag{15}$$

In this case, I_i is I_{ref} as the maximum input current of the first 4-bit ADC and $I_{i,4}$ is $\frac{1}{2^4}$ times the I_{ref} as the maximum input current of the second 4-bit ADC. SP_{max} of this algorithm can be expressed as Equation (16).

$$SP_{max} = \left(4+\frac{1}{2^4}-1\right)\left(I_{ref}+\frac{1}{2^4}I_{ref}+\frac{1}{2^8}I_{ref}\right)V_{DD} + \left(I_{ref}+\frac{1}{2^4}I_{ref}\right)V_{DD} = 4.33V_{DD}I_{ref} \tag{16}$$

If the digital output is made through 12 comparison stages without using the resetting current part of the proposed circuit, SP_{max} of this algorithm is expressed by Equation (17).

$$SP_{max} = \sum_{k=1}^{12}\left(\frac{1}{2^k}+\frac{1}{2^{k-1}}+\frac{1}{2^{k-2}}+\cdots+\frac{1}{2}\right)I_{ref}V_{DD}$$
$$= \left(12+\frac{1}{2^{12}}-1\right)V_{DD}I_{ref} = 11.00V_{DD}I_{ref} \tag{17}$$

We can see from Equation (16) and Equation (17), because the 4-bit ADC is cascaded, the power consumption is reduced.

IV. RESULTS AND DISCUSSIONS

In this paper, we implemented a current mode 12-bit ADC using MagnaChip / SK Hynix 350nm process and analyzed its performance through post-layout simulation using Cadence MMSIM.

Figure 8 shows the layout of a current-mode 12-bit ADC. The proposed ADC operates at 3.3V of supply voltage, occupying an area of $318\mu m \times 514\mu m$.

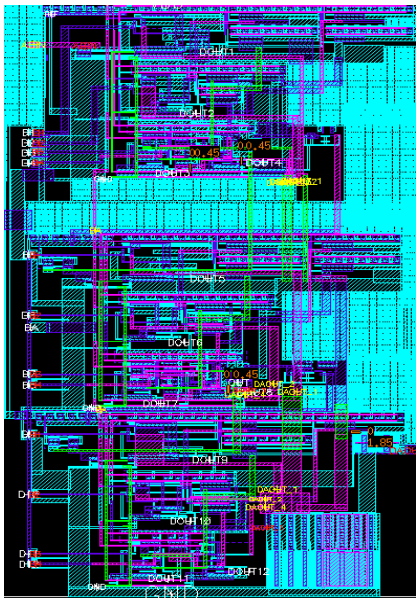
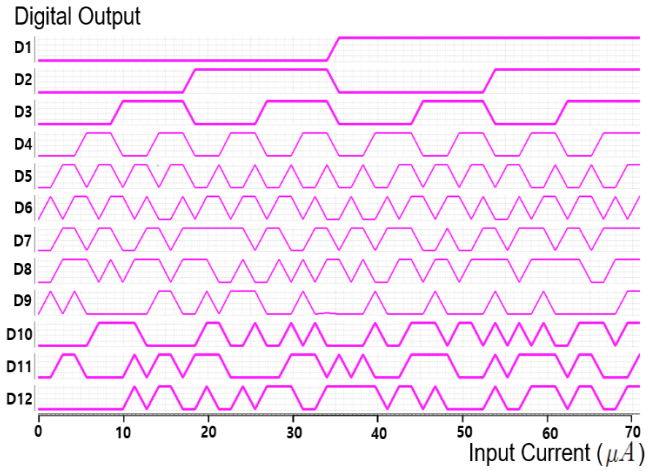


Fig. 8. Layout of 12-bit ADC ($318\mu m$ x $514\mu m$)

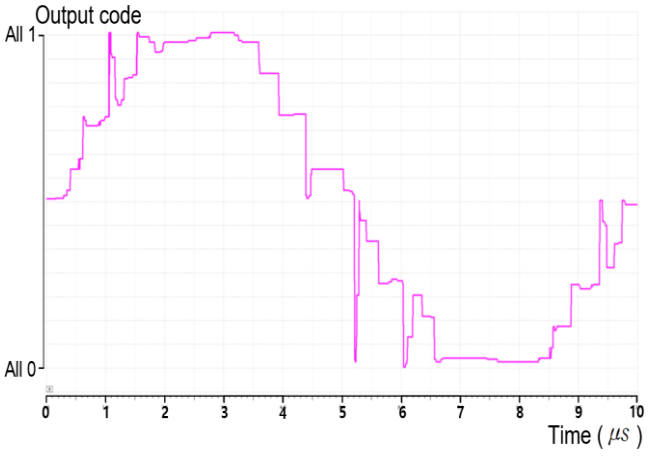
Figure 9(a) shows the post simulation of the digital $(D_1 \sim D_{12})$ output according to the input current. Figure 9(b) shows the post simulation of the output code when sine wave input is $\frac{I_{ref}}{2}\sin\omega t + \frac{I_{ref}}{2}(f = 100kHz)$.

Table 1 shows chip test results of the error between ideal reference current and actual reference current of the current mode 12bit ADC from 1bit to 12bit. In this paper, the ideal reference current I_{ref} of the ADC is $70.75\mu A$. However, due to the current mismatch in the reference current transfer and the conversion current transfer, the reference current I_{ref} has an error of $4.19\ \mu A$.

Figure 10 shows chip test result of output code at different input currents. The red dotted line in the figure represents an ideal ADC with no quantization error with I_{ref} as $70.75\ \mu A$. The chip test results show that a metastable phenomenon occurs, in which the digital code is not determined to be 0 or 1. Due to the characteristics of the proposed circuit, this phenomenon can cause errors in linearity because the digital output is the input to the calculation stage. For the samples with metastable errors, a small voltage was considered as 0 and a large voltage as 1 based on whether the voltage is greater than or less than $\frac{V_{DD}}{2}$.



(a)



(b)

Fig. 9. Post-Layout (a) DC Simulation of digital output (b) output code transition simulation (sine input $f = 100$kHz)

TABLE I. Chip reference current of 12-bit ADC

BIT	Ideal Reference current (μA)	Actual Reference current (μA)	Error (μA)
1	35.375	31.3534	-4.0216
2	17.6875	20.8020	3.1145
3	8.8438	11.7043	2.8605
4	4.4219	4.8346	0.4127
5	2.2109	3.4762	1.2653
6	1.1055	1.4737	0.3682
7	0.5527	0.8246	0.2718
8	0.2764	0.3283	0.0520
9	0.1382	0.0607	-0.0755
10	0.0691	0.0301	-0.039
11	0.0345	0.0175	-0.017
12	0.0173	0.0125	-0.0047

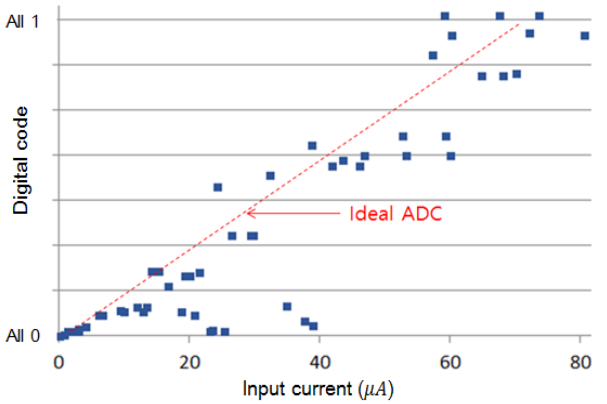


Fig. 10. Chip test result of proposed ADC at different input currents (number of samples : 52)

Figure 11 shows the post-layout DC simulation results of power consumption according to the input current. The average power consumption was 3.4mW. According to the SP_{max} that was introduced in this paper as a criterion for determining the power consumption, the power consumption of the ADC is proportional to the reference current I_{ref}. Therefore if I_{ref} is lower, then the circuit can operate with less power.

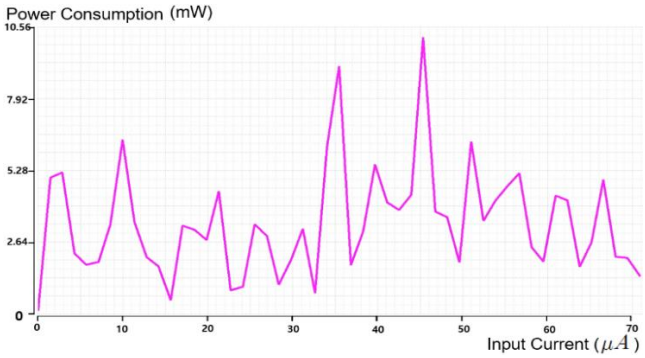


Fig. 11. Post-Layout DC Simulation result of power consumption at different input currents

V. CONCLUSION

Processors implemented with digital circuits have a problem in that power consumption increases as operating frequencies increase. Thus, a processor structure using digital circuits and analog circuits may be a method for enabling low-power operation. Therefore, low power consumption operation of ADC, the boundary between analog and digital, is very important. Accuracy is also an important specification for ADCs. Therefore, it is important to ensure that the error in linearity is low.

In this paper, it is shown that the use of current mode signal is more suitable for low power design than the use of voltage mode signal. The proposed 12-bit ADC is implemented by Magnachip / SK Hynix 350nm process and post-layout simulation is performed using Cadence MMSIM to analyze the performance of ADC. It operates at 3.3V power supply, occupies an area of $318\mu m \times 514\mu m$. The chip test results show that there is an error in linearity due to metastability. However, the proposed 12-bit ADC shows the possibility of operating with low power consumption of 3.4mW on average. The proposed low power ADC is expected to contribute to the fabrication of low power processors in the future.

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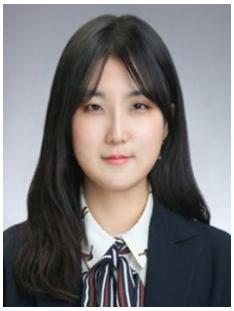

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