Design of 1:1 Transformer based 2-Stage Differential Low-noise Amplifier for W-band Radar

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***Abstract* - This paper introduces a 77-81 GHz CMOS low-noise amplifier (LNA) designed for FMCW radar applications, with the goal of achieving high gain and low noise figure. To attain these objectives, a two-stage differential common-source (CS) structure is adopted, and neutralization capacitors are employed in each stage to obtain high gain. The proposed LNA is implemented in bulk CMOS 65nm process, providing a gain of over 17 dB and a noise figure of less than 4.5 dB in the frequency range of 77-81 GHz. The chip size, including pads, is 0.69 µm × 0.39 µm.**

***Keywords*—5G, CMOS, Low noise amplifier, Neutralization capacitor**

I. INTRODUCTION

The millimeter-wave radar system stands as a pivotal technology for future control systems. In comparison to sensors based on infrared or lasers, the most notable advantage of millimeter-wave radar lies in its exceptional performance under adverse weather conditions. Therefore, millimeter-wave radar is being introduced for applications such as vehicle radar and short-range sensor systems for drones. The key to the successful commercialization of millimeter-wave radar systems lies in securing essential components in the W-band [1].

Receivers operating in the W-band face challenges, as they exhibit relatively insufficient gain from a single transistor compared to the Ku or Ka bands and are susceptible to noise figure. Moreover, among the components in the receiver configuration, low-noise amplifiers (LNAs) play a critical role, being connected immediately after the antenna and determining the overall reception performance [2][3]. Hence, high-performance LNAs are imperative. To address this, conventional designs have focused on multi-stage LNAs with high gain. However, due to the multi-stage configuration, achieving high gain leads to increased noise figure, resulting in a trade-off. To resolve these issues, this paper proposes the design of a 2-stage differential structure CS LNA with high gain and low noise figure.

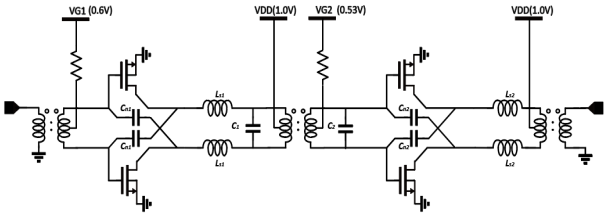
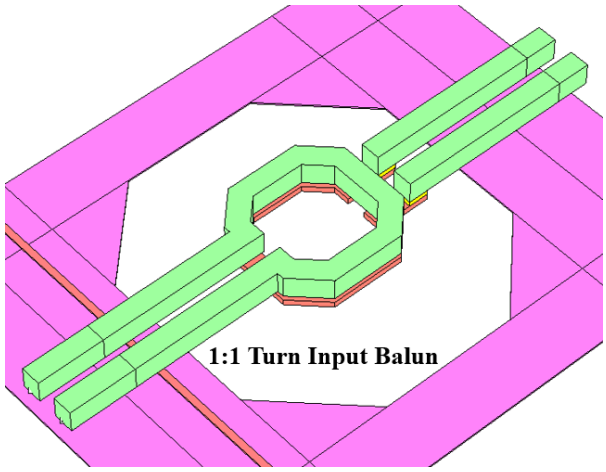
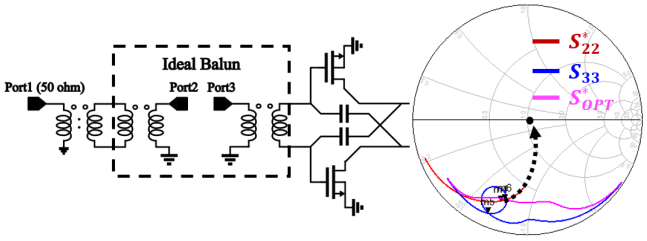


Fig. 1. Schematic diagram of the designed LNA



(a)



(b)

Fig. 2. (a) The layout of the 1:1 Turn transformer used in the input stage. (b) Design methodology for achieving input matching and minimum noise figure

This is achieved by incorporating neutralization capacitors for high gain and optimizing the structure of the input balun.

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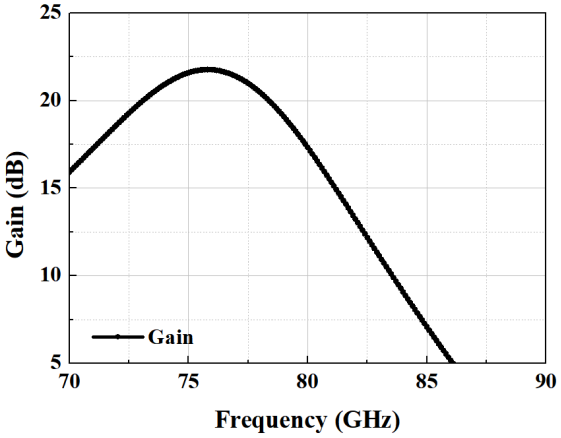

Fig. 3. Post-layout simulation result of S21 for the 2-stage LNA.

The goal is to design an LNA that balances high gain with low noise figure in the W-band.

II. DESIGN OF 2-STAGE DIFFERENTIAL LNA

Figure 1 illustrates the circuit diagram of the 2-stage differential CS LNA proposed in this paper. The use of a differential structure, employed for achieving high gain, requires the use of an input transformer, typically leading to compromises in noise figure. Particularly in the strongly

linear W band, noise figure can further increase [4]. To minimize this effect, this paper optimizes the input transformer by configuring it as a 1:1 Turn, as shown in Figure 2, to mitigate noise figure. The LNA features a specific source optimum point on the transistor to minimize noise, exhibiting the minimum noise when matched to the input port (50 ohms). Additionally, for optimal matching, the input impedance of the transistor gate should also be matched to 50 ohms. To achieve this, as shown in Figure 2 (b), the transistor and surrounding components were arranged to place the gate's input impedance S_{33} and S_{OPT}^{*} at the same location. The transformer's S_{22}, S_{33}^{*}, and S_{OPT}^{*} were matched to achieve input matching and noise figure optimization.

Furthermore, by adopting a differential structure, this paper leverages neutralization capacitors to obtain high gain in the W band, where a single transistor may lack sufficient gain. The input transformer enables broadband matching. Consequently, the designed LNA in this paper achieves high gain, broadband matching, and low noise figure with a simple configuration. Considering the significant impact of parasitic capacitance in the W band, EM simulations were conducted to account for this, and the results were reflected in the post-layout simulations.

III. SIMULATION AND MEASUREMENT RESULTS

Figures 3 through 6 present the post-layout simulation results incorporating electromagnetic (EM) simulations, while Figures 8 through 12 illustrate the measured results of the LNA that was actually fabricated.

Figure 3 presents the simulated S21. The maximum gain is 23.2 dB and minimum gain is 21.7 dB between 76.9 and 80.7 GHz. Figure 4 and 5 shows the simulated input and output reflection coefficients. S11 is lower than -10 dB between 76.9 and 80.7 GHz for the LNA. The noise figure of the LNA is shown in Figure 6. The minimum noise figure is 4.48 dB at 77 GHz in simulation.

The LNA fabricated in TSMC 65 nm CMOS technology. Figure 7 shows the chip microphotograph. The overall chip area is $0.69 \times 0.39\ mm^2$. The LNA consumes 45 mW from a 1 V supply. The measured S-parameters are shown in Figure 8 to 10. The measured gain (S21) with correct bias current achieves a maximum value of 23.1 dB at 77 GHz, and minimum value of 21.7 dB at 80.7 GHz. In this frequency range, the measured input return loss (S11) is less than -10 dB, the measured output return loss (S22) is less than -10 dB. The simulation in general agrees well with the measured results. Figure 11 shows the simulation and measurement result graphs of gain and noise figure. The measurement results exhibit a similar trend to the simulation results, with a slight shift in the actual chip compared to the EM simulation, attributed to the inclusion of a small parasitic capacitance component. Figure 12 illustrates the measured IP1dB results at 78 GHz. An IP1dB of -22.46 dBm was observed at 78 GHz, showing a value similar to the simulation. Table I at the bottom provides the recorded IP1dB for each frequency.

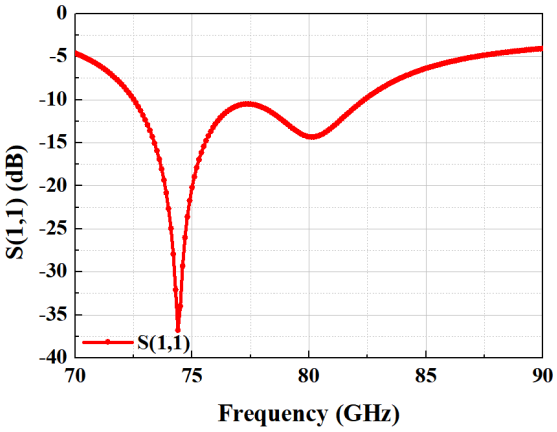

Fig. 4. Post-layout simulation result of S11 for the 2-stage LNA.

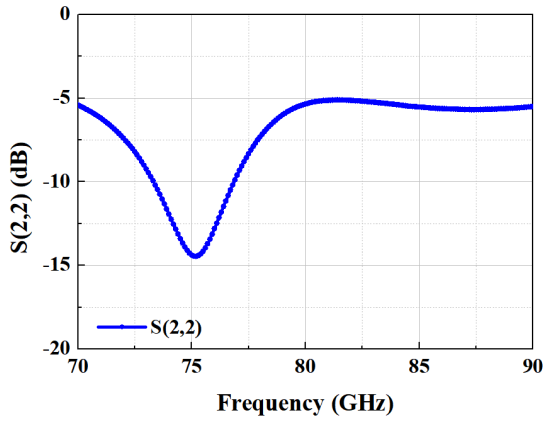

Fig. 5. Post-layout simulation result of S22 for the 2-stage LNA.

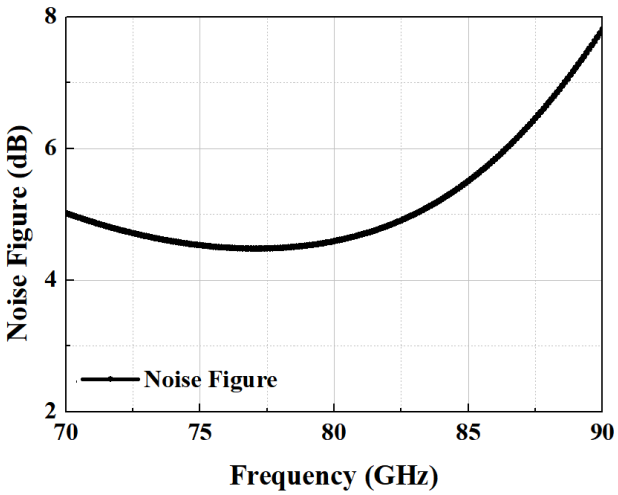

Fig. 6. Post-layout simulation result of noise figure for the 2-stage LNA.

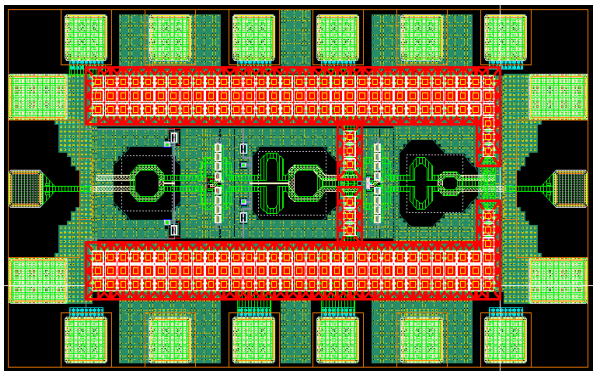

Fig. 7. Chip micrograph.

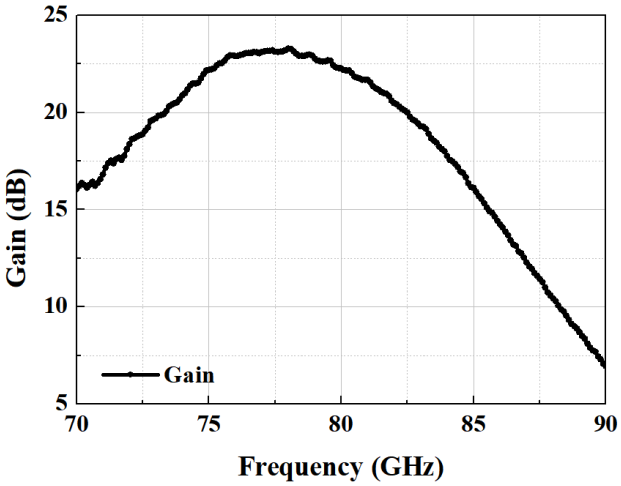

Fig. 8. Measured results of S21 with correct bias current for the 2-stage LNA.

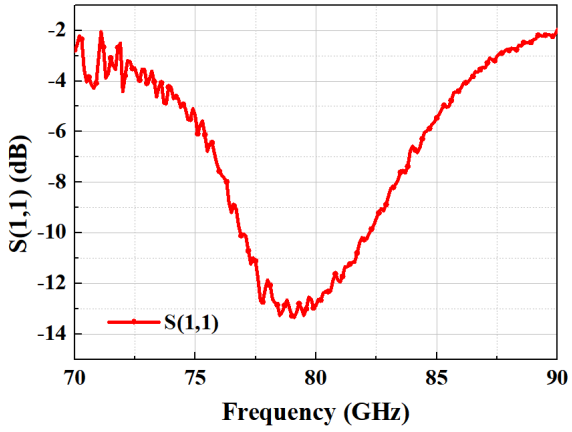

Fig. 9. Measured results of S11 for the 2-stage LNA.

Table II presents a comparison with other reported Low noise amplifier in W-band.

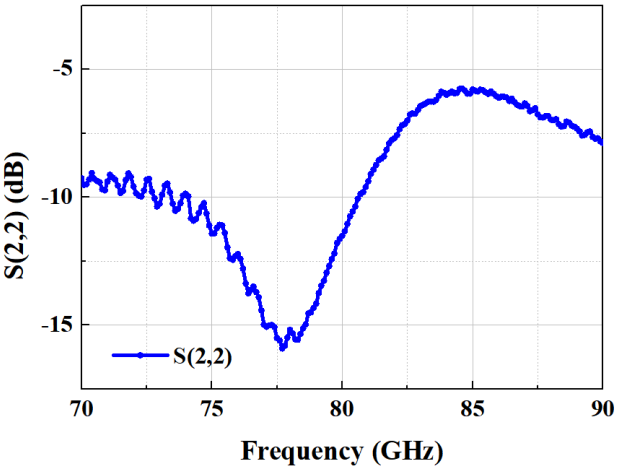

Fig. 10. Measured results of S22 for the 2-stage LNA.

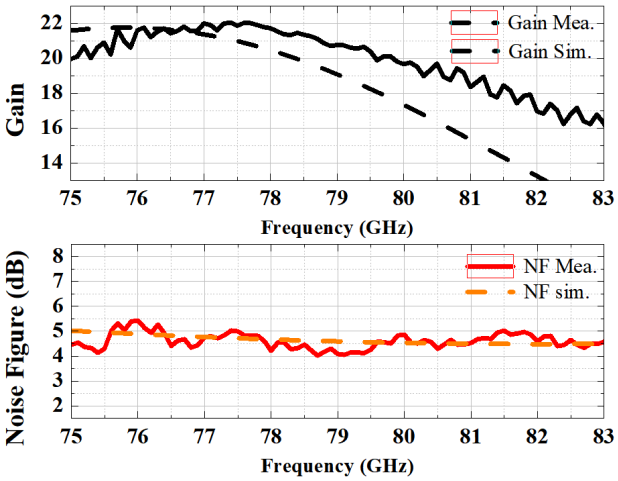

Fig. 11. Measured results of noise figure for the 2-stage LNA.

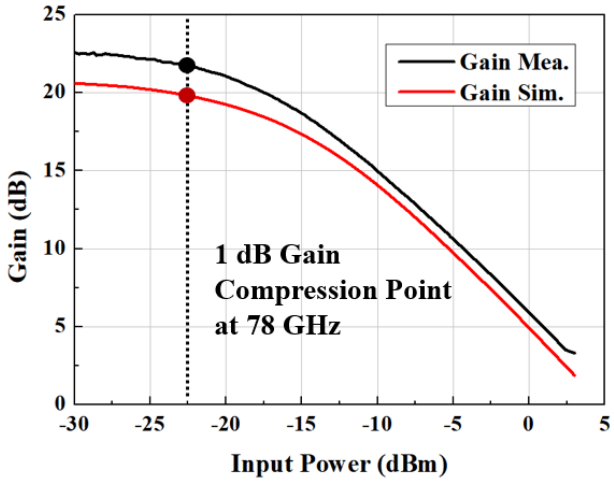

Fig. 12. Measured results of P1dB for the 2-stage LNA.

TABLE I. The measured results of IP1dB for the proposed LNA at various frequencies.

Frequency [GHz]	IP1dB [dBm]
76	-20.18
77	-21.32
78	-22.46
79	-22.08
80	-23.03
81	-22.65
82	-22.08
83	-22.46

TABLE II. Comparison of the proposed LNA with the reported W-band CMOS LNAs.

	This work	[5]	[6]	[7]
Tech (nm)	65	28	65	65
Freq (GHz)	79	86	75	100
Gain (dB)	21	25	14.2	16.4
BW_{3dB} (GHz)	7.7	10	30	21.5
Min. NF (dB)	4.3	6	6.3	6.8
IP1dB (dBm)	-23	-32	-10	N/A
Topology	2Stage	5Stage	2Stage	5Stage

IV. CONCLUSION

In this paper, a W-band 2-stage differential low-noise amplifier was designed using the TSMC 65nm process. The designed low-noise amplifier achieved broadband matching and low noise indices by employing a 1:1 Turn transformer. Additionally, high gain was achieved by applying neutralization capacitors to each stage.

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