A Microscale Neural Implant ASIC for Scalable Multichannel Brain-Machine Interface

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***Abstract* – The Brain-Machine Interface (BMI) is a pivotal tool for the study and repair of the nervous system, facilitating connections between the brain and external devices. The implementation of a flexible and adaptable multichannel system is essential for effective communication and analysis of a large number of neurons in the anatomically and physiologically complex human nervous system. This paper presents the development of a wireless stimulation and recording ASIC, fundamental for creating a modular BMI system with multiple modules. Simulations reveal the on-chip antenna's peak efficiency at the target frequency within a streamlined design. The inclusive wireless power system, featuring the resonant tank, rectifier, and LDOs, delivers a 1.2 V supply voltage, allocating 22.56 µW to the recording subsystem, while providing 9.7 µW and 2.1 mW to resting and active stimulators, respectively. The spike detection front-end, utilizing an energy operator, conveys data via backscatter communication, and the stimulation back-end executes 8-channel biphasic current stimulation, marking a notable stride in the evolution of flexible and adaptive BMI technology.**

***Keywords* - mm-sized distributed implants, wireless power transmission, neural recording, neural stimulation**

I. INTRODUCTION

Brain-Machine Interface (BMI) has been studied with the expectation that it would open a new way of communication by connecting the human brain and external machines. Clinical studies confirmed the possibility of patients controlling the device using brain signals to some extent [1], [2], and studies to improve the inconvenience of the existing wired system and brain signal analysis algorithms continued. However, many deficiencies still exist in implementing high spatial resolution recording and bidirectional interactions in neural interfaces. It is well known that the number of input and output channels enhances the quality of the interpretation. Despite the advance in highly integrated microelectrode fabrication, there is a limit to increasing spatial resolution and dealing with broad brain cortex areas. Although electroencephalography (EEG) analyzes brain signals in a large area in a complex way, it is clear that the spatial resolution is lower than that of invasive devices. To go beyond simply receiving signals from the motor cortex and intuitively interpreting them, it is necessary to capture the user's intentions so that the user can handle the machine in a more flexible and human-like way. Therefore, a system that can receive signals from a broad, scalable area and provide stimulus feedback is required.

Recent research on the distributed microscale wireless device design showed possible solutions [3]–[5]. The system achieves scalability by adopting a distributed configuration of numerous sub-mm size miniature devices that are completely wireless and operate independently. This approach is achieved through low-power complementary metal-oxide-semiconductor (CMOS) fabrication with stable wireless power transmission, which encodes downlink data into carrier frequencies and transmits uplink data in a backscattering manner. Various energy transfer methods based on light, ultrasound, and magnetic coupling have been studied, and among them, wireless power supply through RF (Radio Frequency) electromagnetic waves are representative [6]–[9].

With advances in high channel count and wireless operation, however, the simultaneous task of recording and stimulating is still challenging. Our work focuses on acquiring brain activity from distributed multiple sites while stimulating. As shown in Fig. 1, bidirectional micro-implants consist of stimulation and independently recording IC interacting with the external device.

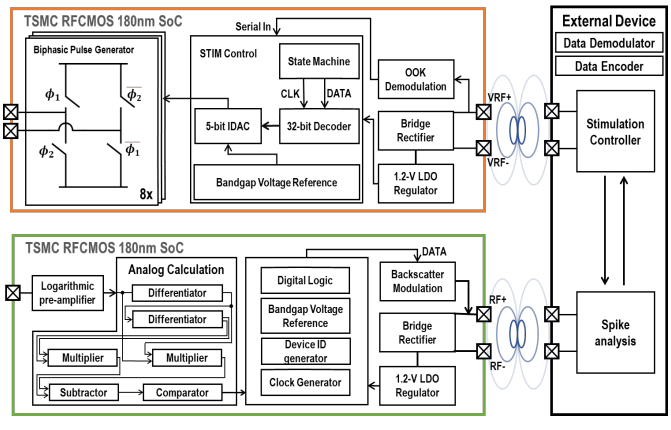

Fig. 1. Block diagram of the bidirectional micro-implant.

The paper is structured as follows: Section II briefly reviews the proposed BMI system's overall architecture and circuit diagram, Section III covers the experimental results of the recording and stimulation circuits with a wireless transceiver, and Section IV concludes the paper.

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Manuscript Received Sep. 27, 2023, Revised Dec. 16, 2023, Accepted Dec. 17, 2023

II. SYSTEM ARCHITECTURE AND ASIC DESIGN OVERVIEW

A. Spike Detection

The neural recording microsystem consists of a bio amplifier, a nonlinear operator-based detector, and a comparator. The system amplifies the neural signal, detects the spike signal included in the amplified signal, and wirelessly transmits the detected result as a digital signal to an external communication module.

The amplifier included in the IC is designed in fully differential mode. Two cascading stages using a feedback capacitor and subthreshold MOS resistor are used to amplify and filter the signal. Each transistor operates in weak, moderate, and strong inversion regions. A complementary input was used to reduce the amplifier noise, and a telescopic arrangement was made to obtain a higher gain. This topology is suitable for inducing capacitive loads and can minimize noise. The common-mode feedback (CMFB) circuit stabilizes the output voltage by controlling the common-mode output current. The cascade structure of the amplifier further stabilizes the output voltage. The MOS pseudo resistor feedback of the amplifier is based on the symmetrical biasing of the body and gate of two NMOS transistors under the subthreshold operating region. The circuit can utilize a very high resistance of tens of tera-ohms by using the simple MOS transistor architecture. The pseudo-resistor MOS transistors also have a diode property; the logarithm amplifier can be achieved by carefully adjusting the parameter and structure of the feedback pseudo-resistor. The feedback increases exponentially to the amplifying stage's output as the output is adjusted to follow the logarithmic output function. The relatively small neural spikes are normalized to a recognizable amplitude, and a significant noise or artifact has a small amplification ratio so the system can resist saturation. The specifications of the designed amplifier are listed in Table I.

TABLE I. Amplifier Specification

Parameter	Value
Supply voltage	1.2 V
Power Consumption	7.32 μW
Total Gain	35 dB
Bandwidth	0.2 Hz ~ 7 kHz
CMRR	70 dB
PSRR	80 dB
Input referred noise	5.4 μVrms

A distinguishing signal operation is required to utilize the spike signals at a noise level because the system has a logarithmic transfer function with a higher amplification ratio for noise-level signals. The spike is detected by the operator and planned to be utilized in the spike frequency-based BMI system rather than the system based on the signal waveforms. A robust analog spike detecting operator in low signal-to-noise, a Nonlinear energy operator (NEO), has already been used to compute signals' instantaneous frequency and amplitude [10]–[15]. The circuit is relatively simple and can be implemented on a large-scale implantable chip.

The frequency component of the signal is extracted from the derivative, the low-frequency components are attenuated, and the high-frequency components are emphasized. The operator shows the robust property against low-frequency noise. The calculation of the NEO in the input signal is performed by the analog calculation circuit consisting of an analog differentiator, multiplier, and subtractor.

B. Constant Current Stimulator

Constant current stimulation (CCS) is used mainly because of its advantages in better control of the amount of charge transferred during stimulation, high calibration accuracy, and better stimulation efficiency. It is also believed that the CCS provides a constant charge regardless of the impedance change at the electrode-tissue interface. For a current source, a 5-bit binary-weighted current steering Digital to Analog Converter (DAC) delivers up to 100μA of stable current to each output stage. Bandgap voltage reference circuit provides stable bias voltage to DAC delivering 2.2 μA. The summed current of the 5-stage DAC is transmitted to the biphasic pulse generator through the current mirror.

Generally, the current source-sink structure may be vulnerable to changes in output load due to the reduced voltage swing in half. In this system, the output voltage swing was maximized by switching the bias of the reference electrode in the bipolar-type stimulus structure. Also, the output stage of the current source-sink design increases the output impedance by adding feedback to the regulated cascoded current mirror.

TABLE II. Stimulator Specification

Parameter	Value
Supply voltage	1.2 V
Mode	Biphasic current stim.
Channel	8
Current	120 μA
Pulse width	50 μs – 1 ms
Frequency	5 – 1 kHz
Power consumption	9.7 μW / 2.1 mW

Pads of the 8-channel active electrode are arranged in a regular hexagonal structure with the reference pad placed in the center. The electrode arrangement in the regular hexagonal shape can precisely designate the location of the stimulus according to the channel selection, and it is possible to predict the amount of charge reaching the target with high precision by calculating the amount of reduction in current diffusion in the electrolyte. Detailed specification of stimulator unit is listed in Table II.

C. On-chip Coil Antenna

The structure of the antenna coil was designed and simulated using ANSYS HFSS. Additional antenna efficiency, resonant frequency matching, and matching circuits were verified by Cadence Design Simulator using

simulation data extracted from HFSS. In Fig. 2, the simulation model is a silicon-based chip of 1 mm × 1 mm, designed to implement the dielectric property of substrate silicon, an oxide layer, a polysilicon layer, and metal layers. The in-vivo dielectric condition of multi-layer tissue was constructed of 1 mm skin, 0.14 mm fat, 7 mm skull, 0.5 mm dura, 0.2 mm cerebrospinal fluid (CSF), and 81 mm Greymatter assuming the relay coil is inserted in CSF. The size of the on-chip coil is chosen to maximize coil efficiency and utilization of the area within the 1 mm × 1 mm boundary. 2-turn coil structure was selected to secure the inside of the CMOS fabrication area. The width and spacing of the metal were swept to maximize coil efficiency under 915 MHz transmission frequency. The 915 MHz frequency of transmission RF signal was selected to limit tissue absorption while providing enough powering mm size coils. The on-chip coil was fabricated with Metal 6 in TSMC 180 nm RFCMOS process.

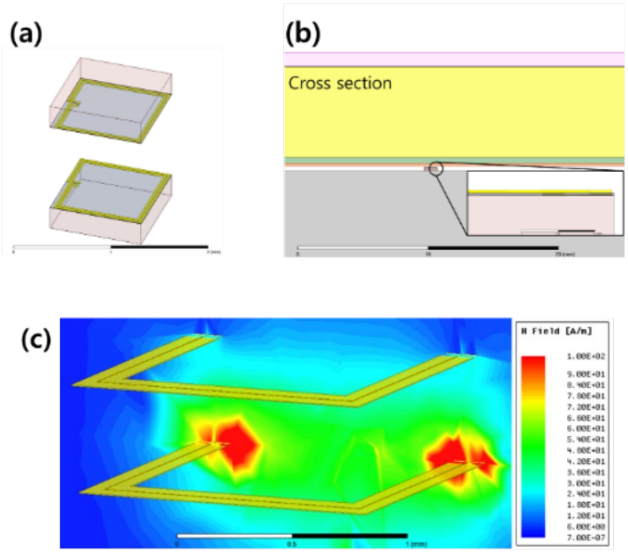

Fig. 2. Coil design of (a) 1 mm × 1 mm on-chip coil facing toward each other, (b) cross-section of chip mounted on head layers, (c) magnetic field simulation result.

D. Power IC

A 2-stage bridge rectifier with 5 pF charging capacitors and a capless LDO regulator [16] modulates the power management circuit's 900-915 MHz carrier frequency. With a 3 dBm input power, the rectifier generates 1.17V dc voltage. The capless regulator is turned on when the designed rectifier receives sufficient power. The regulator supplies a stable supply voltage to the stimulation and spike recording IC. The regulator consists of a conventional PASS transistor, an error amplifier, a start-up circuit, and a reference voltage generator. The target gain is over 80dB, and the phase margin is 60°.

E. Uplink–Downlink Transceiver

As the proposed neural implants independently communicate with the external device, each IC needs an up/down transceiver. Backscatter communication is now widely used for biomedical implants. We utilized backscattering modulation for uplink communication of recording IC. NMOS transistor is placed at the rectifier's input port to modulate the antenna's matching impedance. The transistor size is calculated based on the parasitic capacitance and resistance. The modulation frequency is calculated according to the spike rate. The narrow backscattering turn-on period prevents the failure of losing stable VDD, but still quite a considerable variation for a detectable signal.

An envelope detection circuit with additional passive LPF is implemented for the downlink communication in stimulation IC. The on-off shift keying (OOK) demodulation circuit with a 915 MHz carrier frequency sends the demodulated signal to a comparator. Also, the internal ring oscillator provides the clock to the comparator and digital logic, lowering the bit error rate.

The demodulated binary signal works as the clock synchronization input to the digital logic circuit. There are several counters and registers in digital logic for generating a sequential switching signal that is passed to an analog switch that provides a programmable stimulation pulse. Also, it controls the current amplitude using an on-chip 4-bit DAC, generates timing signals for the pulse width and frequency, and sets the current direction using the switch at the biphasic pulse generator.

III. EXPERIMENTAL RESULTS

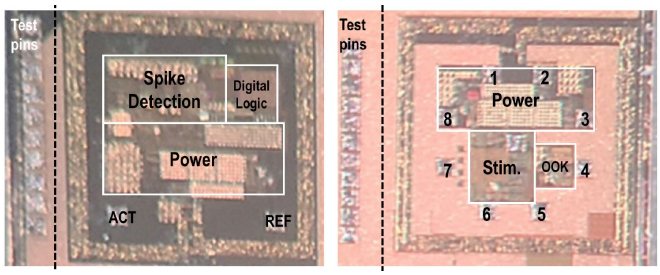

Fig. 3. Microphotograph of neural implant ASIC

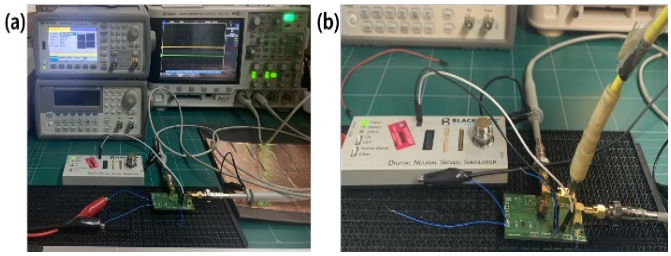

Fig. 4. Experimental setup of the system. (a) A signal measurement setup, and (b) wireless power and data transmission test setup.

The proposed system was fabricated in the TSMC 1P6M 180nm CMOS process. The microphotograph of the whole chip in Fig. 4 includes a 1-channel spike recorder and an 8-channel stimulator, which have their wireless transceiver to form an independent system. Test pins at the left of each IC help characterize the core circuits. Both IC is mounted on customized PCB with 50 Ω line matching. Fig. 3. Shows the microphotograph of neural implant ASIC, and Fig. 4. Shows

the experimental setup for the ASIC test.

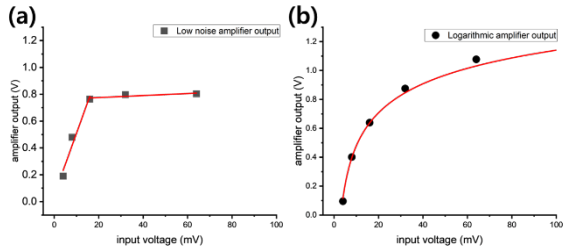

Fig. 5. Transfer function comparison of (a) typical linear amplifier and (b) designed logarithmic amplifier.

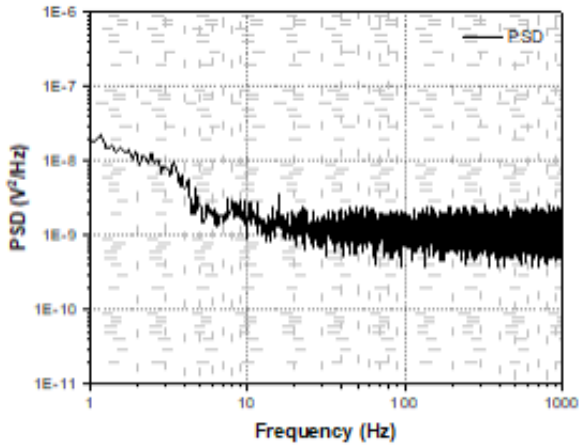

Fig. 6. Noise performance test result of the designed amplifier.

The analog front-end amplifier was verified via measuring noise and transfer function. The input signal greater than the input range of the typical amplifier is logarithmically adjusted as shown in Fig. 5., and Fig. 6 shows the noise performance of the amplifier.

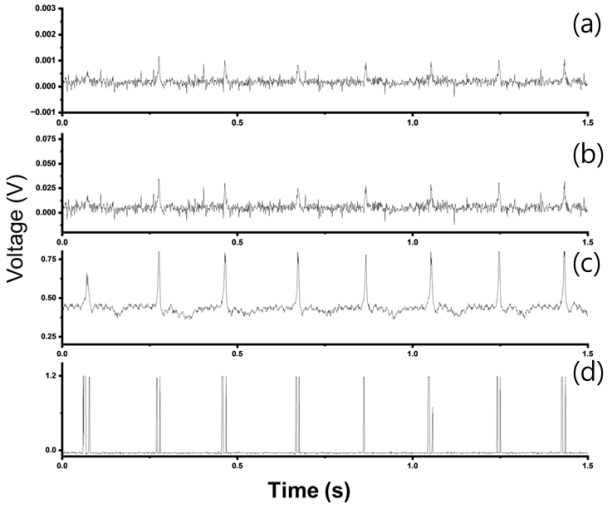

Fig. 7. (a) The output of the spike signal generator (b) The attenuated signal (c) The amplifier output of the system (d) The spike detection result of the system

The system output was measured using a spike shape signal generator. The spike generator generated spike-shaped (instantaneous frequency, high amplitude) signals. The 49 dB attenuation was performed to adjust the input range to a level similar to the actual neural spikes. An oscilloscope recorded the measurement of the amplifier and spike detection module. In Fig. 7, the oscilloscope recorded the raw signal (a), (b), amplifier output (c), and spike detection result (d) at the same time.

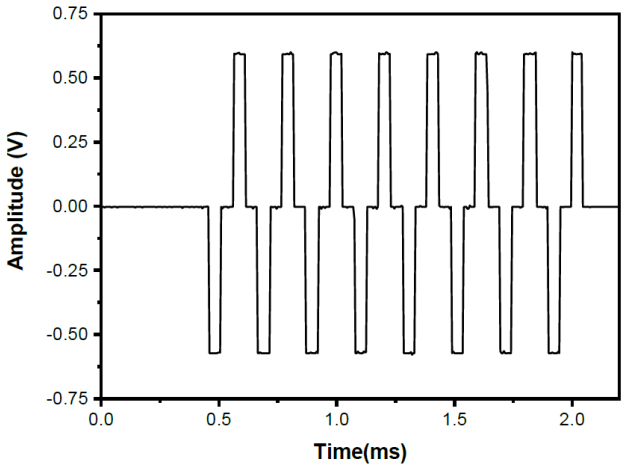

Fig. 8. Measured stimulation pulse in PBS solution.

Fig. 8 shows the voltage measurement with Pt/Ir conical electrode. The resistance of the electrode was 8-11 kΩ. Stimulation voltage is measured between the active and reference electrodes placed in the PBS 1x solution. The interphase delay between the cathodic and anodic phases is optional.

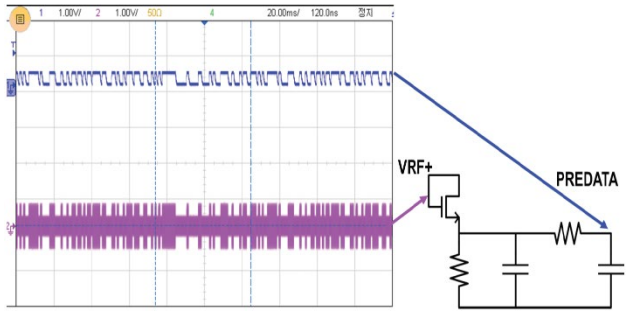

Fig. 9. Measurement of RF demodulation circuit with RF signal generator.

Fig. 9 shows the RF signal demodulation with the OOK demodulator. The result indicates that a low pass filter reduces the amplitude of PREDATA. However, it is sufficient for demodulation because the comparator got 320 mV as reference voltage below the PREDATA. The minimum amplitude detected for demodulation was 350 mV, regenerating 1 MHz clock. The system clock of 1.07 MHz was divided from a 12 MHz ring oscillator, and an additional D-Flip-flop synchronized the DATA and CLK.

IV. CONCLUSION AND FUTURE WORK

In this study, we've developed a refined, distributed multichannel architecture for sub-mm size wireless neural stimulation and recording devices. This innovative method facilitates simultaneous access to multiple critical sites of interest, allowing ongoing, precise recording and stimulation activities. Our demonstrations have successfully illustrated the capability of distinct neural interface techniques, utilizing an energy-operator-based spike detection and a versatile multichannel biphasic stimulation.

This study not only emphasizes the advanced design and functionality of our system but also foregrounds its adaptability and flexibility in recording methodologies. The focus of our future work will pivot towards the development of an integrated system on chip (SoC), consolidating the functionalities of recording and stimulation ASIC. This will be instrumental in forging a robust network of distributed systems, essential for the realization of an optimized, fully functional Brain-Machine Interface (BMI), contributing significantly to the forward momentum in neuroscientific exploration and application.

ACKNOWLEDGMENT

This research was supported by the Bio & Medical Technology Development Program of the National Research Foundation (NRF)& funded by the Korean government (MSIT) (2022M3E5E9016884). Also, the chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

REFERENCES

[1] C. Ethier, E. R. Oby, M. J. Bauman, and L. E. Miller, "Restoration of grasp following paralysis through brain-controlled stimulation of muscles," *Nature*, vol. 485, no. 7398, pp. 368–371, 2012, doi: 10.1038/nature10987.

[2] L. R. Hochberg *et al.*, "Neuronal ensemble control of prosthetic devices by a human with tetraplegia," *Nature*, vol. 442, no. 7099, pp. 164–171, 2006, doi: 10.1038/nature04970.

[3] V. W. Leung *et al.*, "Distributed Microscale Brain Implants with Wireless Power Transfer and Mbps Bi-directional Networked Communications," *Proc. Cust. Integr. Circuits Conf.*, vol. 2019-April, pp. 7–10, 2019, doi: 10.1109/CICC.2019.8780289.

[4] D. Ahn and M. Ghovanloo, "Optimal Design of Wireless Power Transmission Links for Millimeter-Sized Biomedical Implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 1, pp. 125–137, 2016, doi: 10.1109/TBCAS.2014.2370794.

[5] N. Ahmadi *et al.*, "Towards a Distributed, Chronically-Implantable Neural Interface," *Int. IEEE/EMBS Conf. Neural Eng. NER*, vol. 2019-March, pp. 719–724, 2019, doi: 10.1109/NER.2019.8716998.

[6] D. Seo, J. M. Carmena, J. M. Rabaey, E. Alon, and M. M. Maharbiz, "Neural Dust: An Ultrasonic, Low Power Solution for Chronic Brain-Machine Interfaces," no. April, 2013, [Online]. Available: http://arxiv.org/abs/1307.2196.

[7] J. Lee *et al.*, "Neural recording and stimulation using wireless networks of microimplants," *Nat. Electron.*, vol. 4, no. 8, pp. 604–614, 2021, doi: 10.1038/s41928-021-00631-8.

[8] P. Yeon, M. S. Bakir, and M. Ghovanloo, "Towards a 1.1 mm2 free-floating wireless implantable neural recording SoC," *2018 IEEE Cust. Integr. Circuits Conf. CICC 2018*, pp. 1–4, 2018, doi: 10.1109/CICC.2018.8357048.

[9] S. Ha *et al.*, "Silicon-Integrated High-Density Electrocortical Interfaces," *Proc. IEEE*, vol. 105, no. 1, pp. 11–33, 2017, doi: 10.1109/JPROC.2016.2587690.

[10] J. F. Kaiser, "On a simple algorithm to calculate the 'energy' of a signal," *ICASSP, IEEE Int. Conf. Acoust. Speech Signal Process. - Proc.*, vol. 1, no. 10, pp. 381–384, 1990, doi: 10.1109/icassp.1990.115702.

[11] B. Gosselin and M. Sawan, "An ultra low-power CMOS automatic action potential detector," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 17, no. 4, pp. 346–353, 2009, doi: 10.1109/TNSRE.2009.2018103.

[12] Y. G. Li, Q. Ma, M. R. Haider, and Y. Massoud, "Ultra-low-power high sensitivity spike detectors based on modified nonlinear energy operator," *Proc. - IEEE Int. Symp. Circuits Syst.*, pp. 137–140, 2013, doi: 10.1109/ISCAS.2013.6571801.

[13] E. Koutsos, S. E. Paraskevopoulou, and T. G. Constandinou, "A 1.5 μw NEO-based spike detector with adaptive-threshold for calibration-free multichannel neural interfaces," *Proc. - IEEE Int. Symp. Circuits Syst.*, pp. 1922–1925, 2013, doi: 10.1109/ISCAS.2013.6572243.

[14] W. Cao and H. Li, "Ultra-low-power neural recording microsystem for implantable brain machine interface," *Proc. - 2013 IEEE Int. Conf. Green Comput. Commun. IEEE Internet Things IEEE Cyber, Phys. Soc. Comput. GreenCom-iThings-CPSCom 2013*, pp. 1050–1053, 2013, doi: 10.1109/GreenCom-iThings-CPSCom.2013.178.

[15] J. P. Kim, H. Lee, and H. Ko, "0.6 V, 116 nW neural spike acquisition IC with self-biased instrumentation amplifier and analog spike extraction," *Sensors (Switzerland)*, vol. 18, no. 8, pp. 1–13, 2018, doi: 10.3390/s18082460.

[16] Y. Jia, Y. Gong, A. Weber, W. Li, and M. Ghovanloo, "A mm-sized free-floating wireless implantable opto-electro stimulation device," *Micromachines*, vol. 11, no. 6, pp. 1–17, 2020, doi: 10.3390/mi11060621.

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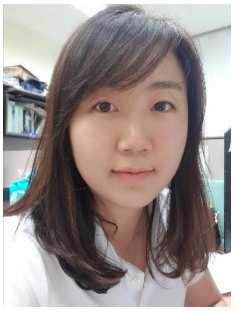

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