Design of K-Band CMOS Variable Gain Amplifier Using Amplification Stage and Variable Attenuation Stage

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Abstract - **In this study, we design a K-band CMOS variable gain amplifier (VGA) for beamforming system applications. The designed VGA consists of amplification and attenuation stages. The amplification stage consists of two common-source gain stages and has a power gain of approximately 18 dB in the simulation. In the case of the attenuation stage, it has a total of 5-bit attenuation steps, and the attenuation range in the simulation is 31 dB. To suppress insertion loss, attenuation bits for low attenuation levels were designed in a distributed structure. On the other hand, attenuation bits for high attenuation levels are designed in a π-structure to secure high attenuation levels. In addition, to suppress the phase error, tail capacitors are added to transistors used in the attenuation stage. The designed K-band VGA was manufactured using a 65-nm RFCMOS process. The chip size of the designed VGA was 0.65 × 0.50 mm^2. At operating frequencies 22.0 GHz to 23.6 GHz, the measured variable gain range was between 26.5 dB and 28.2 dB. In this case, the measured RFM phase and attenuation errors were less than 6.40° and 1.24 dB, respectively.**

Keywords—**Attenuator, beamforming, CMOS, variable gain amplifier**

I. INTRODUCTION

With the development of 5G mobile communication technology, beamforming systems are in the spotlight as one of the main transceiver structures of wireless communication systems [1–4]. Such a beamforming system is expected to be adopted not only in 5G but also in 6G mobile communication, and attempts are being made to apply it to various applications [5–7].

With the introduction of beamforming systems, interest in functional circuits that can adjust the beam patterns of antennas, such as phase shifters, variable gain amplifiers (VGAs), and attenuators, is also increasing. In particular, VGAs and attenuators played a major role in typical transceiver systems for mobile communication, and their importance has increased further in beamforming systems [8–11]. For such VGAs, the variable gain range and RMS phase and gain errors are the main performance indicators. Similarly, for attenuators, variable attenuation ranges and RMS phase and attenuation errors are the main performance indicators.

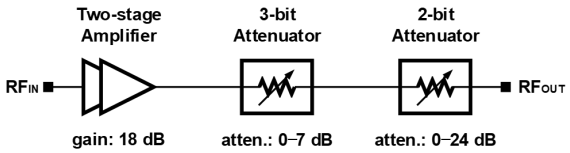

Fig. 1. Block-diagram of the designed VGS.

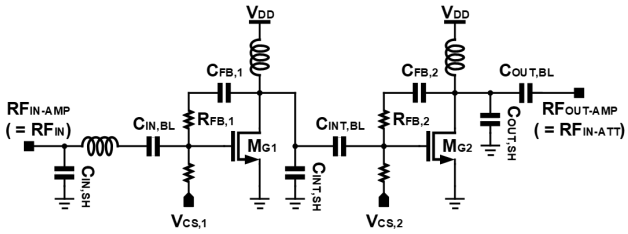

Fig. 2. Schematic of the amplification stage.

In this study, for the beamforming system in the flexible access common spectrum (FACS) applications [5–7], we designed a K-band CMOS VGA. In particular, we combined a gain amplifier and a digital step attenuator to simultaneously secure variable gain and variable attenuation function with a single integrated circuit (IC). In order to secure a sufficient gain, the gain amplifier was composed of two-stages. Here, in order to suppress the phase error due to the variation of the gain, a variable function was implemented only at the attenuation stage of the designed VGA. In addition, a digitally controllable attenuator was combined with a total of 5-bits to secure a sufficient variable gain range. To further suppress the phase error, tail capacitors were added to transistors used in the attenuation stage.

II. DESIGN OF THE K-BAND CMOS VGA

In this study, in order to secure both variable attenuation and gain functions at the same time, the VAG consisted of two stages and a 5-bit attenuator, as shown in Fig. 1. Here, the operating frequency was set from 22.0 GHz to 23.6 GHz. As follows, the gain amplification stages were first

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TABLE I. Specific values of the devices used in the amplification stage.

Device	Value	Device	Value
M_{G1}, M_{G2} (μm)	40[1)]	$C_{INT,BL}$ (fF)	420
$C_{IN,SH}$ (fF)	80	$C_{OUT,SH}$ (fF)	23
$C_{IN,BL}$ (fF)	420	$C_{OUT,BL}$ (fF)	420
$C_{FB,1}$, $C_{FB,2}$ (fF)	107	$R_{FB,1}$ (Ω)	1,028
$C_{INT,SH}$ (fF)	17	$R_{FB,2}$ (Ω)	771

[1)] total gate width

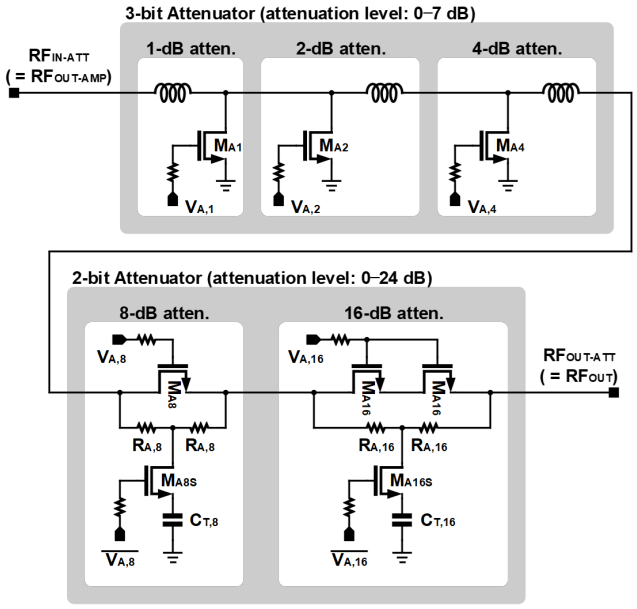

Fig. 3. Schematic of the attenuation stage.

described, and then the attenuator was described.

A. Two stage gain amplifier

As shown in Fig. 1, the proposed CMOS VGA consists of amplifiers and attenuators. Fig. 2 shows the schematic of the amplification stage constituting the designed VGA. The amplification stage is formed by connecting two common-source (CS) structures.

The gate bias voltages were applied through resistors, and the supply voltage, V_{DD} was 1.0 V. The stability of the entire amplification stage was secured through RC feedback technique. A capacitor was added between the drain and source of the transistor to reduce the size of the load inductor, thereby suppressing power loss caused by the inductor and reducing the overall chip size. Other capacitors were used as the role of the dc blocking and for matching. Additionally, an additional series inductor was also used for input matching. $RF_{OUT-AMP}$, which is an output signal of the amplification stage, becomes RF_{IN-ATT}, which is an input signal of the attenuator. Specific values of the devices used in the amplification stage are shown in Table I.

B. 5-bit Attenuator

The schematic of the 5-bit attenuator is shown in Fig. 3. In order to minimize insertion loss, the lower three bits were designed with a distributed structure. Thanks to the repeated structure of series inductance and shunt capacitance of the distributed structure, bandwidth degradation caused by the lower three bits was minimized [12–16]. In addition, compared to M_{A4} in Fig. 3 for 4 dB attenuation, M_{A1} for 1 dB attenuation and M_{A2} for 2 dB attenuation are designed to have relatively small gate width. This means that the parasitic capacitances of M_{A1} and M_{A2} are smaller than that of M_{A4}. Therefore, in order to reduce the chip area, the parasitic capacitances of M_{A1} and M_{A2} were regarded as an integrated capacitance from the perspective of the composition of the distributed structure. Through this, the inductor between M_{A1} and M_{A2} was removed for the configuration of the distributed structure.

On the other hand, attenuators for attenuation of 8 dB and 16 dB are designed in a π-structure to secure high attenuation levels [17–19]. In general, the size of the shunt transistor in the π-structure to secure a high attenuation level is designed relatively larger than that of the transistor in the distributed structure. Therefore, in the π-structure, a phase variation occurs according to the attenuation level by a relatively large parasitic capacitance of the shunt transistor. In this study, to mitigate this, tail capacitors $C_{T,8}$ and $C_{T,16}$ were added as shown in Fig. 3.

RF_{IN-ATT}, which is an input signal of the amplification stage, is the same as $RF_{OUT-AMP}$, which is an output signal of the amplifier. Specific values of the devices used in the attenuation stage are shown in Table II.

TABLE II. Specific values of the devices used in the attenuation stage.

Device	Value	Device	Value
M_{A1} (μm)	1.7[1)]	M_{A8S} (μm)	7.2[1)]
M_{A2} (μm)	6.1[1)]	M_{A16S} (μm)	28.0[1)]
M_{A4} (μm)	9.0[1)]	$C_{T,8}$ (fF)	400
M_{A8} (μm)	40[1)]	$C_{T,16}$ (fF)	800
M_{A16} (μm)	40[1)]	-	-

[1)] total gate width

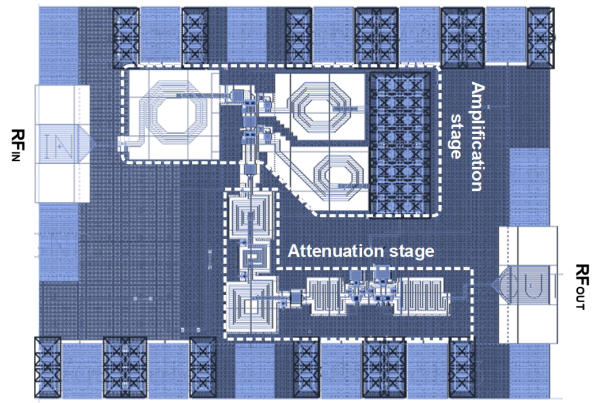

Fig. 4. Layout of the designed K-band CMOS VGA.

III. SIMULATION RESULTS OF THE K-BAND CMOS VGA

Fig. 4 shows the layout of the designed K-band CMOS VGA. The 65-nm RFCMOS process, which provides nine metal layers, was used. The areas of each of the amplification and attenuation stages are shown in Fig. 4. As shown in Fig. 4, in consideration of the connection with other circuits constituting each transceiver channel of the beamforming system, the attenuation stage was arranged in a bent form. Therefore, in the case of the test chip shown in Fig. 4, the

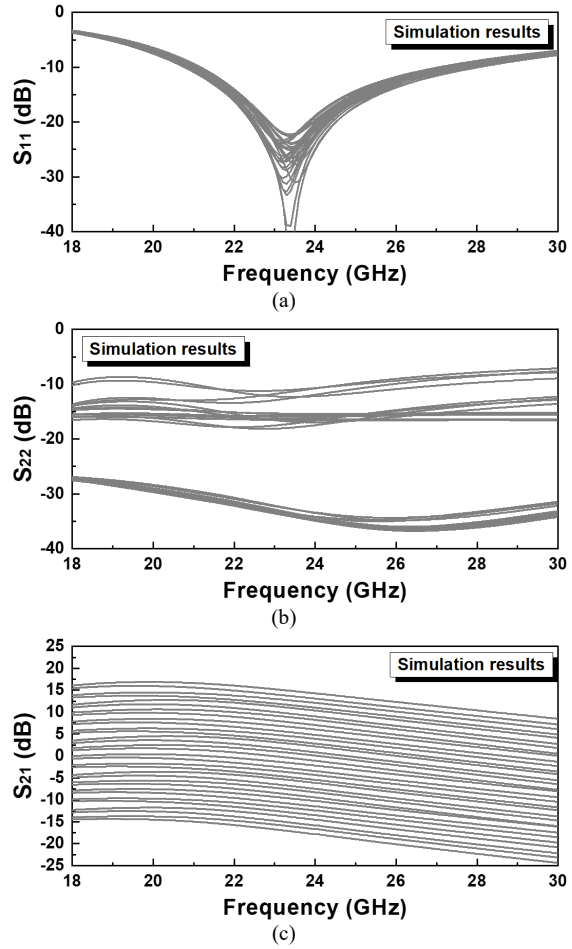

Fig. 5. Simulation results of S-parameters: (a) S_{11}, (b) S_{22}, and (c) S_{21}.

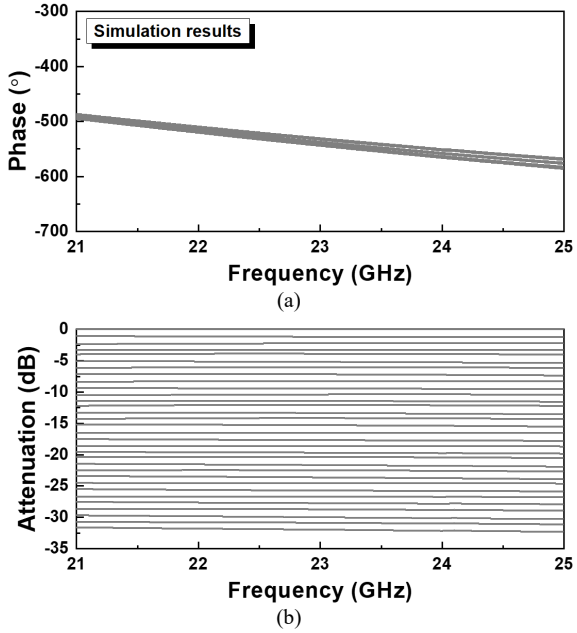

Fig. 6. Simulation results of phase and attenuation: (a) phase and (b) attenuation.

chip size increased due to the empty space where no devices and signal lines were placed. However, in the actual transceiver channel for beamforming system, other circuits were placed in the empty space of the designed test chip

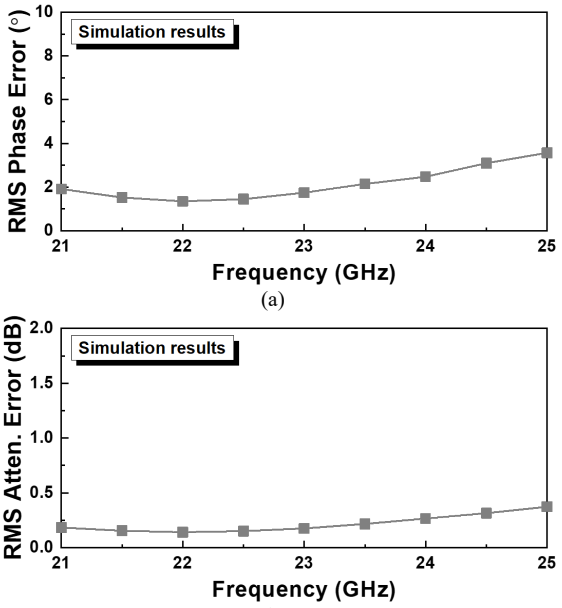

Fig. 7. Simulation results of RMS errors: (a) RMS phase and (b) RMS attenuation errors.

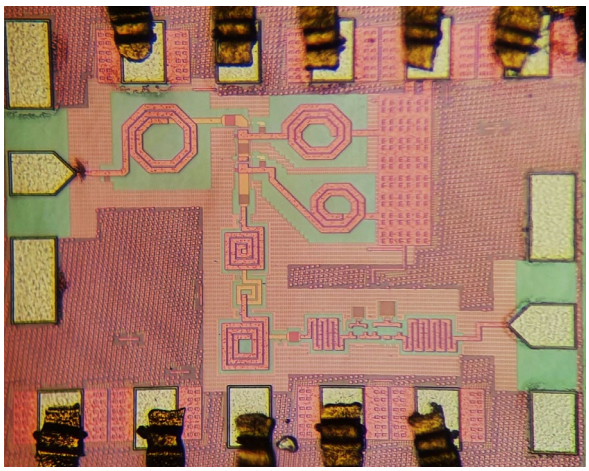

Fig. 8. Chip photograph of the designed K-band CMOS VGA.

shown in Fig. 4.

A supply voltage V_{DD} for the amplification stage is 1.0 V. In addition, the gate biases of the amplification stage, $V_{CS,1}$ and $V_{CS,2}$, are 0.55 V and 0.60 V, respectively. Control voltages V_{A1}, V_{A2}, V_{A4}, V_{A8}, and V_{A16} for adjusting the attenuation level are 0 V and 1 V. These supply voltage, gate biases, and control voltages were used equally not only in simulation but also in measurement.

To ensure the accuracy of the simulation, the effects of metal lines, inductors, and pads in the entire layout were considered through electromagnetic (EM) simulation. The target operating frequency range was 22.0 GHz to 23.6 GHz.

Fig. 5 shows the simulation results of the S-parameters. The target values of S_{11} and S_{22} were less than −10 dB. In the 21.0 GHz to 24.5 GHz range, which includes the target operating frequency range, both S_{11} and S_{22} were designed to be less than −10 dB. The degree of attenuation for each attenuation bit was confirmed from S_{21} of Fig. 5. The gain ranges at operating frequencies 22.0 GHz and 23.6 GHz were from 16.1 dB to −15.7 dB and 14.7 dB and −17.4 dB,

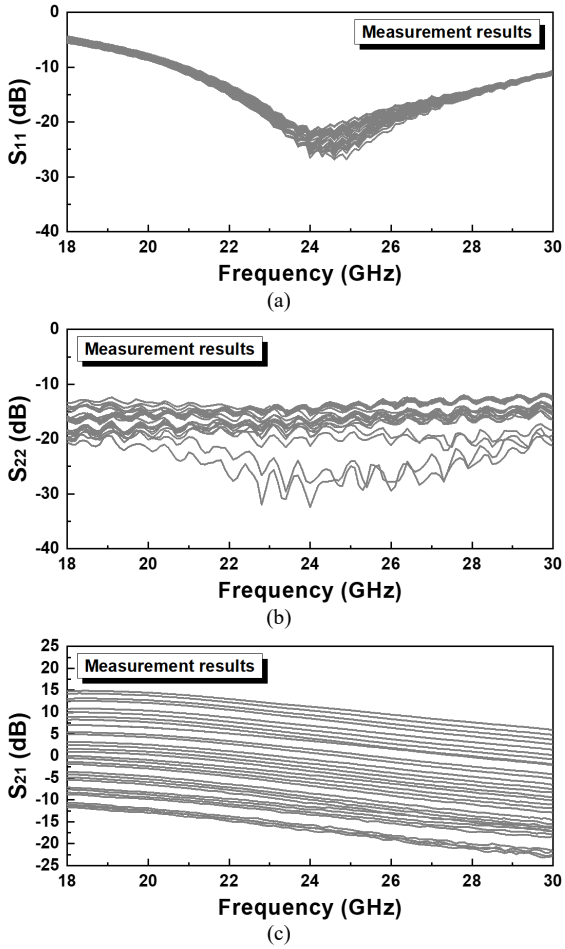

Fig. 9. Measurement results of S-parameters: (a) S_{11}, (b) S_{22}, and (c) S_{21}.

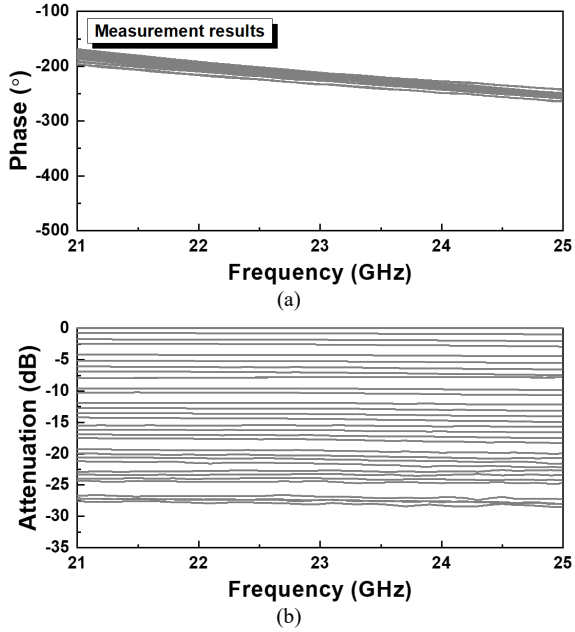

Fig. 10. Measurement results of phase and attenuation: (a) phase and (b) attenuation.

respectively. As a results, the variable gain ranges at operating frequencies 22.0 GHz and 23.6 GHz were 31.8 dB and 32.1 dB, respectively.

Fig. 6 shows the simulated phase and attenuation of each bit of the designed K-band CMOS VGA. At this time, Fig. 6(b) shows the simulated attenuation compared to the highest gain according to the frequency of the designed VGA. Fig. 7 shows the simulated RMS phase and attenuation errors derived based on the simulation results of the phase and attenuation shown in Fig. 6. From Fig. 7, in the operating frequency range of 22.0 GHz to 23.6 GHz, the RMS phase and attenuation errors were less than 2.25° and 0.22 dB, respectively.

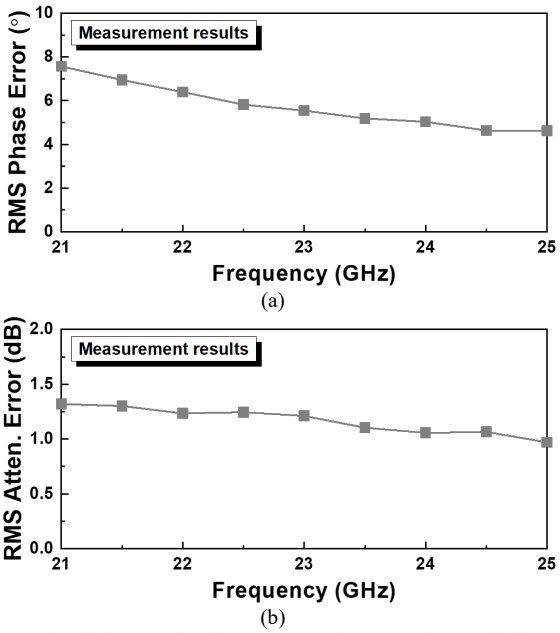

Fig. 11. Simulation results of RMS errors: (a) RMS phase and (b) RMS attenuation errors.

IV. MEASUREMENT RESULTS OF THE K-BAND CMOS VGA

Fig. 8 is a chip photograph of the designed K-band CMOS VGA. The total chip size, including the test pads, is 0.65 × 0.50 mm^2. RF input and output signals were measured using an RF probe on the wafer. Ground, supply voltage, gate biases, and control voltages were applied using bonding-wires.

Fig. 9 shows the measurement results of the S-parameters. The target values of S_{11} and S_{22} were less than −10 dB. In the 21.0 GHz to 30.0 GHz range, which includes the target operating frequency range, both S_{11} and S_{22} were designed to be less than −10 dB. The degree of attenuation for each attenuation bit was confirmed from S_{21} of Fig. 9. The gain ranges at operating frequencies 22.0 GHz and 23.6 GHz were from 13.0 dB to −14.9 dB and 11.6 dB and −16.6 dB, respectively. As a results, the variable gain ranges at operating frequencies 22.0 GHz and 23.6 GHz were 26.5 dB and 28.2 dB, respectively.

Fig. 10 shows the measured phase and attenuation of each bit of the designed K-band CMOS VGA. At this time, Fig. 10(b) shows the measured attenuation compared to the highest gain according to the frequency of the designed VGA. Fig. 11 shows the measured RMS phase and attenuation errors derived based on the measurement results of the phase and attenuation shown in Fig. 10. From Fig. 11, in the operating frequency range of 22.0 GHz to 23.6 GHz,

TABLE III. Performance comparison with various CMOS VGAs

Ref.	Tech. (nm)	Freq. (GHz)	Peak gain (dB)	Gain range (dB)	RMS phase error (°)
MWCL '19 [20]	65	30.0 – 34.5	20.8	10.6	< 3
MWCL '19 [21]	65	27.5	21.2	5	< 11 [1)]
MWCL '18 [22]	65	26 – 33	27.1	8.7	< 18 [1)]
APMC '20 [23]	65	24 – 28	29.4	6.2	< 3.3 [1)]
RFIC '18 [24]	65	27 – 42	9.6	7.8	< 3.5 [1)]
This work	65	22.0 – 23.6	13.0 – 11.6	26.5 – 28.2	< 6.40

[1)] maximum phase variation

the RMS phase and attenuation errors were less than 6.40° and 1.24 dB, respectively. The measured RMS errors were somewhat deteriorated compared to the simulation results. It is presumed that the main cause of deterioration is not only due to process variation, but also to the accuracy of electromagnetic simulation.

As shown in Table III, despite the wide range of gain variations, the measured RMS phase error characteristics are acceptable.

V. CONCLUSIONS

In this study, a K-band CMOS variable gain amplifier was designed. In order to secure power gain, two common-source gain stages were designed. In addition, in order to vary the gain, a variable attenuation stage that can be controlled with a total of 5-bits was designed. The distributed structure and π-structure were applied to the attenuation stage to suppress insertion loss and secure a wide variable attenuation range. The designed K-band VGA was fabricated using a 65-nm RFCMOS process. The chip size of the fabricated VGA was 0.65×0.50 mm^2. The variable gain range measured at operating frequencies 22.0 GHz to 23.6 GHz was from 26.5 dB to 28.2 dB. In the same frequency range, the measured RMS phase and attenuation errors were less than 6.40° and 1.24 dB, respectively.

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