Design of H-Band Oscillator IC in 250-nm InP HBT Process

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***Abstract* - In this paper, a voltage-controlled oscillator (VCO) operating at H-band (220-330 GHz) with 250-nm InP HBT technologies is presented. The VCO is designed with a Colpitts topology to oscillate at a fundamental frequency of 250 GHz. A common-base output buffer amplifier is implemented to isolate the oscillator core from the output load, thereby reducing the load-pulling effect. The VCO is designed by using Agilent Advanced Design System (ADS) tools. Small and large signal analysis were implemented by ADS. The measured frequency tuning range of the VCO is 12.6 GHz, spanning from 226.2-238.8 GHz. The maximum output power was measured at 230 GHz and recorded as 2.7 dBm. The dc power consumption is 32.2 mW, resulting in a dc-to-RF conversion efficiency of 5.2 %. The measured phase noise is -71.2 dBc/Hz at 10-MHz offset frequency.**

***Keywords*—Efficiency, tuning range, voltage-controlled oscillator (VCO)**

I. INTRODUCTION

The Terahertz (THz) band ranges from 0.1 to 10 THz. As THz signals are attenuated in the atmosphere resulting in shorter penetration distances than microwaves, they present challenges in applications. However, their broadband characteristics can significantly improve data rates, making THz a promising frequency band for high-speed communication (6G), high resolution radars and sensors [1]. A high power and high efficiency VCO, used as a signal source in the system, is an essential circuit block for implementing low-cost THz systems. Solid-state integrated circuits (ICs) are essential for small-sized, light weight, and low-cost THz systems [2]. However, there are several limitations to THz oscillator implemented as ICs. The CMOS technologies which have been utilized for implementing THz systems have advantages of high-integration and low-cost. However, CMOS technology has clear disadvantages such as low intrinsic power gain and power capability due to its low cut-off frequency(f_t) and maximum oscillation frequency (f_{max}) [3]. In [4], 300 GHz VCO was implemented in CMOS technology. The VCO has the advantage of a compact chip size, but it suffers from the low output power due to the low power characteristic of the CMOS technology. This necessitates an additional power amplifier (PA) in the transmitter of the system, which results in high power consumption and reduced efficiency of the system. In this work, an oscillator capable of operating as a standalone signal source at very high frequencies like H-band was designed using InP HBT technology, a type of compound semiconductor process known for its superior power characteristics. To lower the total cost of the systems where the oscillator will be applied, an oscillator was designed to minimize DC power dissipation for high dc-to-RF efficiency, and to produce relatively high output power, sufficient to operate the system without additional PA. The remainder of the paper is organized as follows; Section II explains the design procedure of the proposed oscillator, Section III represents the implementation of a VCO as well as measurement results, and Section IV concludes the paper.

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II. CIRCUIT DESIGN

A. Process utilized in the design

In this work, H-band VCO is designed using 250-nm InP HBTs by Teledyne Scientific, which provide high cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) around 350, and 650 GHz. Additionally, InP HBTs technology provides high 4.5 V breakdown voltage. Thus, this technology is suitable as an integrated part of a multifunctional chip and can be fully utilized for power amplifier, oscillator in transmitters and low noise amplifier in receivers, which are likely to be used as low-cost THz applications in the future [5]. Fig. 1 shows the back-end-of-line (BEOL) structure of the 250-nm InP HBT process. The BEOL structure includes four metal layers (M1-M4) for high-performance passive circuits. The thickness of the top metal layer, M4, is 3 μm, while the bottom metal layer M1 is 0.8 μm thick, and the intermediate layers, M2 and M3, are each 1 μm thick. Each metal layer is separated by a Benzocyclobutene (BCB) layer with a dielectric constant of 2.7. To minimize HBT's underlying resistance and collector-base capacitance, it is important to align the two contacts closely. Since the resistors, capacitors, and HBTs are connected to M1, the signal line utilizes M1, and ground uses M3 to reduce additional parasitic effects of interconnections. This arrangement results in a relatively short ground connection, thereby providing low inductance to ground for the active device. It can also help to design compact circuit size. M4 was used to supply voltage and current to transistors.

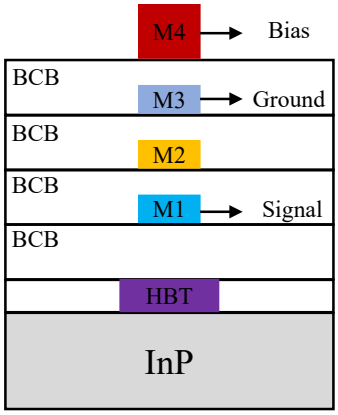

Fig. 1. The BEOL structure of 250-nm InP HBT technology.

B. Design of oscillator core

Fig. 2 shows the small-signal equivalent circuit of the Colpitts oscillator. In high-frequency applications, the Colpitts oscillator is widely utilized due to its low phase noise and wide tuning range [6]. Colpitts oscillator consists of an LC tank with two series-connected capacitors, C_{BE}, C_{var}, and a parallel-connected inductor, L_B. The LC tank of the oscillator resonates when the reactance of the series capacitors matches that of the parallel inductor, causing the oscillator to oscillate at the oscillation frequency f_{osc}. The resonance frequency f_{osc} is given as

$$f_{osc} = \frac{1}{2\pi\sqrt{L_B\frac{C_{BE}C_{var}}{C_{BE}+C_{var}}}}.$$

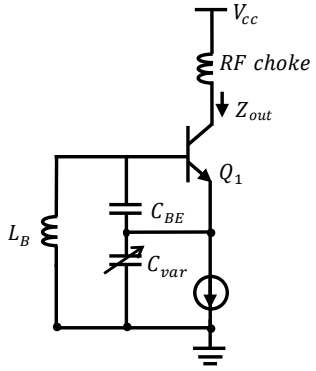

Fig. 2. The equivalent circuit of the Colpitts oscillator.

The varactor capacitance, C_{var}, is implemented as a variable capacitance using a base-emitter tied HBT and can be tuned with a control voltage, V_{CON}. When V_{CON} = 0 V, C_{var} is 7.6 fF. C_{BE} represents the base-emitter junction capacitance and has a fixed value. Based on the capacitance values of C_{var} at 7.6 fF and the fixed C_{BE} capacitance at 250 GHz, a small signal analysis was conducted by sweeping the base terminal's inductance, L_B. Fig. 3 illustrates the results of the small signal impedance analysis. It can be observed that negative resistance is generated when L_B is less than 40 pH. In this work, L_B = 30 pH was chosen to facilitate the startup of oscillation due to its high magnitude of negative resistance.

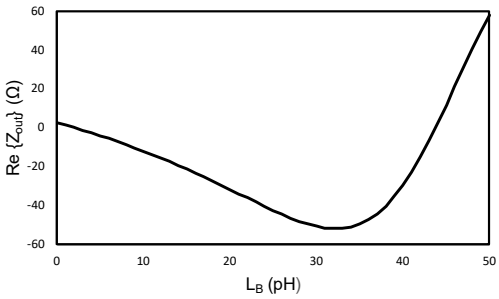

Fig. 3. Output resistance according to L_B.

Fig. 4 illustrates the structure of the VCO core. The current source is implemented as a transmission line with a length of λ/4 at 250 GHz, and the base inductance L_B is realized as a transmission line TL_B at the base terminal.

By configuring the feedback network as described above, Colpitts oscillator which generates high-power could be implemented.

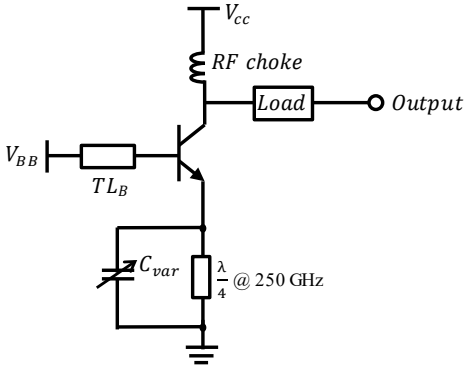

Fig. 4. The schematic of the VCO core.

C. Final design of VCO

To predict the output power of the oscillator and the oscillation frequency (f_{osc}) that varies with load impedance, both small signal analysis and large signal analysis were implemented by Agilent Advanced Design System (ADS). In this work, the load-pull simulation for large-signal analysis was used to find optimum load impedance $Z_{L,opt}$ which provides high power at desired f_{osc}. Fig. 5 shows the power contours obtained from load pull simulation. This figure demonstrates that the load impedance satisfying the oscillation frequency exists within a restricted region as shown in the Smith chart. This indicates that the load-pulling effect of the designed core of the VCO is significant.

To minimize the load-pulling effect and achieve stable oscillation, a buffer amplifier was added to isolate the core of the VCO from the output load. In this work, a common-base output buffer amplifier was implemented.

Fig. 6 shows the load-pull contours for output power of the oscillator with buffer amplifier. It shows that the dependency on the load impedance for output power has decreased. This is equivalent to a decrease in the load-pulling effect. Furthermore, the utilization of a buffer amplifier also shows an increase in the output power

compared to the case when a single core is employed. The maximum output power has increased by 2.9 dB, from the previous 4.3 dBm to 7.2 dBm.

In the load-pull contours for output power, as the impedance moves towards the upper region of the Smith chart, the output power increases, but f_{osc} decreases. Therefore, in this work, the optimum load impedance $Z_{L,opt}$ has been chosen to achieve a suitably high output power and high f_{osc} simultaneously.

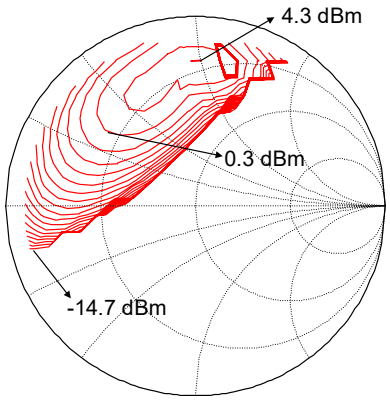

Fig. 5. Load-pull contours for output power of the oscillator core (solid lines in steps of 1 dB).

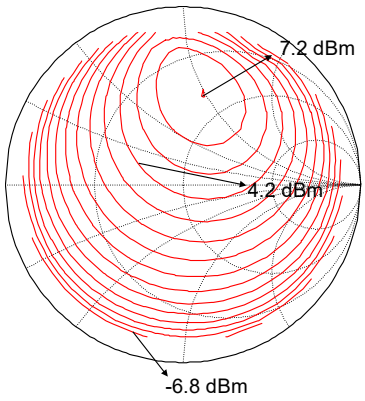

Fig. 6. Load-pull contours for output power of the oscillator with a buffer amplifier (solid lines in steps of 1 dB).

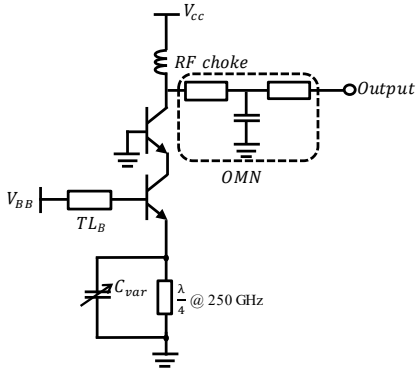

Fig. 7. The schematic of the VCO with the buffer amplifier.

The schematic of the VCO with the buffer amplifier is depicted in Fig. 7. The output matching network, consisting of series transmission lines and shunt capacitor, was implemented to achieve $Z_{L,opt}$. The transmission lines of the VCO are implemented using the inverted microstrip structure, where the lowest metal layer M1 is used as a signal path and M3 layer is used as a ground plane. This structure could minimize the parasitic effects of the interconnection lines due to its short interconnection to the transistors.

The HBT utilized in the buffer amplifier is biased to the collector current of 9 mA and the voltage of 3.6 V. Electromagnetic (EM) simulations were performed to check the operation of the designed oscillator. In Fig. 8, the simulated oscillation frequency (f_{osc}), and output power obtained from EM simulations are plotted. It is observed that the frequency tuning range is 40.2 GHz (236.6 GHz to 276.8 GHz), the maximum output power is about 4.5 dBm, and the maximum dc-to-RF efficiency calculated from the output power is 8.8 %.

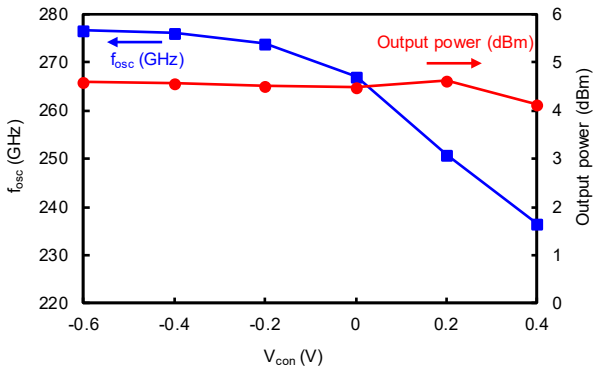

Fig. 8 Simulated f_{osc}, and the output power of the VCO as a function of the varactor voltage (V_{CON}).

III. MEASUREMENT

Fig. 9 shows the photograph of the fabricated VCO IC. The chip size is 590 μm × 420 μm. On-wafer measurement setup for output power, f_{osc} and phase noise is depicted in Fig. 10. Output power was measured by a PM5 power meter with a WR-3.4 probe. To detect the oscillation frequency, *H*-band oscillation signal is down-converted to IF signal using a sub-harmonic mixer. The resultant IF signal is measured by using a spectrum analyzer. Attenuator is used to limit the input power level into the sub-harmonic mixer to prevent damage due to the limited damage level of the sub-harmonic mixer. Frequency extender module (frequency multiplier-by-6) is used to generate LO signal and drive the sub-harmonic mixer. Fig. 11 represents the measurement results obtained using the mentioned setup. Measurement results indicate the frequency tuning range of 12.6 GHz (226.2 GHz to 238.8 GHz), the maximum output power of 2.7 dBm, and the peak dc-to-RF efficiency of 5.2 %. From the measured results, it is observed that the output power is about 2 dB lower than the simulation results. Also, the frequency tuning range decreased significantly to one-third, from 40.2 GHz to 12.6 GHz. The decrease in output power and frequency tuning range is attributed to the interconnection between

TABLE I. Performance Comparison With H-band VCOs

Ref.	Tech.	Pout (dBm)	f_{osc} (GHz)	Tuning range (GHz)	Phase noise (dBc/Hz) @ 10 MHz	PDC (mW)	Efficiency (%)	Size (mm^2)
[4]	32 nm CMOS	-7	234 – 247.5	13.5	-	7	0.09	0.06
[7]	250 nm InP HBT	1.5	272.4 – 310.8	38.4	-96.4	148	0.95	0.2
[8]	250 nm InP HBT	4.7	294.9 – 304.8	9.9	-86.6-	75.6	3.90	0.22
[9]	250 nm InP HBT	-5	310 - 320	10.0	-	46.2	0.68	-
[10]	250 nm InP HBT	4.8	298.1 – 316.1	18.0	-	88.1	3.43	0.22
This work	250 nm InP HBT	2.7	226.2 – 238.8	12.6	-71.4	32.2	5.2	0.25

transistors and signal lines, as well as additional parasitic components not included in the transistor model provided by the foundry. Since parasitic effects alter the LC resonance frequency, they lead to changes in both the oscillation frequency and the output power. It also seems that oscillation frequency and output power drop rapidly due to the low Q -factor of the varactor as V_{CON} exceeds 0.2 V. Fig. 12 shows the spectrum at V_{CON} = 0 V. At this condition, the phase noise is the lowest, with the output signal frequency at 232.06 GHz. This output signal, mixed with a $2f_{LO}$ = 220 GHz signal in a subharmonic mixer, results in a 12.06 GHz IF signal displayed on the spectrum analyzer, exhibiting a phase noise of -71.2 dBc/Hz at 10 MHz offset frequency. In the phase noise spectrum, a discontinuity is observed near the 1 MHz offset frequency. This issue occurs due to the challenges in calibrating the influence of an external subharmonic mixer on the phase noise. As in [11], at low offset frequencies, it is extremely challenging to ensure resolution bandwidth that prevents accidental measurement of carrier power due to fluctuation of oscillation frequency.

Table 1 summarizes the performance of the proposed VCO and compares it with other VCOs operating at H-band. Unlike other works that employ a differential structure with superior noise characteristics, the proposed VCO uses a single-ended structure, leading to a slight degradation in phase noise performance. However, this approach significantly reduces DC power consumption by more than half, resulting in a markedly higher dc-to-RF efficiency, which is a dominant factor in reducing system cost.

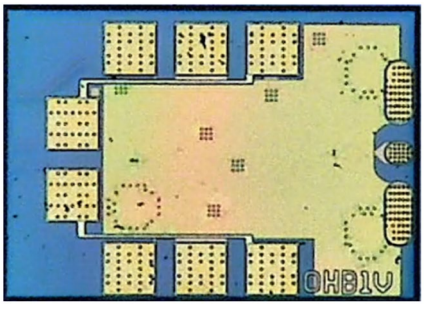

Fig. 9. Photograph of fabricated VCO.

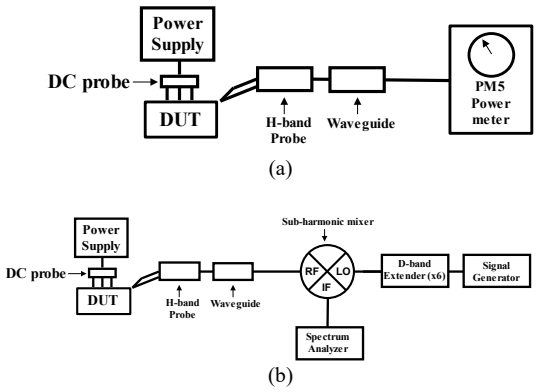

Fig. 10. Measurement setup (a) Power measurement (b) Spectrum and phase noise measurement.

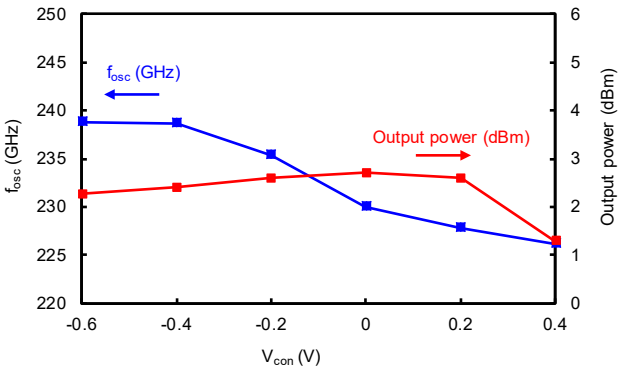

Fig. 11. Measured f_{osc}, and the output power of the VCO as a function of the varactor voltage (V_{CON}).

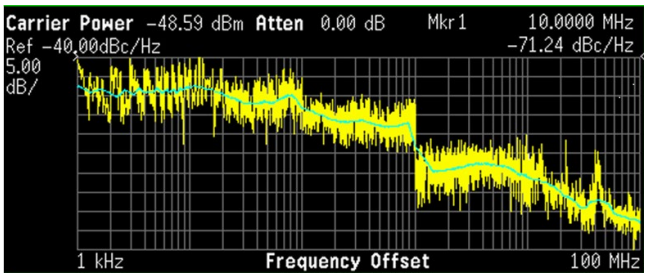

Fig. 12. Measured phase noise of the VCO.

IV. CONCLUSION

In this paper, H-band VCO with Colpitts oscillator core and a buffer amplifier in 250-nm InP HBT technology was presented. All IC circuit is designed using EM simulation (ADS). Load-pull technique is used to generate high power and high efficiency oscillator at H-band. Thus, designed H-band IC demonstrates sufficient performance (output power = 2.7 dBm, efficiency = 5.2 %) to be used as a signal source at H-band. Measured results of oscillator are slightly worse than simulated results. The output power and the oscillation frequency down-shifted. This phenomenon is due to additional parasitic components.

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REFERENCES

[1] P. H. Siegel, "Terahertz technology," in IEEE Transactions on Microwave Theory and Techniques, vol. 50, no. 3, pp. 910-928, March 2002.

[2] J. Kim, S. Jeon, M. Kim, M. Urteaga and J. Jeong, "H-Band Power Amplifier Integrated Circuits Using 250-nm InP HBT Technology," in IEEE Transactions on Terahertz Science and Technology, vol. 5, no. 2, pp. 215-222, March 2015.

[3] D. -W. Park, D. R. Utomo, B. Yun, H. U. Mahmood and S. -G. Lee, "A D-Band Power Amplifier in 65-nm CMOS by Adopting Simultaneous Output Power-and Gain-Matched Gmax-Core," in IEEE Access, vol. 9, pp. 99039-99049, 2021.

[4] N. Landsberg and E. Socher, "240 GHz and 272 GHz Fundamental VCOs Using 32 nm CMOS Technology," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 12, pp. 4461-4471, Dec. 2013.

[5] K. Eriksson, S. E. Gunnarsson, V. Vassilev and H. Zirath, "Design and Characterization of H-Band (220–325 GHz) Amplifiers in a 250-nm InP DHBT Technology," in IEEE Transactions on Terahertz Science and Technology, vol. 4, no. 1, pp. 56-64, Jan. 2014.

[6] S. Kang, J. -C. Chien and A. M. Niknejad, "A W-Band Low-Noise PLL With a Fundamental VCO in SiGe for Millimeter-Wave Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 10, pp. 2390-2404, Oct. 2014.

[7] D. Kim and S. Jeon, “A WR-3 band fundamental voltage-controlled oscillator with a wide frequency tuning range and high output power,” IEEE Trans. Microw. Theory Techn., vol. 67, no.7, pp. 2759–2768, Jul. 2019.

[8] D. Kim and S. Jeon, "A 300-GHz high-power high-efficiency voltage- controlled oscillator with low power variation," IEEE Microwave and Wireless Components Letters, vol. 30, no. 5, pp. 496-499, May 2020.

[9] J.-Y. Kim, H.-J. Song, K. Ajito, M. Yaita, and N. Kukutsu, “InP HBT voltage-controlled oscillator for 300-GHz-band wireless communications,” in Proc. Int. SoC Design Conf. (ISOCC), Nov. 2012, pp. 262–265.

[10] J. Yun, D. Yoon, H. Kim and J. -S. Rieh, "300-GHz InP HBT Oscillators Based on Common-Base Cross-Coupled Topology," in IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 12, pp. 3053-3064, Dec. 2014.

[11] M. Seo et al., "InP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THz," in IEEE Journal of Solid-State Circuits, vol. 46, no. 10, pp. 2203-2214, Oct. 2011.

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