A Fully Integrated Circuit for High Current Multiple-Output

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Abstract - **This paper presents a fully integrated circuit for high current multiple-output that can independently control supply voltage of several circuit building blocks. This work combines digital-to-analog converters (DACs) and low dropout regulators (LDOs) to offer a high output voltage resolution and a high output current capability. A resistor-floating-resistor-string DACs achieves a 10-bit resolution with a small silicon area. A multi-stage LDO removes voltage offsets with high loop gain and improves transient responses with high gain-bandwidth product. A test chip fabricated in a 0.18µm CMOS process achieves an output voltage range of 0.6 V to 1.3 V, maximum output current of 5 mA, voltage regulation accuracy of 0.7 mV with 1.8V V_{DD}.**

Keywords— **Digital-to-analog converter (DAC), low dropout regulator (LDO).**

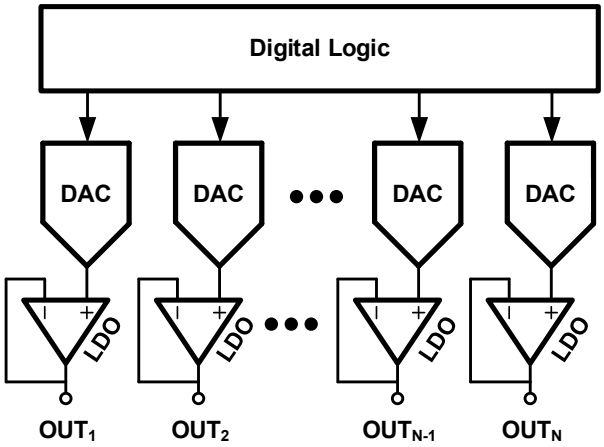

Fig. 1. Concept of a fully integrated circuit for high current multiple-output circuit.

I. INTRODUCTION

With the advancement of integrated circuit (IC) fabrication technology, circuit density has increased, leading to a continuous rise in power consumption per unit area. This has resulted in significant power wastage due to issues such as IR drop in the power delivery network. On the other hand, as ICs are becoming more complex, including multiple circuit types and optimal operating voltage and speed requirements varying for each circuit and at different times, fine-grained dynamic voltage-frequency scaling (DVFS) techniques are being widely adopted to improve power efficiency.

Fig. 1 shows a simplified architecture of a fully integrated circuit for high current multiple-output. Circuits such as optical phased array (OPA) drivers and column drivers require the ability to independently supply voltage and drive high output current. To drive multi-channel OPAs and columns, OPA drivers and column drivers require a small size. For each channel, the output voltage of the DAC is used as the reference voltage for the LDO to generate an independent voltage, which can drive the current required by the channel.

Fig. 2 shows a 6-bit resistor DAC (RDAC) with a two-stage structure. The MSB determines which resistor in the first ladder is connected to the buffer input. The output

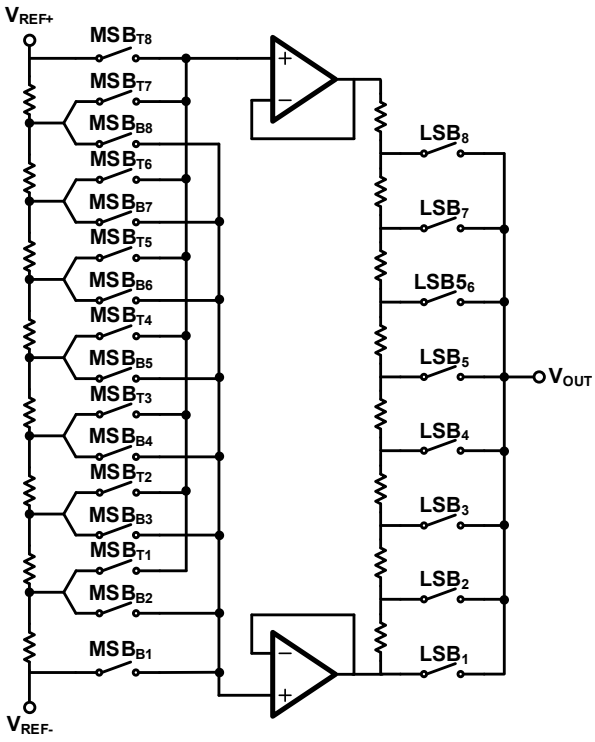

Fig. 2. 6-bit two-stage resistor DAC (RDAC) architecture.

voltage of the buffer is distributed through voltage division by the second resistor ladder, and the LSB selects the output voltage. The two-stage structure has higher area efficiency than a conventional single-stage DAC with the same number of bits. However, two-stage RDAC performance is limited by factors such as buffer offset and speed.

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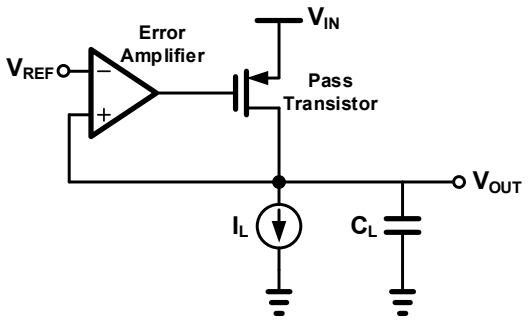

Fig 3. Conventional low dropout regulator.

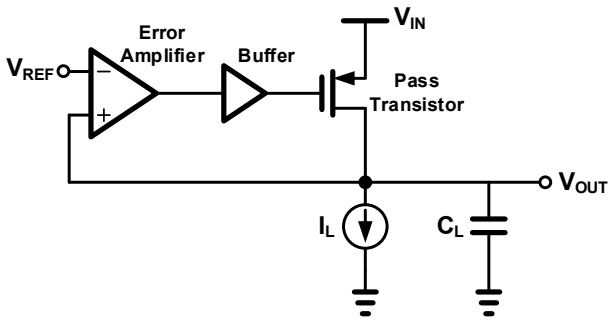

Fig. 4. Low dropout regulator with buffer impedance attenuation.

Fig. 3 shows a conventional LDO. LDOs typically consist of a feedback structure connecting an error amplifier, which amplifies the comparison between the output voltage and the reference voltage, to a pass transistor that supplies the output current. The final pass transistor primarily determines the maximum output current.

In order to meet the high current demands of recently designed high-performance circuit blocks, relatively large pass transistors are required, which in turn increases the gate capacitance of the pass transistor. While the output current density of transistors increases with the advancement of process nodes, the size of the gate capacitance of the pass transistor required for a certain output current drive is generally maintained constant without being affected by scaling. In particular, due to the decrease in circuit driving voltage and short-channel effects such as velocity saturation, there are limitations to obtaining additional drive current gain by increasing the overdrive voltage of the pass transistor. Moreover, if the overdrive voltage increases, the required source-to-drain voltage to operate the pass transistor in the saturation region also increases, resulting in additional power consumption, which can be particularly detrimental to recent low-voltage circuit operation.

Therefore, unless using a digital control method, the gate capacitance of the pass transistor is determined at a certain level regardless of the process when the output current is specified, and the gain-bandwidth product (GBW) and quiescent current of the error amplifier for the stability of the feedback loop are also determined accordingly.

Various research has been conducted to overcome the limitations and improve the performance and current efficiency of LDOs. Fig. 4 shows a method to amplify the output of the error amplifier using a unity-gain buffer with high bandwidth and use it to drive the pass transistor [1]. As the signal passes through the buffer, the output driving

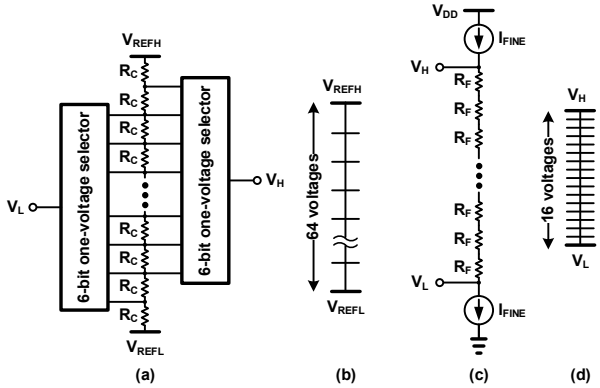

Fig. 5. 10-bit RFR-DAC (a) 6-bit RDAC (b) 6-bit RDAC voltage range (c) 4-bit floating resistor string DAC (d) 4-bit floating resistor string DAC voltage range.

capability is improved, resulting in an even higher GBW. However, additional current is required to drive the buffer for this purpose.

It is important to design the LDO with a high loop gain to improve the performance of LDOs such as line regulation and load regulation. As the output current of the LDO increases, the gain that can be obtained from the pass transistor, which is the last stage, decreases, resulting in a decrease in the loop gain. Therefore, to obtain the desired loop gain at all possible output currents, it is necessary to obtain sufficient loop gain from the error amplifier.

The remainder of this paper is organized as follows. Section II elaborates a detailed architecture of this work. Section III provides measurement results from a test chip fabricated in 0.18 μm. Then section IV draws the conclusion.

II. CIRCUIT IMPLEMENTATION

A. Resistor-Floating-Resistor-String DAC (RFR-DAC)

The conventional second-stage RDAC consists of two RDACs connected in a cascaded manner, where a buffer is employed to separate the resistor string of the first RDAC from the loading effect of the second RDAC. The design of the buffer becomes a burden that determines the performance of the DAC. To minimize this problem, the resistor-floating-resistor string DAC (RFR-DAC) is adopted in this work [2]. The RFR-DAC is composed by serially connecting an RDAC and a floating resistor string DAC. The floating resistor string DAC corresponding to the second stage uses current sources/sinks, showing a very high impedance and adding negligible load to the resistor string of the first stage RDAC, thus minimizing loading effect issue. Fig. 5 shows a 10-bit RFR-DAC. The 6-bit voltage selector selects the adjacent node voltages of two resistor strings in the first stage and connects them to the top and bottom of the floating resistor string. Although there is a current flowing in the switch that connects the top and bottom of the floating resistor string, it can be ignored due to the high impedance effect of the floating resistor string.

The RFR-DAC in Fig. 6 is presented for analyzing errors caused by switch resistance and current source/sink finite resistance. The symbol R_C denotes the segment resistance of the first-stage (coarse) resistor string, and R_F represents the

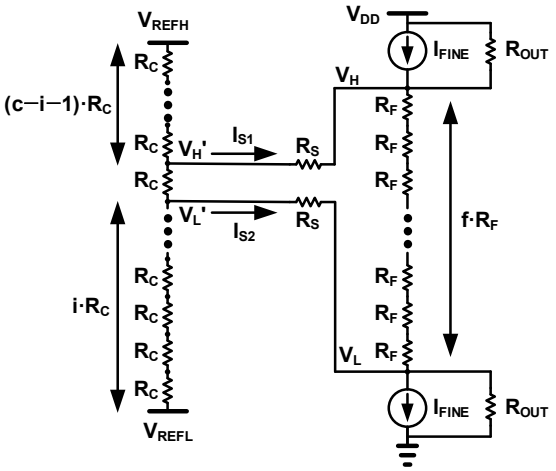

Fig. 6. Simplified RFR-DAC for analyzing errors caused by switch resistance and current source/sink finite resistance.

segment resistance of the second-stage (fine) resistor string, and R_S represents the on resistance of the voltage selector. The output resistance of the current source and sink are represented by R_{OUT}. The notation c denotes the number of first-stage resistor string, and f represents the number of second-stage resistor string, and i represents the number of first-stage resistor string from V_{REFL} to V_L'. The voltage difference between V_H and V_L is denoted as

$$V_H - V_L = (V_H' - V_L') - I_{S1}R_S + I_{S2}R_S = \frac{(V_{REFH} - V_{REFL})}{c} - \frac{I_{S1}(i+1)(c-i-1) - I_{S2}i(c-i)}{c}R_C - I_{S1}R_S + I_{S2}R_S. \quad (1)$$

The second, third, and fourth terms of (1) represent error voltages due to the effects of the switch and finite impedance of the floating resistor string (second-stage) RDAC. These error voltages are somewhat small because they are canceled out by similar values of I_{S1} and I_{S2}.

B. Three-Stage Low Dropout Regulator (LDO)

Using amplifier structures with multi-stage, such as Nested Miller compensation, enables the design of LDO structures with high loop gain, resulting in high-performance line and load regulation [3]. It also allows for a higher GBW than traditional 2-stage LDO designs. The improved GBW enables the design of 3-stage LDOs with improved transient response compared to traditional 2-stage LDOs. The design of multi-stage amplifiers with Miller compensation structures is still being researched [4]. Utilizing existing research results, a 3-stage LDO design for high current output can be achieved.

Fig. 7 shows the 3-stage LDO structure. By assuming $g_{mP} >> g_{m1}$ and g_{m2}, the transfer function of the 3-stage LDO is given by

$$A_V(s) = \frac{A_0}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)} \quad (2)$$

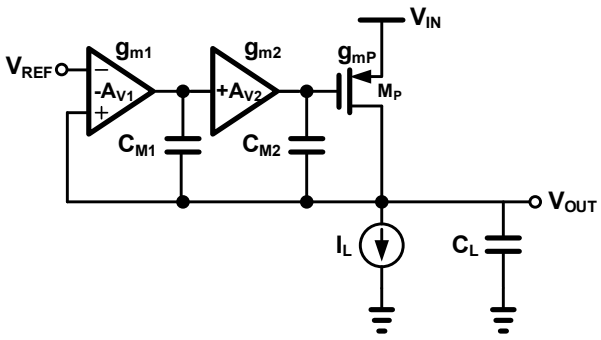

Fig. 7. 3-Stage LDO structure

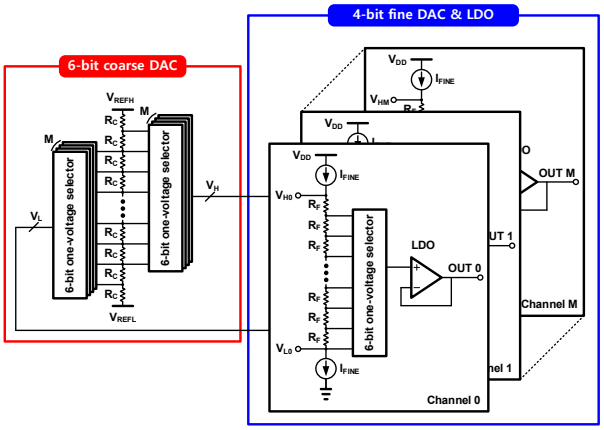

Fig. 8. Architecture of a fully integrated circuit for high current multiple-output circuit.

where

$$A_0 = g_{m1}g_{m2}g_{mP}R_{o1}R_{o2}R_{oL}. \quad (3)$$

$$\omega_{p1} = \frac{1}{C_{M1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}}. \quad (4)$$

$$\omega_{p2} = \frac{g_{m2}}{C_{M2}}. \quad (5)$$

$$\omega_{p3} = \frac{g_{mP}}{C_L}. \quad (6)$$

The assumption of $g_{mP} >> g_{m1}$ and g_{m2}, made earlier, is reasonable for LDOs that use a large pass transistor. The GBW can be obtained from the equations presented in (3) and (4), where $GBW = A_0\omega_{P1} = g_{m1}/C_{M1}$. To ensure stability, the nondominant poles are designed to be located at $\omega_{P2} > 2GBW$ and $\omega_{P3} > 4GBW$, with a phase margin of at least 50 degrees.

C. Top-Level Architecture

Fig. 8 shows the top-level architecture of the DAC and LDO described in sections A and B of Section 2. The DAC is implemented with a 2-stage structure consisting of a 6-bit coarse DAC and a 4-bit fine DAC to improve area efficiency. The 6-bit coarse RDAC is implemented as a global resistor string to maximize area efficiency, and the 4-bit fine RDAC is implemented as a floating resistor string that is free from performance limitations in the buffer. Each channel uses two independent 6-bit voltage selectors to

TABLE I. Simulated current and power consumption in key building blocks for 16 channels

		Static current (uA)	Static power (mW)
16 DACs	1 coarse RDAC	35.63	0.0256
	16 fine RDAC	66.05	0.1189
	Voltage selector	0.0174	0.0000313
16 LDOs		4,550.4	8.191

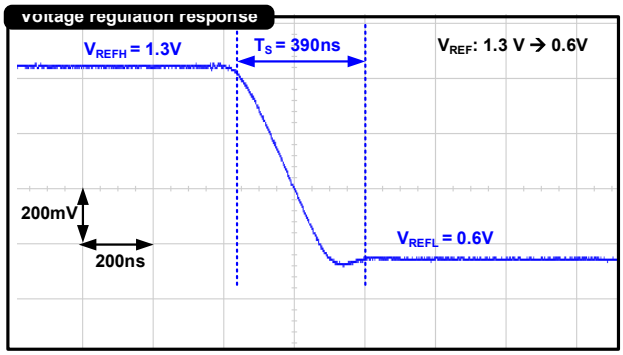

Fig. 9. Voltage regulation response with V_{REF} changing from = 1.3V to 0.6V.

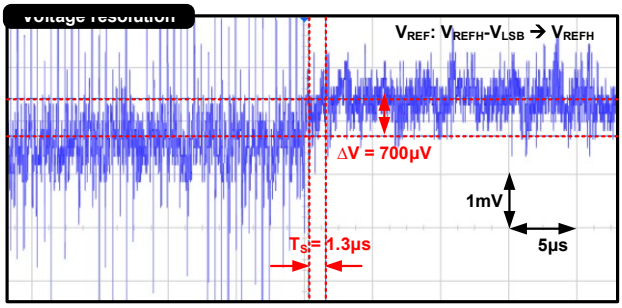

Fig. 10. Voltage regulation accuracy with V_{REF} changing from = 1.3V – V_{LSB} to 1.3V.

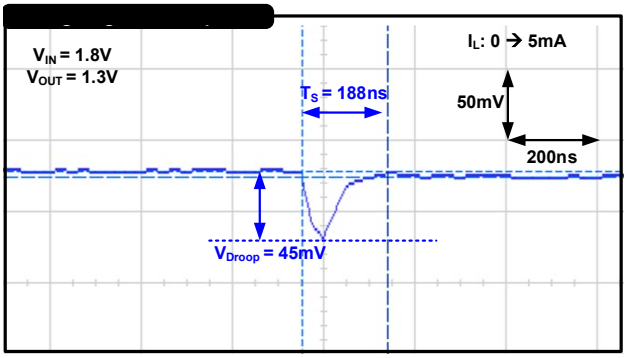

Fig. 11. Voltage regulation response with I_L changing from 0 to 5mA.

select the voltages (V_H and V_L) required by each 4-bit fine RDAC from the 6-bit coarse RDAC. Due to the high impedance using RFR-DAC structure in the second-stage, the voltage error of the first-stage caused by driving several second-stage can be ignored. The LDO receives the output voltage of the DAC as a reference voltage and supplies the required voltage and current to the load. The 3-stage structure of the LDO, based on high loop gain and GBW, provides high accuracy and fast transient response.

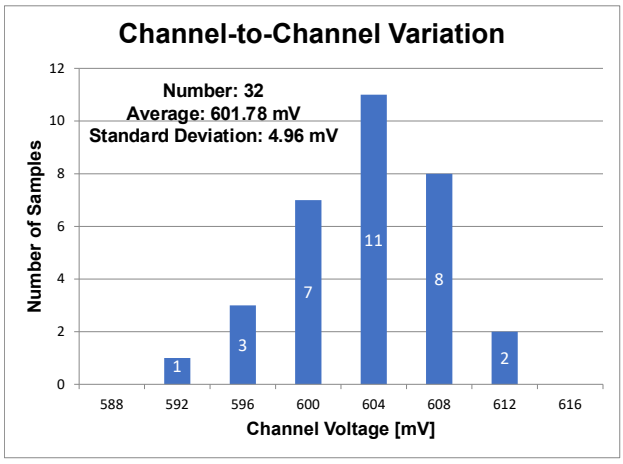

Fig. 12. Channel-to-channel variation of output voltage in one chip.

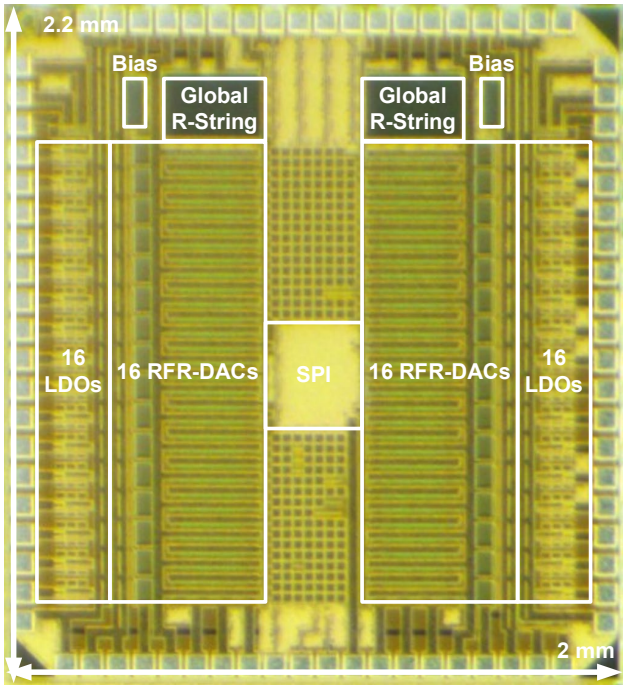

Fig. 13. Die micrograph of 0.18 μm CMOS test chip.

III. RESULTS AND DISCUSSIONS

This section presents the measurement results of a test circuit manufactured in 0.18 μm process. Table I denotes simulated current and power consumption of each block for 16 channels. The results indicate that the test chip consumes about 0.52mW per channel. Fig. 9 shows the voltage control response time for the circuit, which has an output voltage range of 1.3 V to 0.6 V. The reaction time was tested by changing the DAC's output from the maximum voltage (V_{REFH} = 1.3 V) to the minimum voltage (V_{REFL} = 0.6 V), and it was confirmed to be 390 ns. Fig. 10 demonstrates the voltage control accuracy, showing a difference of 1 LSB in the output voltage when applying a digital input with a difference of 1 LSB to the DAC. The voltage difference (ΔV) was confirmed to be 1 LSB, corresponding to the designed value of 700 μV. The load transient response performance was measured by applying an instantaneous current of 5 mA, which is the maximum value per channel, and the

measurement result is presented in Fig. 11. The circuit showed a setting time of 188 ns and a load regulation performance of 0.875 mV/mA. To evaluate the effect of process variation and mismatch, the channel-to-channel variation of the output voltage at V_{REFL} was measured, and the histogram of the channel-to-channel variation is shown in Fig. 12. For one chip, the standard deviation of the channel-to-channel variation was found to be 4.96 mV, and the average was 601.78 mV. The chip micrograph in 0.18 μm CMOS is shown in Fig.13.

IV. CONCLUSION

This paper proposes a fully integrated high-current multiple-output system that combines the functionalities of a DAC and an LDO. The global resistor string and 2-stage RFR DAC architecture are used to improve area efficiency, while the 3-stage LDO architecture provides high accuracy and fast transient response. The proposed system can be expanded to a larger number of channels by simply adding more 2-stage DACs and LDOs without the need for circuit redesign.

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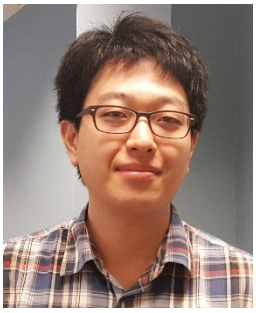

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