K-band CMOS High-Power Harmonic Response Rectifier for Nonlinear Detection based Wireless Power Transfer

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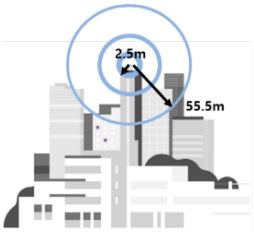
Abstract **- This paper presents a K-band CMOS harmonic response rectifier based on 2-stage cross coupled bridge rectifier. The proposed CMOS harmonic response rectifier configured with rectification stage and second harmonic output stage can be used for nonlinear detection based wireless power transfer. The transformer in the rectification stage did not only generate differential signal but also matched to 50 Ω at a fundamental frequency to achieve low transmission loss for high power conversion efficiency (PCE) and conversion gain (CG). To maximize CG, the second harmonic stage was matched to 50 Ω at second harmonic frequency. The proposed CMOS harmonic response rectifier was designed using a 65 nm CMOS process and had a chip area of 0.35 mm x 0.22 mm. The simulation results show that the PCE was 15.2–20.2 %, and the CG was -23–-21.2 dB at an input power of 25.5 dBm in the frequency range of 20.5–27 GHz.**

Keywords—**Cross coupled bridge rectifier, harmonic backscattering, millimeter wave, wireless power transfer (WPT)**

I. INTRODUCTION

Millimeter wave (mmWave) wireless power transfer (WPT) has gained increasing attention with the development of 5G communication. It is important to improve power transfer efficiency in mmWave WPT. The factors that determine the power transfer efficiency are the accurate transfer of power toward a charging target and the power conversion efficiency (PCE) of rectifiers. The retro-directive technique was proposed because the power transmitter basically does not know where the power receiver is located. The power transfer efficiency of the retro-directive technique, which transfers power automatically toward a charging target, is reduced by additional power consumption caused by the emission of isotropic pilot signals from the charging target for detecting its location [1]. Recently, to solve the problem on power consumption, harmonic backscattering rectifiers, which detect the positions of charging targets by utilizing harmonic signals or intermodulation signals generated through the rectifiers,



* FSPL : Free space path loss

d	2 m	20m
EIRP	85 dBm	85 dBm
FSPL (@24GHz)	66.1 dB	86.1 dB
G_r	10 dBi	10 dBi
P_r	28.9 dBm	8.9 dBm

Fig. 1. Hypothetical mmWave WPT scenario for a macro cell with tabulated link budget.

have been used in microwave WPT research [2]–[13]. High DC power can be obtained by maintaining high power transfer efficiency through automatic transfer of power to the correct location of the charging target without additional power consumption by applying a harmonic back scattering rectifier to WPT.

The PCE of the rectifier is emphasized to have a wide input power and frequency range in mmWave WPT system as Microwave WPT, because it is affected by the input power change according to the charging distance and by the frequency range according to a wideband signal at various center frequencies [14]–[16]. The conventional CMOS rectifier, that could not be harmonic response, have been proposed for mmWave WPT [17]-[18].

In [17], a 3-stage Dickson charge pump with a diode-connected MOSFET was introduced. Even though it had a peak PCE of 15.6% at high input power of 12 dBm in 26 GHz, it did not achieve a high PCE under a wide input power range. A cross coupled bridge rectifier based on a 3-stage transformer was proposed in [18] for operating at various frequency ranges. It can match to 50 Ω about both frequency of 38/60 GHz, but it could not have a high PCE under a wide input power range.

In this letter, we integrate the harmonic backscattering rectifier structure from microwave WPT into the mmWave harmonic response rectifier for nonlinear detection based WPT applications. The proposed novel CMOS high power harmonic response rectifier was composed of 2-stage cross coupled bridge rectifier based rectification stage and second harmonic output stage that has nonlinear response. The rectification stage was matched to 50 Ω using a transformer based matching network (TFBMN) at a fundamental frequency to achieve the PCE over 15 % at input power range of 12–32.5 dBm at 24 GHz and frequency range of 20.5–27 GHz at 25.5 dBm.

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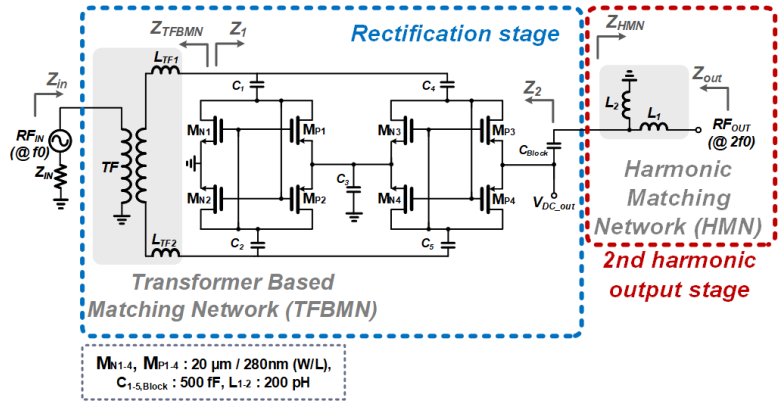


Fig. 2. Schematic of the proposed harmonic response rectifier

The second harmonic output stage was designed to match the second harmonic signal generated by the MOSFET in the rectification stage. This facilitated the efficient delivery of power to the second harmonic output port, minimizing transmission loss and contributing to a high conversion gain (CG) exceeding -25 dB across a frequency span of 20–29 GHz. The proposed CMOS harmonic response rectifier can transfer power to the location of the charging target without additional power consumption, and it achieves high PCE at a wide input power and frequency range, thereby improving wireless power transfer efficiency.

II. DESIGN METHODOLOGY

In [19], the maximum available effective isotopically radiated power (EIRP) in the 24 GHz band was 85 dBm. The power received by a charging target varied from 28.9 dBm to 8.9 dBm when the distance between the transmitter and the charging target changed from 2 m to 20 m, as shown in Fig. 1. The proposed harmonic response rectifier was designed a goal of having high PCEs at wide input power and frequency ranges to maintain high rectification efficiency for various modulated signals from short to long distances.

The proposed CMOS harmonic response rectifier does not only rectify the received fundamental signals but also backscatters the second harmonic signals for nonlinear detection based WPT. Fig. 2 shows a schematic of the proposed circuit comprised of rectification stage and second harmonic output stage. In the rectification stage, we used 2-stage cross coupled bridge rectifier to achieve high PCEs at the wide input power range and TFBMN with less transmission loss because that is not required additional matching network.

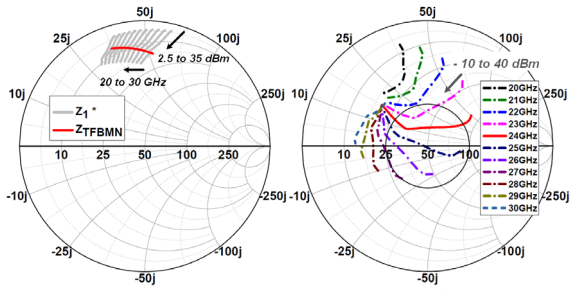
A 2-stage cross coupled bridge rectifier core was composed of a diode, designed using MOSFETs with a gate width of 20 μm and a length of 0.28 μm to operate at high input power levels, and the C_1–C_5 capacitors with 500 fF.

The proposed TFBMN can perform complex matching to Z_1 in the frequency range of 20–30 GHz at the input power of 25.5 dBm to achieve high PCEs at a wide frequency range as shown in Fig. 3(a).

Furthermore, the input impedance Zin was strategically positioned within the voltage standing wave ratio (VSWR) circle of 2 across the expansive frequency span of 23–27 GHz. Likewise, it remained within the VSWR circle of 2 across a broad input power range, spanning from 4 dBm to 33.5 dBm at 24 GHz. These characteristics are illustrated in Fig. 3(b).

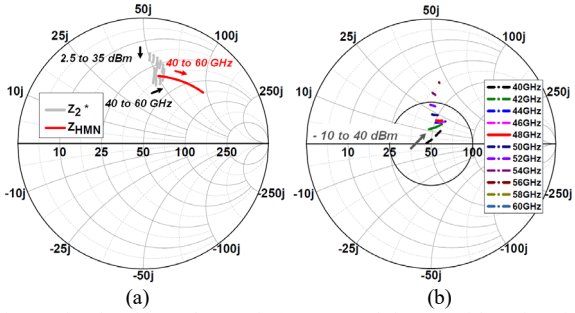
The conventional CMOS rectifier include a bypass capacitor to eliminate harmonic signals generated by nonlinear devices like MOSFETs or diodes. We added a second harmonic output port after the 500 fF DC Block capacitor (C_{Block}) and used the second harmonic signal, which was not used in previous studies on rectifiers, to increase WPT efficiency. A harmonic matching network (HMN) composed of series (L_1) and shunt (L_2) inductors, which were 200 pH, was used for matching to 50 Ω about second harmonic frequency.

The HMN impedance Z_{HMN} was matched with the complex impedance Z_2^* of Z_2 in Fig. 2 in second harmonic frequency range of 40–48 GHz, as shown in Fig. 4(a). The output impedance Z_{out} was located inside of VSWR = 2 circle in the wide frequency range of 40–52 GHz, the second harmonic frequencies, and in the wide input power range of -10–40 dBm, as shown in Fig. 4(b).



(a) (b)

Fig. 3. Simulated impedance of (a) TFBMN and (b) Z_{in} with various input power and frequency ranges.



(a) (b)

Fig. 4. Simulated impedance of (a) HMN and (b) Z_{out} with various input power range and second harmonic frequencies.

TABLE I. Comparison of recently reported mmWave rectifiers.

		[17]**	[18]**	[20]**	[21]**	This work
Tech.		CMOS 65nm	CMOS 40nm	CMOS 65nm	Schottky diode (MA4E2054A)	**CMOS 65nm**
Input power range for PCE > 15 % (dB)		N.A	N.A	14*	11*	**23.5**
Peak PCE.	PCE (%)	15.6	8.1 / 4.6	36	35	**20**
	Power (dBm)	12	-7.8 / -6.6	15	18	**25.5**
	Freq. (GHz)	26	38 / 60	35	25	**24**
The freq. range for peak PCE > 15 % (GHz)		26–28	N.A	29–40	N.A	**20.5–27**
Input power range for CG > -25 dB (dB)		N.A	N.A	N.A	N.A	**26.5**
Peak CG.	CG (dB)	N.A	N.A	N.A	N.A	**-21.3**
	Power (dBm)	N.A	N.A	N.A	N.A	**26.5**
	Freq. (GHz)	N.A	N.A	N.A	N.A	**24**
The freq. range for peak CG > -25 dB (GHz)		N.A	N.A	N.A	N.A	**20–29**
Size(mm^2)		0.4 x 0.25	0.19 x 0.135	0.43 x 0.27	N.A	**0.35 x 0.22**

*: graphically estimated, **: measurement results.

III. RESULTS AND DISCUSSIONS

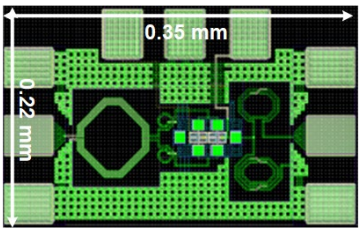


Fig. 5. Layout of the proposed harmonic response rectifier.

The proposed harmonic response rectifier was designed using a 65-nm RF-CMOS process, and it has a 0.35 × 0.22 mm^2 chip size, as shown in Fig. 5. We simulated and then selected an extrinsic optimum DC load impedance of 680 Ω.

The PCE can be obtained by P_{dc_out} / P_{in} × 100%, where P_{dc_out} represents the output dc power of the rectification stage, and P_{in} stands for the input power of the proposed harmonic response rectifier. The CG was calculated by P_{harm_out} *(dB)* - P_{in} *(dB)*, where P_{harm_out} corresponds to the second harmonic power of the second harmonic output stage.

Fig. 6(a) shows the simulated PCE and CG at 24 GHz across various input power levels. The peak PCE was 20.1 % at an input power of 25.5 dBm. PCE was over 15 % in a wide input power range of 12–35.5 dBm at 24 GHz. The peak CG at 24 GHz was -22.9 dB at an input power of 26.5 dBm. CG was over -25 dB in wide input power range of 7.5–34 dBm at the same frequency. Fig. 6(b) shows the simulated PCE and CG at different frequencies with an input power of 25.5 dBm. PCE was over 15 % in a wide frequency range of 20.5–27GHz at 25.5 dBm. CG was over -25 dB in a wide frequency range of 20–29 GHz at the same input power level.

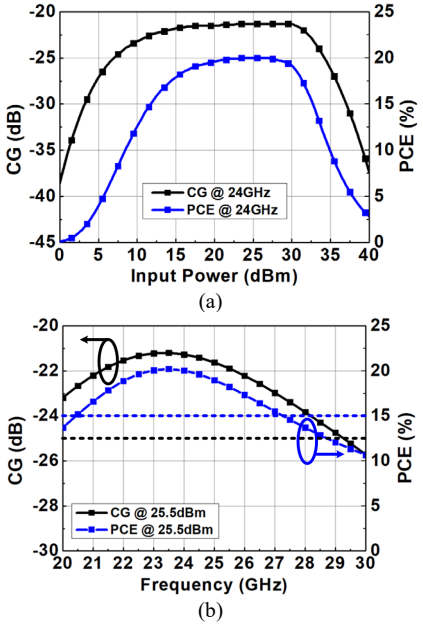
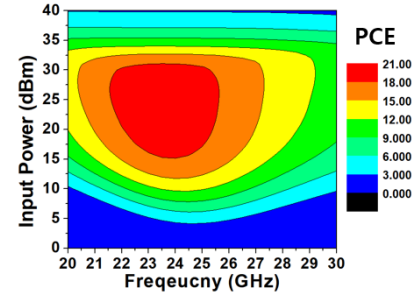
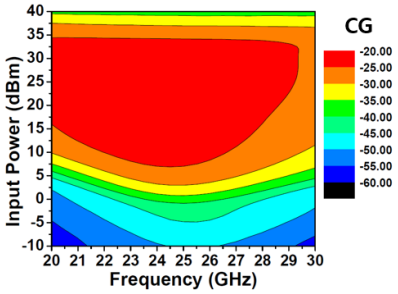


Fig. 6. Simulated PCE and CG (a) with different input power levels at 24 GHz (b) with different frequencies at the input power of 25.5 dBm.

When the input power level was changed from 20 to 30 dBm, the proposed circuit achieved a the PCE over 18 % across the frequency range of 21–27 GHz, as shown in Fig. 7(a). It achieved a CG over -25 dB in frequency range of 20–27.5 GHz, when the input power was changed from 15 to 32.5 dBm, as shown in Fig. 7(b).

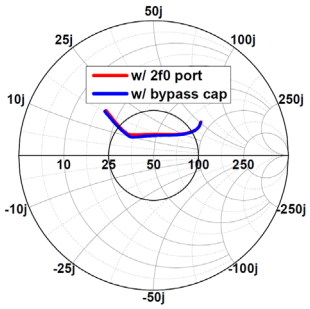


(a)

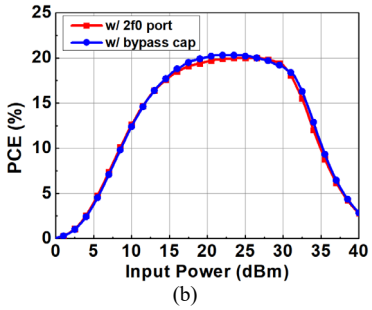


(b)

Fig. 7. Simulated (a) PCE and (b) CG with various input power and frequency range.



(a)



(b)

Fig. 8. Simulated (a) input impedance with the second harmonic output port versus with a bypass capacitor at 24 GHz (b) PCE with the second harmonic output port versus with a bypass capacitor at 24 GHz.

Fig. 8(a) provides a comparison between the input impedance when there is a second harmonic output port and when there is a bypass capacitor without a second harmonic output port. It shows that the second harmonic output port of the proposed harmonic response rectifier did not influence the input impedance. Therefore, the performance of PCE was not affected by the presence or absence of the second harmonic output port, as shown in Fig. 8(b).

The harmonic response rectifier was not presented in previous mmWave circuit studies therefore, we compared the proposed harmonic response rectifier with the previous mmWave rectifiers, as shown in Table 1. It achieves more than 15% PCE for a wider input power range than [17]–[18] and [20]–[21], despite the proposed harmonic response rectifier has a lower peak PCE than [20]–[21]. The PCE of the proposed harmonic response rectifier was superior to that in [17]–[18] and [21] in terms of operation frequency range.

IV. CONCLUSION

In this study, a 65-nm CMOS harmonic response rectifier for nonlinear detection based wireless power transfer was presented. The proposed harmonic response rectifier can match to 50 Ω at a fundamental frequency using a TFBMN with less transmission loss and emit second harmonic signal generated by the rectification stage using a HMN. The proposed TFBMN is used to achieve high performance of the PCE and CG in same input power level by having low transmission loss. The simulated peak PCE and CG were 15.2–20 % and -23–-21.2 dB, respectively in 20.5–27 GHz frequency range. Therefore, the proposed circuit can have superior rectifying and frequency conversion performances from fundamental to second harmonic about wide frequency ranges and input power levels.

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