Capless Low-Dropout Regulator with Voltage Damper and Body Bias Feedback with Fast Transient Response

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Abstract **- This paper presents an output cap-less low-dropout regulator (LDO) using a voltage damper and body bias feedback for fast load transient response. The voltage damper makes load transient fast. To make the LDO react to relatively slow distortion of the output, the body bias feedback is included. The proposed LDO regulator is fabricated in a 0.18μm CMOS process with an active area of 0.026mm2 and an on-chip capacitance of 9.32pF. The operating conditions are set to an input voltage of 1.8V, a maximum load current of 100mA, and an output voltage of 1.6V. The maximum undershoot was 284 mV and the maximum overshoot was 199 mV.**

Keywords**—Fast load transient, Low-dropout regulator (LDO), Voltage damper**

I. INTRODUCTION

Due to the advancements in chip fabrication that allow for the integration of multiple circuits onto a single chip, power management integrated circuits (PMICs) are becoming increasingly important to support advanced chip applications [1]. As multiple modules can be integrated on a single chip, PMICs must support multiple voltage supplies.

In electronic and electrical systems, power supplier and regulator are essential components and cannot function properly without stable energy supply. DC/DC converter and LDO regulator are used as an internal power supply unit on chip. Therefore, LDO regulator must be able to output stable voltage by default, while supporting various voltage supplies. To achieve this, LDO regulator must always be on, making query current an important factor in power efficiency.

There are various types of PMICs such as LDO, DC-DC converter, buck converter, and charge pump. Among them, LDO has the advantage of having a simple circuit structure. As can be seen in Fig. 1. (a), a conventional LDO consists of only a few components such as an error amplifier and a main transistor, which can be NMOS or PMOS. The PMOS is commonly used. Additionally, there is also an output capacitor, which helps to ensure transient response and stability of the system, providing a more stable and accurate output voltage.

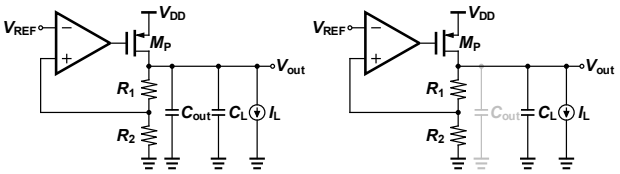

Fig. 1. Conventional LDO regulator (a) with output capacitor (b) without output capacitor (capacitor-less LDO).

However, recently, as part of the technology to improve chip integration, studies on LDO structures without output caps, as shown in Fig. 1. (b), are actively underway [2]-[8]. The reason why the capless LDO is more popular than the conventional one is as follows. Due to the bulky size of the output capacitor required in conventional circuit, it is difficult to integrate them on System-on-Chip (SoC). However, by removing this capacitor, it becomes possible to significantly reduce the area and integrate the circuit within the SoC. Also, if the area is reduced, the chip fabrication cost and PCB production cost are also reduced accordingly.

Unfortunately, it also has some drawbacks in the capless LDO regulator. These are problems that arise because there is no output capacitor, which is contrary to what was mentioned earlier. To see the critical issues in the design, first, there is a stability issue under light load conditions. Second, load transient performance is not well indicated because over/undershoot causes signal degradation [9].

To overcome the drawbacks and integrate the LDO into SOC to operate stably, it is necessary to devise a circuit-level solution inside the chip. In particular, to improve the fast load transient, this paper proposes the capless LDO regulator using voltage damper and body bias feedback.

To operate the LDO regulator stably and integrate it into SOC while overcoming its drawbacks, a circuit-level solution inside the chip is necessary. One of the issues that needs improvement is load transient, which can be achieved by using Voltage Damper (VD) and Body Bias Feedback (BBF). The voltage damper is inserted for feedback the transition of the load condition into M_P, allowing it to respond quickly to changes in load condition and achieve fast transient response. The body bias feedback is applied to

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hold bias of the M_P's body bias, lowering its threshold voltage and increasing its current drivability, thereby overcoming the drawbacks.

To overcome the shortcomings and limitations of the capless LDO, this paper proposes the capless LDO regulator using voltage damper and body bias feedback. The paper is organized as follows: The brief concept and design of the fundamental circuit blocks are presented in Section II. The simulation results are explained in Section III. Finally, a conclusion is presented in Section IV.

II. DESIGN METHODOLOGY

A. Basic concept of the proposed LDO regulator

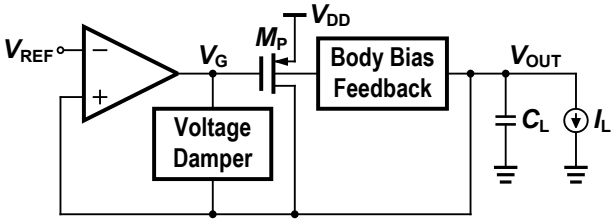

Fig. 2. Block diagram of the proposed LDO regulator.

The block diagram of the proposed LDO regulator is shown in Fig. 2. The proposed LDO regulator is composed of the pass transistor (M_P), the operation amplifier (op-amp), voltage damper (VD), and body bias feedback (BBF). The load for the test is modeled as a combination of a current source (I_L) and a capacitor (C_L).

A cascoded op-amp used in the circuit was designed to operate in the subthreshold region so that it can save power consumption and ensure high DC gain. The proposed op-amp operates as an error amplifier that amplifies the difference between V_{load}, the output voltage of the LDO regulator, and V_{ref}, the reference voltage. The output value is fed back to the gate of M_P to adjust the drain current of MP and make the output voltage closer to V_{ref}. The voltage damper (VD) is placed between the output node and the gate node of M_P to detect changes in load conditions and provide feedback to M_P. The body bias feedback (BBF) is placed to fix the body bias of M_P, which lowers the threshold voltage, therefore increasing the current flowing through M_P. Thus, each component works well together to optimize the transient response and enable fast operation.

B. Voltage Damper

When using a capless LDO, a structure that can handle the voltage spike previously absorbed by the output node's large capacitor is required since a large capacitor is not used. In this circuit, voltage damper is applied to regulate the output voltage during load transitions, enabling fast load transient response. The detailed circuit diagram of the proposed voltage damper can be seen in Fig. 3. The VD circuit can be divided into two parts: the overshoot damper and the undershoot damper. The VD input node is connected to the

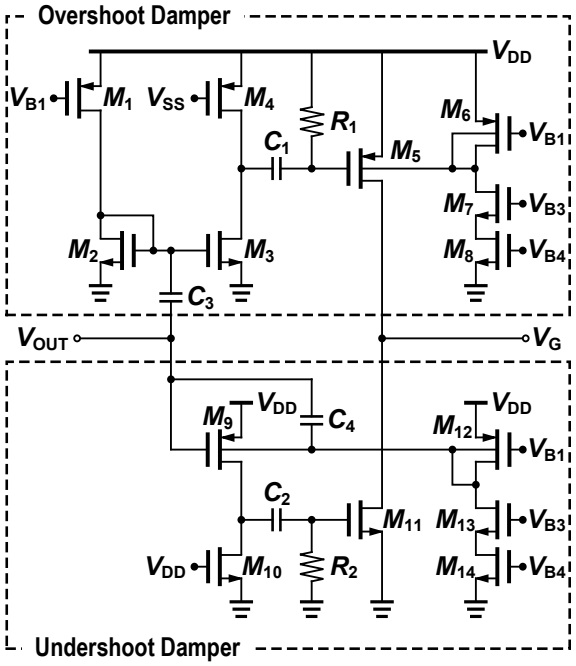

Fig. 3. Detailed circuit diagram of the proposed voltage damper.

LDO output node, and the VD output node is connected to the gate node of the pass transistor. There are two caps, C2 and C3, at the VD input, which block the DC signal coming in.

The overshoot damper is designed to receive the input signal through the input capacitor C3. When there is overshoot in the output voltage(V_{OUT}), which is the input of the VD, it is transferred to the gate of M2 and M3 through C3. The gate of M3 pulls down the drain of M3 and M4. The output undershoot of the inverter is then transferred to M5 through C1. Subsequently, current flows to the gate of the pass transistor for a short period via M5, resulting in lower current drivability of the pass transistor. As a result, the output overshoot of the LDO regulator is reduced.

The undershoot damper is designed to receive the input signal through the input capacitor C4 and the gate of M9. The drain node of M9 and M10 is biased to a low level. The output undershoot voltage (V_{OUT}), which is the input of the VD, is transferred to the body of M9 through C4. The sudden drop in body of M9 pulls up the drain node of M9 and M10. The rise in the output of the drain node of M9 and M10 is then transferred to M11 through C2. The current flows through M11 to the gate of the pass transistor for a short period. This operation increases the current drivability of the pass transistor, resulting in a reduction of the output undershoot of the LDO regulator.

C. Body Bias Feedback

The body bias feedback (BBF) is a feedback loop structure controlling the body bias of the pass transistor MP. Conventional LDOs do not control the body bias, but there are two advantages to adding this feature: (1) It increases the current drivability of MP. (2) It can regulate the relatively

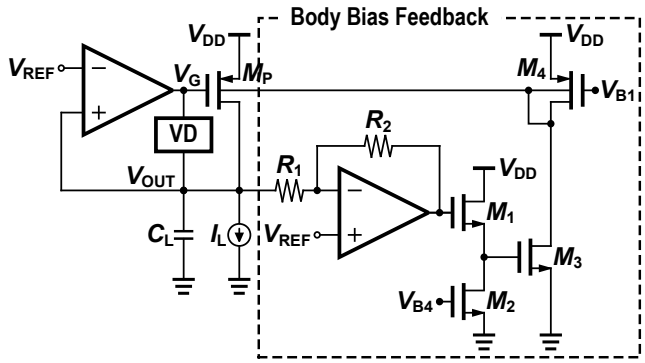

Fig. 4. Detailed circuit diagram of the body bias feedback.

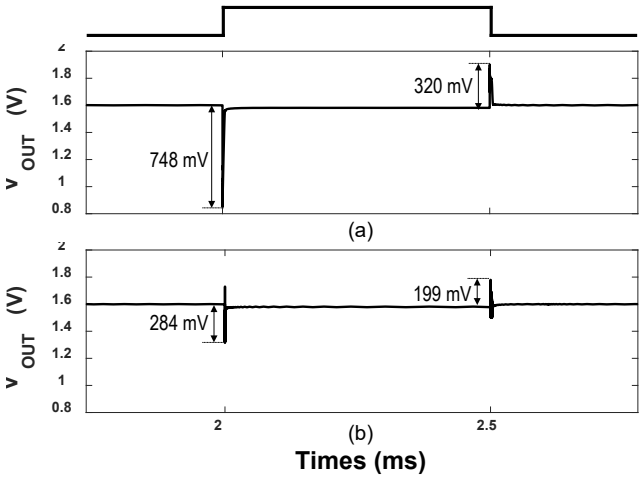

Fig. 5. Load transient response of the proposed LDO for load step of 0.2–100mA with 100ns load current step edge time (a) without VD and (b) with VD.

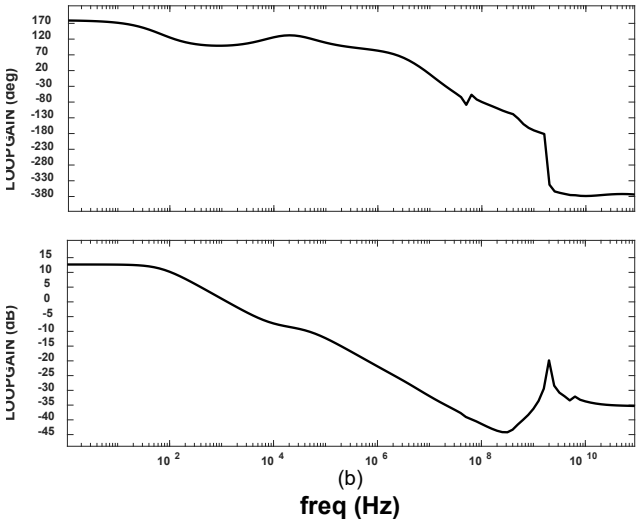

Fig. 6. Proposed LDO regulator stability response.

slow changes in the LDO [10].

The primary function of the body feedback is to increase the current drivability of the pass transistor. The body bias feedback (BBF) utilizes an op-amp, resistors R1 and R2, and transistors M1-4 to achieve this. The inverting op-amp, composed of the op-amp and resistors R1 and R2, generates an output that is fed to the gate of M1. The source follower, which is made up of M1 and M2, acts as a voltage-level shifter to decrease the quiescent current of the common source (CS) stage consisting of M3 and M4 by reducing the gate voltage of M3. The CS stage contains a PMOS current source load, with its body connected to the drain. The body-biasing load maintains the body bias of the pass transistor, which is slightly lower than the supply voltage level. This lowers the threshold voltage of the pass transistor, allowing it to carry a larger current.

The body bias feedback has a second role of regulating the relatively slow changes in the output voltage of the LDO regulator. Input through two capacitors C3 and C4 prevents the voltage damper from feeding back low-speed ripple to the pass transistor due to the design of both overshoot and undershoot dampers. However, the body bias feedback weakens the slow distortion of the output voltage. Ripple in the LDO output voltage is amplified through the feedback system and applied to the body of the pass transistor through M1. Since the body of the MOSFET operates as the gate [11], the input distortion of the body bias feedback negatively feeds back to the output of the LDO regulator, thereby removing the disturbance.

III. RESULTS AND DISCUSSIONS

The proposed circuit was simulated in the TSMC 180nm CM process. A step load current is applied to VOUT from 0.2 to 100 mA, with a step size of 99.8 mA and a rise/fall time of 100 ns. The input voltage of the LDO regulator is 1.8 V, and the regulated output voltage is 1.6 V.

Fig. 5. demonstrates the necessity of the voltage damper by comparing the load transient response of the proposed LDO regulator with and without voltage damper for a load step of 0.2 − 100mA with 100ns edge time. Subfigure (a) shows the load transient response without voltage damper, while subfigure (b) shows the load transient response with voltage damper. The proposed LDO regulator without VD exhibits an undershoot of 748mV and an overshoot of 320mV at the output voltage of 1.6V. However, the undershoot and overshoot output voltages of the proposed LDO regulator with VD are significantly reduced to 284mV and 199mV, respectively.

Fig. 6. displays the frequency response of the proposed LDO. It exhibits a DC gain of 20.22 dB and a phase margin of 81.472 deg. Fig. 7 illustrates the PSRR characteristics of the proposed LDO regulator. The PSRR values at different frequencies are shown in the plot: -76.37dB at 1Hz, -76.37dB at 10Hz, -65.85dB at 100Hz, -46.21dB at 1kHz, -29.94dB at 10kHz, -21.05dB at 100kHz, and -3.289dB at 1MHz. The PSRR of the LDO regulator system was verified and validated against input noise.

The completed layout photo, except for the pads, is shown in Fig. 8. It has a size of 245μm×147μm. Among the

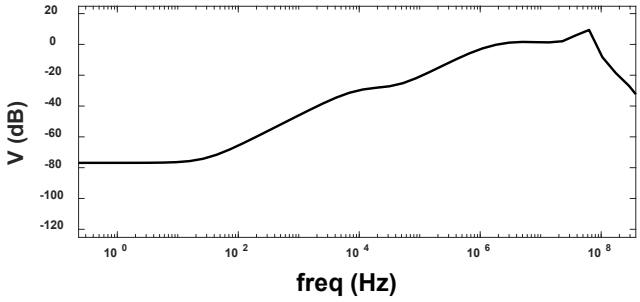

Fig. 7. PSRR of Proposed LDO regulator.

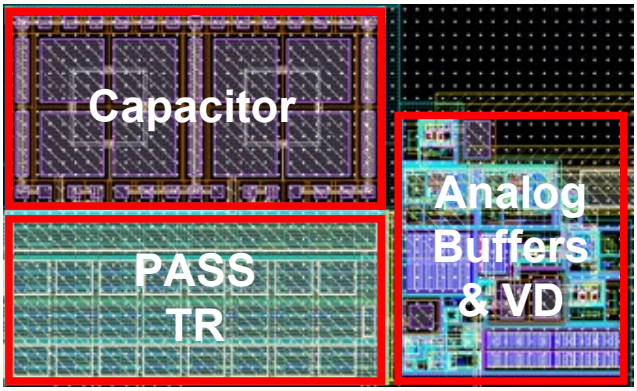

Fig. 8. Layout structure of the proposed LDO regulator.

components, the PMOS pass transistor occupies the largest area, except for the load capacitor.

IV. CONCLUSION

This paper presents the design of the LDO regulator that achieves fast load transient response with the voltage damper and body bias feedback. The voltage damper circuit is included to respond to fast load transients, while the body bias feedback enables the LDO regulator to respond to relatively slow distortion of the output voltage. The proposed LDO regulator achieves an undershoot of 284mV and an overshoot of 199mV at V_{OUT} = 1.6V for a load step ranging from 0.2mA to 100mA with an edge time of 100ns.

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TABLE I. PERFORMANCE COMPARISON TABLE

	[12]	[13]	This Work
Tech (nm)	180	180	180
Area (mm^2)	0.044	0.055	0.026
Output Voltage (V)	1.2	1	1.6
Maximum Load (mA)	100	100	100
$C_{on\text{-}chip}/C_{load}$ (pF)	-	6.5/100	9.32/100

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