9-bit 500-MS/s Pipelined SAR ADC using Dynamic Amplifier with Background Calibration

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***Abstract* – This paper presents a 9-bit 4-stage pipelined successive-approximation-register (SAR) analog-to-digital converter (ADC) using a dynamic amplifier with a background inter-stage gain calibration technique, which resolves the capacitor digital-to-analog converter (CDAC) mismatch of the first stage and the gain errors caused by process, voltage, and temperature (PVT) variations. The increase of residue voltage caused by the two paired offset comparators used for calibration is reduced by the dither injection of the 1st-stage CDAC. The ADC is designed as 3b+3b+3b+3b for each stage and has 3-bit redundancy. The proposed ADC in this paper is fabricated in a 28 nm CMOS process, occupies an area of approximately 0.02 mm^2, and only consumes 11 mW of power. Furthermore, the SNDR of the ADC is 48.37 dB when measured at a sampling rate of 241.37 MHz, which is the Nyquist rate for this ADC.**

***Keywords*—Analog-to-digital converter (ADC), pipelined successive approximation resistor (SAR), background calibration.**

I. INTRODUCTION

Although the successive-approximation-register (SAR) analog-to-digital converter (ADC)s widely used as a low-power ADC structure, it has a limited conversion time and is extremely vulnerable to comparator offset and noise [1]. Given these limitations, pipelined SAR ADC structures have recently been widely employed as high-speed ADCs. The pipelined SAR ADC uses SAR ADCs in a multi-stage structure, enabling it to overcome the limitation of reduced operating speed caused by the limited conversion time [2]. However, when using the pipelined structure, high power consumption and the resolution of the residue amplifier become the main design challenges. Here, using a dynamic amplifier as a residue amplifier in the pipelined stage provides an important solution.

Unlike typical operational amplifiers, a dynamic amplifier does not use static current [3–4]. The structure and operation of a typical dynamic amplifier are displayed in Fig. 1 (a) and (b), respectively. The amplifier is driven by the tail clock pulse. First, the amplifier's output is reset to VDD, and when the tail device is turned on by the clock pulse, the output reduces and is generated the voltage difference. The total current of the amplifier is determined by T_p, which is the turn-on time for the tail device. Moreover, unlike operational amplifiers (which use a static current), dynamic amplifiers use a relatively small dynamic current. However, the gain of dynamic amplifiers is very sensitive to PVT variations. For example, the current in the amplifier flows differently depending on the temperature. As shown in Fig. 1 (b), less current flows in the tail device at low temperatures, whereas more current flows at higher temperatures, resulting in different voltage gains at different temperatures. If such an amplifier was used as a residue amplifier in a multi-stage pipelined SAR ADC, the performance of the ADC would change depending on PVT variations, which would be problematic. Since this design challenge means that the exact gain of a dynamic amplifier cannot be defined in real-world applications, using a calibration technique is essential.

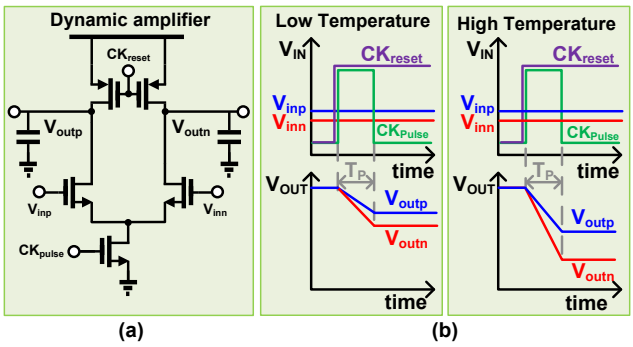

Fig. 1. (a) Structure and (b) operation of a dynamic amplifier.

This paper presents a pseudo random noise (PN) based background calibration method for calibrating the gain of a dynamic amplifier that is sensitive to PVT variations. This method enables multi-stage ADC operation using a dynamic amplifier by revealing the change in bit weight due to temperature variations [5]. Furthermore, this background calibration technique ensures that the signal to noise and distortion ratio (SNDR) does not fall below 2.89 dB at temperatures in the range of −10 to +50 °C. Ultimately, a 9-bit 500 MS/s prototype ADC is implemented in a 28 nm CMOS process.

II. DESIGN AND MEASUREMENT

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A. Proposed pipelined SAR ADC.

Figure 2 displays the structure of the proposed pipelined SAR ADC, which consists of four 3-bit stages, each of which has 1-bit redundancy. However, only the first stage uses background calibration. By including the bit-redundancy, the structure consists of nine bits in total. The residue amplifier connecting the internal stage is composed of the conventional dynamic amplifier displayed in Fig. 1 (a) with a gain of 4 at room temperature, which is the nominal gain of the pipelined ADC with 3bits at each stage and 1-bit redundancy. The total capacitance in the first stage is 200 fF considering KT/C noise and the back-end stage is scaled to 20 fF.

Each stage consists of a 3-bit SAR ADC, except that the first stage consists of a SAR ADC with an additional operation for background calibration. Although it is a 3-bit SAR ADC, it operates one last additional conversion for dither injection, for which the PN generator displayed in Fig. 2 is required. This PN generator consists of a PRBS generator that generates one bit of pseudo-random noise per sampling rate. Since each stage has one bit of redundancy, it is less sensitive to comparator offsets. Therefore, the second and third stages are designed as a loop-unrolled SAR structure, which is helpful for achieving high speed. The last stage uses an asynchronous SAR structure because there is no redundancy.

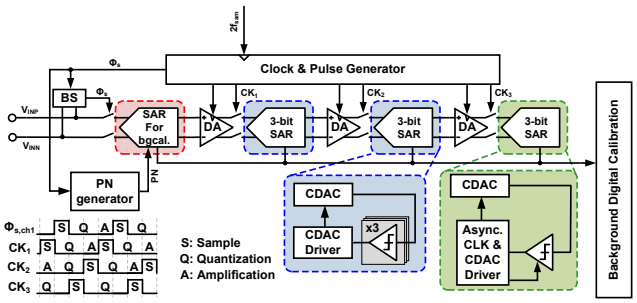

Fig. 2. Proposed pipelined SAR ADC structure.

B. First stage SAR structure for background calibration.

Figure 3 displays the SAR structure of the first stage. The operation of SAR uses a loop-unrolled SAR structure, and two opposite-paired polarity offset comparators are required for conversion. One of the two comparators is selected by the PN signal, and the last conversion is determined solely by PN. A 3-bit CDAC is used for a total of 3-bit SAR, and 0.5 C_u is added for the half least significant bit (LSB/2) dither injection.

If the offset is too large, the linearity of the dynamic amplifier will be limited and the SNDR of the overall ADC will be degraded. In contrast, if the offset is too small, the calibration will be poor. Accordingly, an appropriate offset comparator is required. Figure 4 (a) displays a schematic of the offset comparator. The basic structure is a double-tail comparator, and the offset is achieved by introducing a mismatch into the pre-amplifier's tail device. Four bits control the size of the tail device to create an appropriate offset, which ranges from 70 to +70 mV, as displayed in Fig. 4 (b).

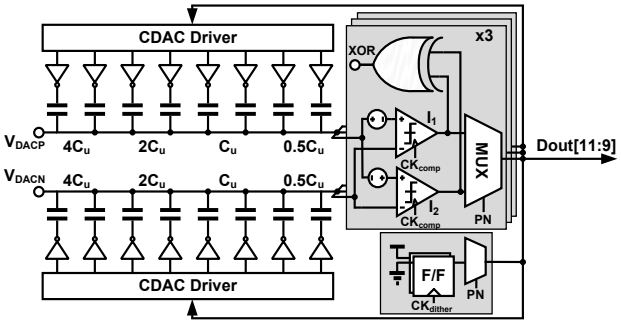

Fig. 3. First-stage SAR structure.

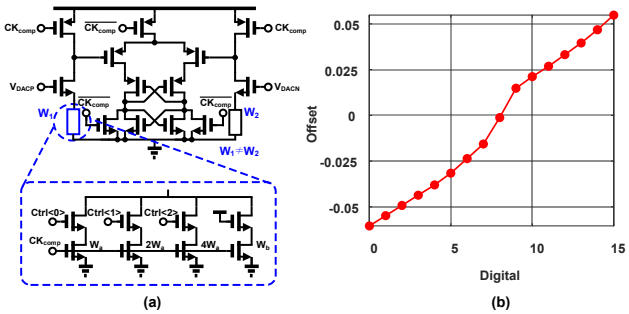

Fig. 4. (a) Schematic of the offset comparator and (b) plot of the control bits vs. offsets.

C. CDAC conversion process

CDAC conversion for background calibration differs from typical CDAC conversion, which is explained by the four steps displayed in Fig. 5. Comparator I_1 has $+V_{os}$ and I_2 has $-V_{os}$ in Fig. 3; hence, the two comparators create a window. This region is where the CDAC voltage (V_{DAC}) lies between the two offsets. As shown in Fig. 5(a), when V_{DAC} enters the window, the two comparators have different outputs, specifically $D_{out,I1} = -1$ and $D_{out,I2} = +1$. This moment can be found by using the XOR gate, as demonstrated in Fig. 3.

Before the VDAC enters the window, it performs a typical conversion operation. However, after V_{DAC} enters the window, conversion is determined by the PN. As demonstrated in Fig. 5 (b), an opposite conversion operation is performed when PN = 1 and PN = −1. When PN = 1, comparator I1 is selected, and when PN = −1, I2 is selected by mux and the opposite conversion progresses by PN, as displayed in Fig. 5(b). Since the output of the comparator is equal to −PN according to the expression in Steps 1 and 2,the ADC output (D_{out}) can also be expressed as −PN.

Figure 5(c) demonstrates that subsequent conversions can also be determined by PN. If Vos is less than half the LSB of CDAC, V_{DAC} cannot enter the window after the previous operation. This means that after Step 2, the opposite conversion progresses compared to Step 2, as explained in Equations (1)–(3).

$$-V_{os} < V_{DAC} < V_{os}, \quad (1)$$

$$LSB = \frac{C_u}{C_{tot}} V_{ref}, \quad (2)$$

$$-V_{os} + LSB < V_{DAC,step3} < V_{os} + LSB, \quad or \quad -V_{os} - LSB < V_{DAC,step3} < V_{os} - LSB. \quad (3)$$

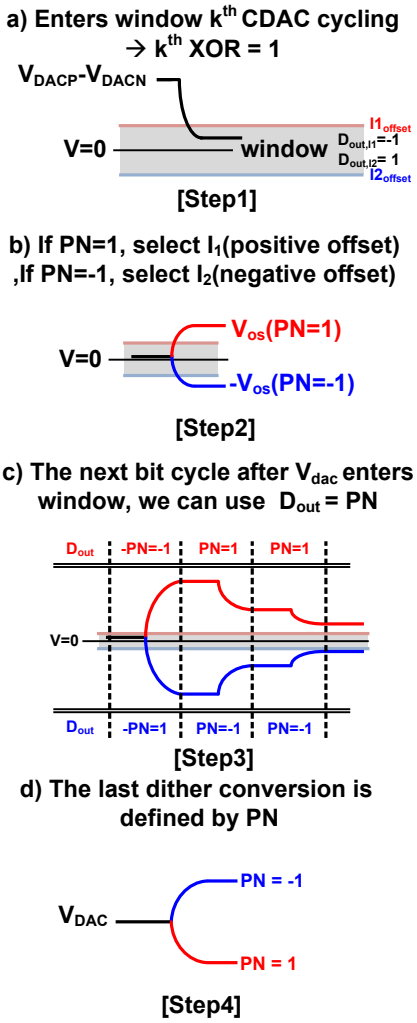

Fig. 5. Conversion process for background calibration.

The moment V_{DAC} enters the window can be expressed using Equation (1), and the LSB can be expressed using Equation (2), where C_u is the unit capacitance and C_{tot} is the total capacitance of CDAC. If V_{os} is less than half the LSB, V_{DAC} in Step 3 ($V_{DAC,step3}$) is either greater than LSB/2 or less than −LSB/2. This means that V_{DAC} does not lie in the window in Step 3. Ultimately, the conversion after Step 2 works in the opposite way to the conversion of Step 2, where D_{out} can be defined as being equal to PN. In other words, according to Steps 1–3, if the moment VDAC enters the window by XORing and the PN can be determined, D_{out} can also be determined.

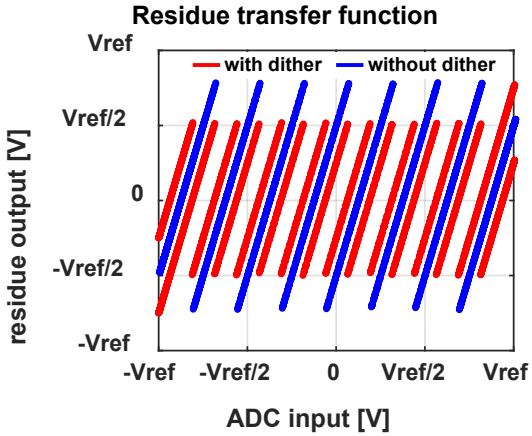

Fig. 6. Residue transfer function with and without dither.

Although this pipelined SAR ADC has one bit of redundancy, the offset comparator increases the output residue, which can create linearity problems for dynamic amplifiers. Injecting LSB/2 dither (similar to the offsets of I_1 and I_2) is necessary to reduce the residue by conversion. This conversion progresses in the direction of reducing residue in accordance with PN. As shown in Fig. 5(d), V_{DAC} increases when PN = −1 and decreases when PN = 1. As a result, as evidenced in Fig. 6, which displays the residue transfer function, the residue output is smaller with dither than without dither.

Table I describes the bit cycling of the conversion process with background calibration. After V_{DAC} enters the offset window, the conversion begins sequentially, similar to Table 1. If V_{DAC} enters the window at the j_{th} cycle, the outputs of I_1 and I_2 will differ and one of the comparators will be selected by PN. In this case, the digital output of the first stage can be defined as $D_{out}[12\text{-}j] = -PN$ and $D_{out}[11\text{-}j:9] = +PN$. After three finished conversions, V_{DAC} will increase or decrease by LSB/2 depending on PN in the dither cycle, as displayed in Table I2.

TABLE I. Bit cycling sequence for ADC conversion

	I_1	I_2	1) j^{th} Bit cycling	2) j^{th} Dither cycle
Case 1	+1	+1	$D_{out}[12\text{-}j]=+1$	If PN = 1 $V_{DAC}=V_{DAC}$-LSB/2 If PN = -1 $V_{DAC}=V_{DAC}$+LSB/2
Case 2	+1	-1	$D_{out}[12\text{-}j]=-PN$	
Case 3	-1	-1	$D_{out}[12\text{-}j]=-1$	

If VDAC enters the offset window at j^{th} cycle, we use $D_{out}[12\text{-}j]=-PN$, and $D_{out}[11\text{-}j:9]=PN$ for the remaining 1st stage bit cycles.

D. Background calibration algorithm

Figure 7 displays the background correction algorithm block diagram. After the conversion of all stages in the ADC is completed, the digital output of each stage can be obtained and the backend stage is used (which is from the 2nd to the 4th stage) as the digital output using the ideal weighted sum output. If the output of the backend stage for each sample is multiplied by PN and averaged using an accumulator, the

weights of the first stage and dither can be obtained, as demonstrated in Equations (4)–(7).

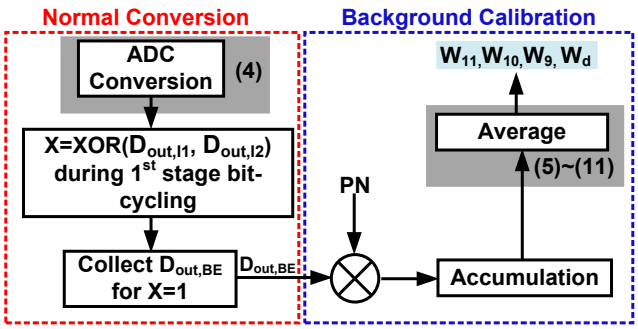

Fig. 7. Block diagram of calibration algorithm.

If V_{DAC} enters the window at the j[th] cycle, the sampled input value can be expressed as Equation (4), where $\boldsymbol{V_{res}}$ is the residue after converting the first stage, $\boldsymbol{A}$ is the gain of the dynamic amplifier, and $\boldsymbol{W}$ is the weight of the stage before calibration.

$$\boldsymbol{V_{in} = \frac{1}{A}V_{res} + \left(\sum_{i=1}^{j-1} D_{out}[12-i]\cdot W_{13-i}\right)} \\ \boldsymbol{-PN\cdot W_{12-j} + \left(\sum_{i=j+1}^{3} PN\cdot W_{12-i}\right) + PN\cdot W_d}, \tag{4}$$

where the difference between $\boldsymbol{V_{res}}$ and the weighted sum output of the backend stage is only the quantization error, which is small enough to be ignored. Hence, we can assume that the two values are equal. Equation (5) can be expressed by rearranging Equation (4) for $\boldsymbol{V_{res}}$, applying it to the weighted sum of the backend stages ($\boldsymbol{D_{out,BEdec}}$) and multiplying by PN. Here, since PN = +1 or −1, $PN^2 = 1$; hence, it can be arranged as in Equation (6).

$$\boldsymbol{D_{out,BEdec}\times PN =} \\ \boldsymbol{A\cdot PN\cdot\left\{V_{in} - \sum_{i=1}^{j-1} D_{out}[12-i]\cdot W_{12-i}\right\}} \\ \boldsymbol{+A\cdot\left(PN^2\cdot W_{12-j} - \sum_{i=j+1}^{3} PN^2\cdot W_{12-i}\right.} \\ \boldsymbol{\left. -PN^2\cdot W_d\right),} \tag{5}$$

$$\boldsymbol{D_{out,BEdec}\times PN =} \\ \boldsymbol{A\cdot PN\cdot\left\{V_{in} - \sum_{i=1}^{j-1} D_{out}[12-i]\cdot W_{12-i}\right\}} \\ \boldsymbol{+A\cdot\left(W_{12-j} - \sum_{i=j+1}^{3} W_{12-i} - W_d\right).} \tag{6}$$

Finally, Equation (6) can be simplified into Equation (7) by averaging. If the number of averaged samples $\boldsymbol{P}$ is sufficiently large, the first term of the right side in Equation (7) converges to zero, meaning that only the second term remains, as in Equation (8). This result is expressed only with $\boldsymbol{A}$ and $\boldsymbol{W}$, and if $\boldsymbol{A}$ changes, this expression also changes.

$$\boldsymbol{average\left(D_{out,BEdec}\times PN\right) =} \\ \boldsymbol{\frac{A\cdot\sum_{h=1}^{P}\left(X(h)\right)\cdot PN}{P}} \\ \boldsymbol{+A\cdot\left(W_{12-j} - \sum_{i=j+1}^{3} W_{12-i} - W_d\right),} \tag{7}$$

$$\boldsymbol{average\left(D_{out,BEdec}\cdot PN\right)} \\ \boldsymbol{\approx A\cdot\left(W_{12-j} - \cdots - W_d\right).} \tag{8}$$

Equation (8) provides us with a simple iterative method for finding all the bit weights. Specifically, we start by collecting $\boldsymbol{D_{out,BEdec}}$ for ADC inputs that do not enter the offset window, which corresponds to

$$\boldsymbol{average\left(D_{out,BEdec}\cdot PN\right) = -A\cdot W_d.} \tag{9}$$

To find $\boldsymbol{W_9}$, we use only $\boldsymbol{D_{out,BEdec}}$ for the samples that enter the window in the last cycle of the first stage conversion.

$$\boldsymbol{average\left(D_{out,BEdec}\cdot PN\right) = A\cdot W_9 - A\cdot W_d.} \tag{10}$$

This process continues until we find $\boldsymbol{W_{11}}$, which is the case when the first cycle of the first stage conversion is within the offset windows, i.e.

$$\boldsymbol{average\left(D_{out,BEdec}\cdot PN\right)} \\ \boldsymbol{= A\cdot W_{11} - A\cdot W_{10} - A\cdot W_{10} - A\cdot W_d.} \tag{11}$$

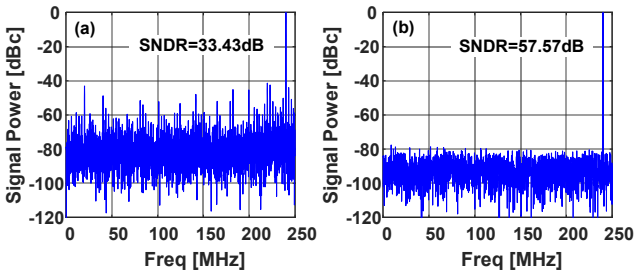

Fig. 8. MATLAB model of ideal 9-bit pipelined SAR ADC FFT plot (a) before and (b) after calibration.

At the end of the iteration, the bit weight reflecting the changed gain can be obtained by sequentially adding or subtracting each average value. As a result, even if the gain of the dynamic amplifier changes due to PVT variations, we can update the bit weight by finding the gain of the amplifier using this method. Figure 8 displays the results of a MATLAB model simulation of a pipelined SAR ADC with a gain error of 20%. Here, SNDR increased from 33.43 to 57.57 dB using this calibration method.

The number of samples used for background calibration is about 100,000, and the more samples that are used, the higher the calibration accuracy, as demonstrated in Equations (7) and (8). Figure 9 displays the weight that changes depending on the number of samples, which converges for more than approximately 50,000 samples.

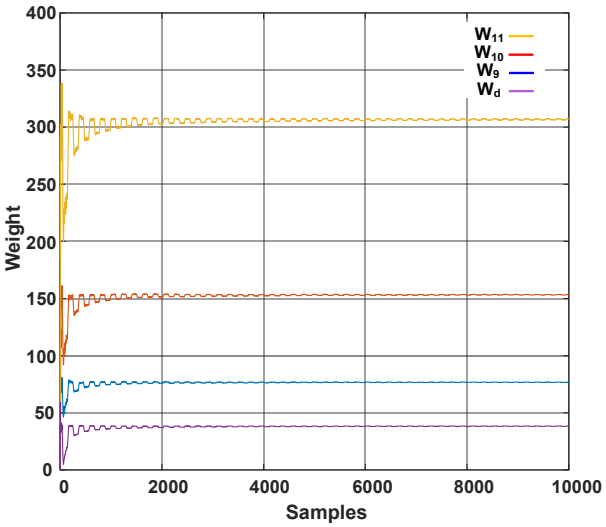

Fig. 9. The convergence of the first stage bit weight.

E. Pipelined SAR ADC measurement

Figure 10 displays the layout of a prototype ADC fabricated using a 28 nm CMOS process. The complete ADC, including the core ADC and reference buffer, occupies an area of 0.08 mm^2.

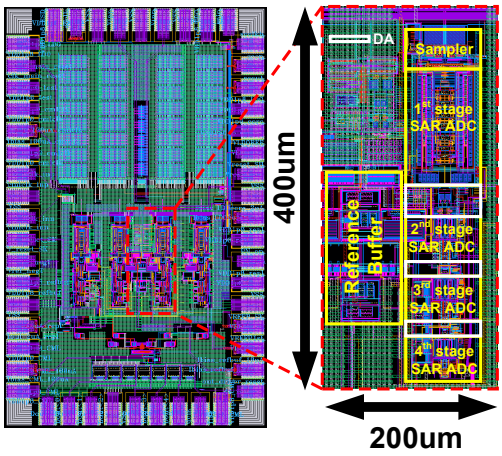

Fig. 10. Layout of a prototype ADC

The total power consumption of the measured ADC when running at 500 MHz sampling frequency was 3.55 mW, of which the first stage consumed 1.88 mW and the backend stage consumed 0.53 mW. Furthermore, the dynamic amplifier only consumed <28 μW of power, which was <1% of the total power. The power consumption of the dynamic amplifier was calculated by determining the ratio of measured power based on simulation results. Figure 11 displays the output spectrum measured at the Nyquist input frequency, where the output is after the decimation of 185.

Figure 12 charts the measured SNDR vs. temperature. The temperature was swept from −10 to +50 ℃ and compared two cases. In both cases the calibration performed at 30 ℃ and compared the results when the temperature was changed with the calibration turned on and off. When the calibration is off, the maximum SNDR drop was approximately 11.95 dB at − 10 ℃, whereas after using the background calibration algorithm, the maximum SNDR variation was only 2.89 dB. Figure 13 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL), which are -0.78/0.56 LSB and -1.49/1.75 LSB, respectively. Figure 13 shows the variation of SNDR as the input frequency is changed. The results are measured by increasing the input signal from 8MHz up to the Nyquist frequency. The results reveal a maximum 48.8dB and a minimum 48.13dB of SNDR.

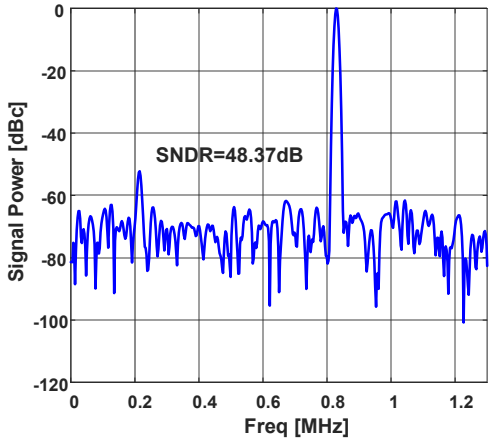

Fig. 11. Measured output spectrum of ADC

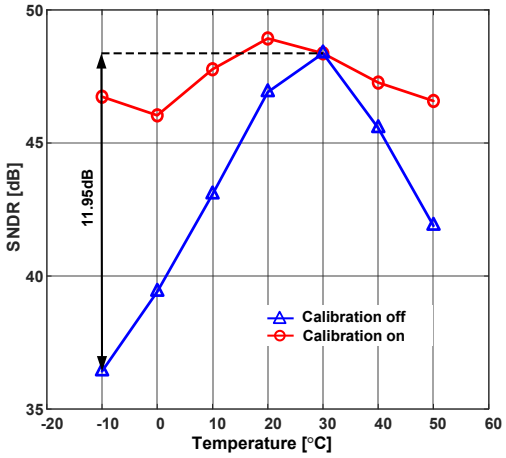

Fig. 12. Measured SNDR vs. temperature.

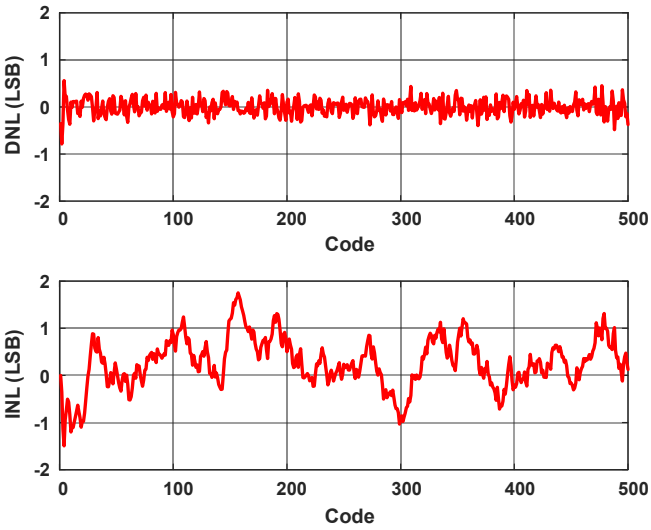

Fig. 13. INL and DNL of the ADC

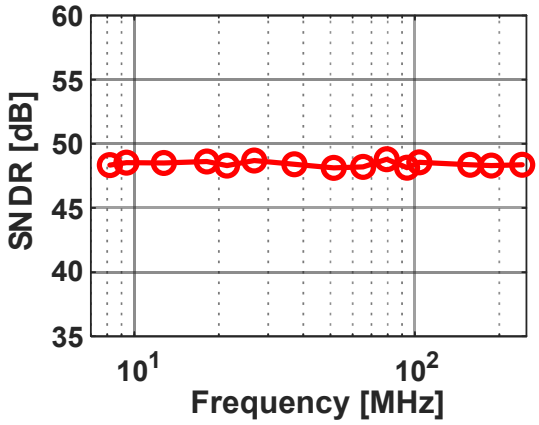

Fig. 14. Measurement of SNDR versus signal frequency

TABLE II. performance summary

	This work	[6]	[7]
Architecture	Pipelined SAR	Pipelined SAR	Pipelined SAR
Process (nm)	28	28	65
Fs (GS/s)	0.5	0.1	0.5
Power (mW)	3.55	11.5	6
SNDR (dB)	48.37	62.1	50.5
FoMw (fJ/conv-step)	33.15	13.1	44
Area(mm^2)	0.08	0.05	0.07

III. CONCLUSION

This paper presented a 9-bit 500MS/s four-stage pipelined SAR ADC utilizing a background inter-stage gain calibration technique. At a 500 MHz sampling frequency, the highest SNDR was 48.37dB and FoMw was fJ/conv-step. Moreover, the ADC operated with only 2.89 dB SNDR degradation from −10 to +50 ℃. Using the proposed background calibration method, it will be possible to design a multi-stage pipelined SAR ADC using a dynamic amplifier with a wide operating temperature range. Furthermore, an increase in SNDR of up to about 12 dB can be achieved by using this method compared to before calibration.

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