A Low-Ripple Charge Pump based on a Parallelized Ring Oscillator with Latches

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Abstract **- The PMICs (Power Management Integrated Circuits) are often required with strict conditions such as highly limited area and power loss as the IoT (Internet of Things) has been developed. Switched- capacitor DC-DC converter is one of the best candidates to meet these demands with its size and efficiency. In this paper, we designed a high efficiency switched-capacitor based charge pump for integrated circuits. The low-ripple is also achieved with smallest output capacitor among the compared works. This charge pump is fabricated with 0.18µm CMOS process and it consumes the active area of 0.068mm^2. The 82.2% peak efficiency(η_{max}) and 0.15% Output Voltage Ripple (OVR) is achieved in 1V supply.**

Keywords**—Charge pump, Low-ripple, Low-ripple, Multi-phase, Small size**

I. INTRODUCTION

Power management integrated circuits (PMICs) help to achieve high power efficiency by adjusting the power delivered to each block in System on Chips (SoCs). PMICs can adjust the power by controlling the voltage and current. By using PMICs in SoCs, we can reduce the number of power sources and make various voltage level with one power source. As Internet of Things (IoT) emerges, the importance of PMIC is increasing with their integrity and efficiency. The inductive DC-DC converter cannot meet these demands due to the necessary of large inductor. LDO; one of the options of making small area integration power module is also not desirable because of its inevitable power leaking structure. Therefore, many researchers pursue the switched-capacitor DC-DC converter (SC DC-DC Converter) also known as charge-pump (CP) for the compact battery powered area IoT systems. Also, the low ripple is needed because the circuits in the IoT systems usually has strict demand of supply ripple, such as PLL and analog sensor interface. The large ripple performance forced the system to use additional LDOs which degenerate the power and area performance.

Therefore, low output voltage ripple (OVR) and highly efficient SC DC-DC converter are proposed in this paper. To make output ripple smaller than existing SC DC-DC converters, latches are arranged between the two self-oscillating voltage doubler structures. Also, high efficiency is achieved by removing unnecessary circuits. Thanks to achieving smaller output ripple, noiseless DC-DC converter makes additional LDO unnecessary. First, conventional DC-DC converters are presented, and the reason why self-oscillating voltage doubler is selected among them is elaborated in this paper. In Section III, the proposed system is explained with detailed circuit-level diagrams. The simulation and measurement results are introduced with the chip layout and performance comparisons with existing works.

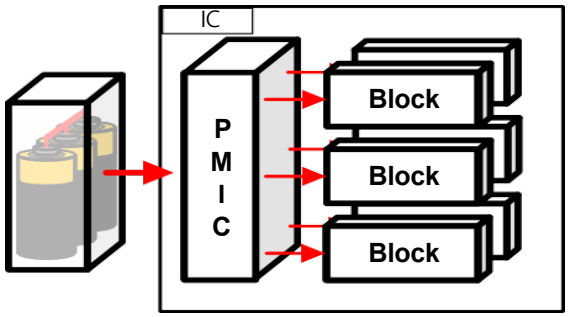

Fig. 1. The usage of power management unit in the IoT based integrated circuit system.

II. CONVENTIONAL SC DC-DC CONVERTERS

The most basic on-chip capacitive voltage multiplier was proposed in 1976 by J. F. Dickson [1], shown in Fig. 2.

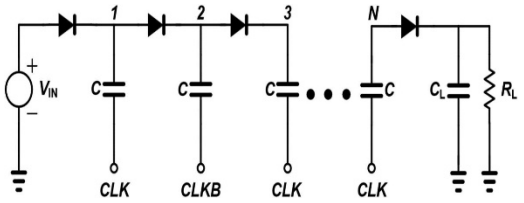

Fig. 2. Dickson Charge pump

The unit cell of the Dickson charge pump consists of one switch implemented by diode-connected transistors in the CMOS process and flying capacitor. The clock signal directly goes into the bottom plate of the capacitor to pump up the voltage. This direct voltage pumping makes bottom plate parasitic capacitance zero. The gain of the charge pump is ideally N + 1 when the high voltage of the clock is the same as the input voltage and N is the number of the unit cell.

$$V_{N+1} = V_N + V_{CLK} \quad (1)$$

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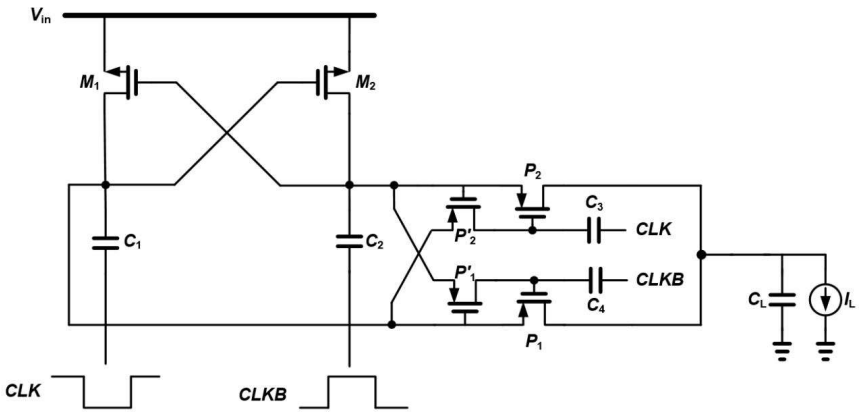


Fig. 3. Cross-coupled charge pump

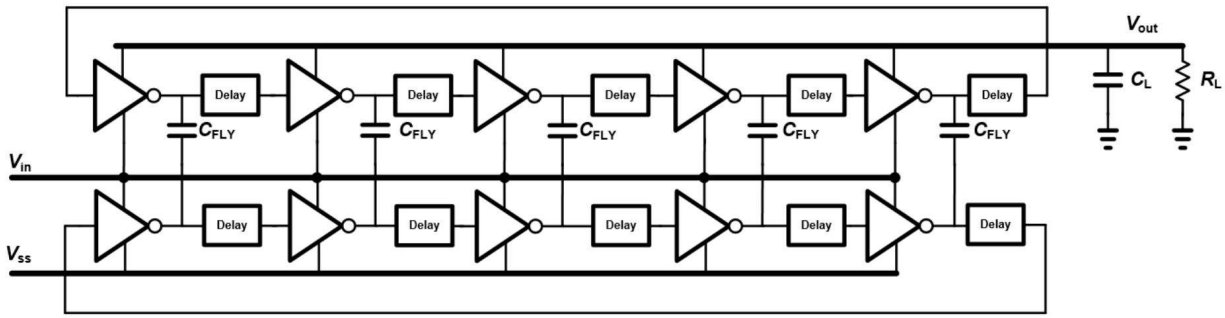


Fig. 4. Basic structure of self-oscillating voltage doubler

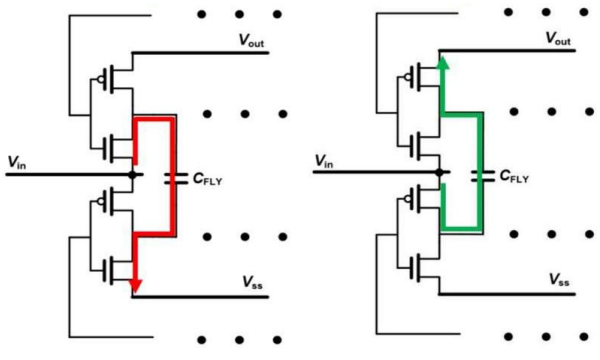
This first came out voltage multiplier has few limitations. MOSFETs are 4 port devices. The port we usually ignore is called body which has to be shared in case of the NMOS in the CMOS process. When we ignore the body, we regard that it has the same voltage as the source. But in the case of the Dickson Charge Pump, the body is connected with ground voltage while the source is $N + 1$ voltage which is the condition we cannot ignore the body effect. Body effect makes the threshold voltage higher so that the turn-on voltage is getting higher as the more the unit cell exists. The voltage drop due to body effect and the forward bias voltage of the diode makes voltage conversion efficiency (VCE) worse. Not only the voltage drops, but a high difference between the ports can also affect on durability. Researchers find the solutions that use other transistors for adjusting body voltages [2] or boost the gate voltages by utilizing charge transfer switches [3]. These problems can be easily solved these days thanks to the deep n-well process in the CMOS process which can divide the body port of the n-well.

In 1998, P. Favrat [4] claimed a cross-coupled voltage doubler which is also called Favrat cell (Fig. 3). NMOS switch is triggered by the pumping signal of the opposite side. This cross-coupled structure makes an automatic dual-phase system. Unlikely the variation of the Dickson voltage multiplier, the importance of having non-overlapping clocks is smaller because of its cross-coupled structure.

The unit cell of the voltage doubler consists of two capacitors and clock voltage on the bottom plate that have 180 ◦ phase differences from each other. PMOS switch is selecting the higher voltage among two capacitor's top plate nodes which will be pumped. According to the name voltage doubler, V_{OUT} will be $2 \cdot V_{IN}$ when VCLK has same amplitude as V_{IN}.

One of the weak points of the switched-capacitor based charge pump is that it needs clock signals. The clock signal is used to make the switch works in proper timing and pump the charge from the capacitors. Every switched capacitor DC- DC converters need clock signal to switching the path and pumping the voltages which means they need external clock signals or additional clock generation blocks. W.Jung [5] claim this aspect as introducing redundant area and power consumption with proposing self-oscillating voltage doubler (Fig. 4).

What they suggested was the fully integrated energy harvester based on a self-oscillating voltage doubler. The system consists of the self-oscillating doubler with delay blocks for the frequency control and the feedback blocks to meet the certain power efficiency by making the certain level of output voltage level reasoning with mathematical derivations.



(a) (b)

Fig. 5. (a) Charging phase of self-oscillating voltage doubler, (b) Discharging phase of self-oscillating voltage doubler

In Fig. 5, the operating principles of self-oscillating voltage doubler are depicted. When the clock produced by the ring locator is high, charge the flow capacitor as much as the input voltage as the NMOS above and below turns on. Then, when the clock goes low in the phase, each PMOS is switched on, so that the output voltage doubles as the input voltage charged in the flying capacitor.

III. PROPOSED SYSTEM ARCHITECTURE

Self-oscillating structure has inevitable problem. Stacked ring oscillator structure, odd number of inverters make the output voltage ripple large. The operation of the parallelized self-oscillating voltage doubler can be divided into two phases. At the phase 1, if the ring oscillator consists with 3 inverters, two capacitors are pumping the charge and one is storing simultaneously. While, at the phase 2, one capacitor is pumping and two are storing. This asymmetric charge pumping against phase occurs voltage ripple on the output node. The first possible solution to solve the ripple is make the oscillator differential so that the number of inverters can be even. However, the differential structure is complicated and not accurate compare to a single-ended one.

Besides, the differential structure has many switches which lead to making undesirable parasitic effects and makes maximum power efficiency worse according to the other possibility is makes two ring oscillators in an anti-phase. As you can see in Fig. 6, the amount of the charge is equal against time. The substantial advantage of this scheme is that it increases stage numbers while reducing the number of switches which causes switching losses. Therefore, we suggest dual single-ended stacked ring oscillators which are synchronized in anti-phase.

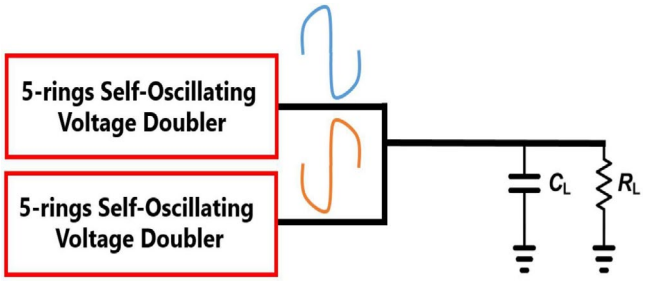


Fig. 6. Self-oscillating voltage doubler with phase difference

Consider the self-oscillating structure as stacked ring oscillator instead of the charge pump [6], the driving power of the lower ring oscillator is bigger than upper ring oscillator. So the phase inverter is connected to make lower ring oscillator will drive the opposite upper ring oscillator in anti-phase (Fig. 7). The phase inverter oscillates with V_{IN} supply. Because upper ring works between V_{IN} and 2 V_{IN}, DC-block capacitor is added after the phase inverter. For operating inverters, the current flows from V_{IN} which makes power efficiency low. However, we expect that this DC-block capacitor also acts as effective flying capacitor so that this power consumption in phase inverter is not the power leakage but power usage for pumping the charge to V_{OUT}.

Because of anti-phasing operation of voltage doubler, charging and discharging phase occur simultaneously, not alternately. So, it makes switching frequency twice as faster than before. The simulation results for comparing voltage output ripple with and without anti-phasing technique is shown in Fig. 9. We checked the output voltage ripple of decreases more than 60% due to anti-phasing technique under output 18pF capacitor.

Fig. 8 shows the full system architecture of proposed parallelized self-oscillating voltage doubler. It consists with the two self-oscillating voltage doubler which has 180° phase difference each other. The self-oscillating voltage doubler has stacked 5-stage ring oscillator with voltage-controlled delay cell. The controlling voltage (V_{CTRL}) is provided externally.

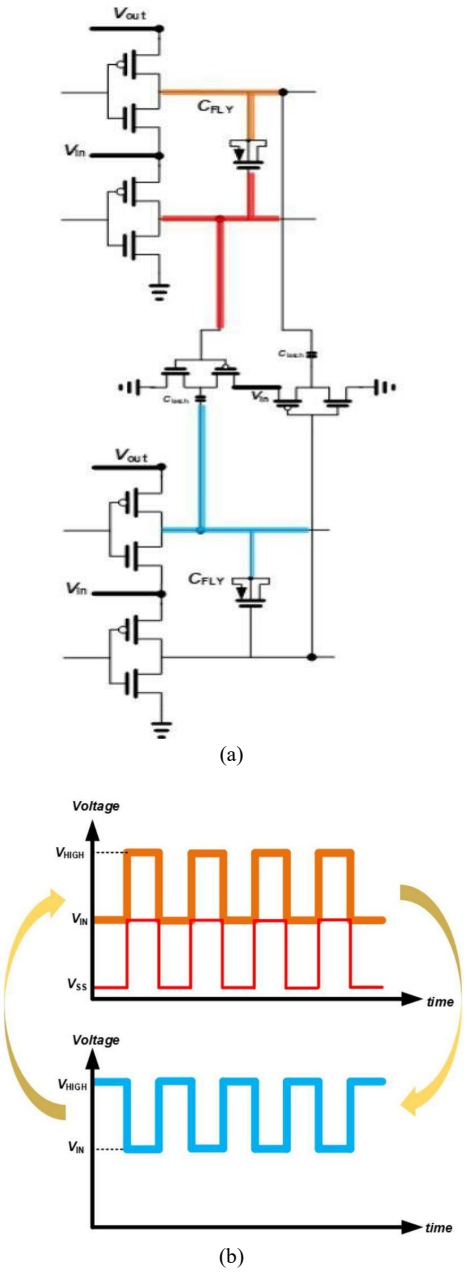


Fig. 7. (a) The detailed circuit diagram of anti-phasing latch and (b) the timing diagram of the system related to the anti-phasing mechanism

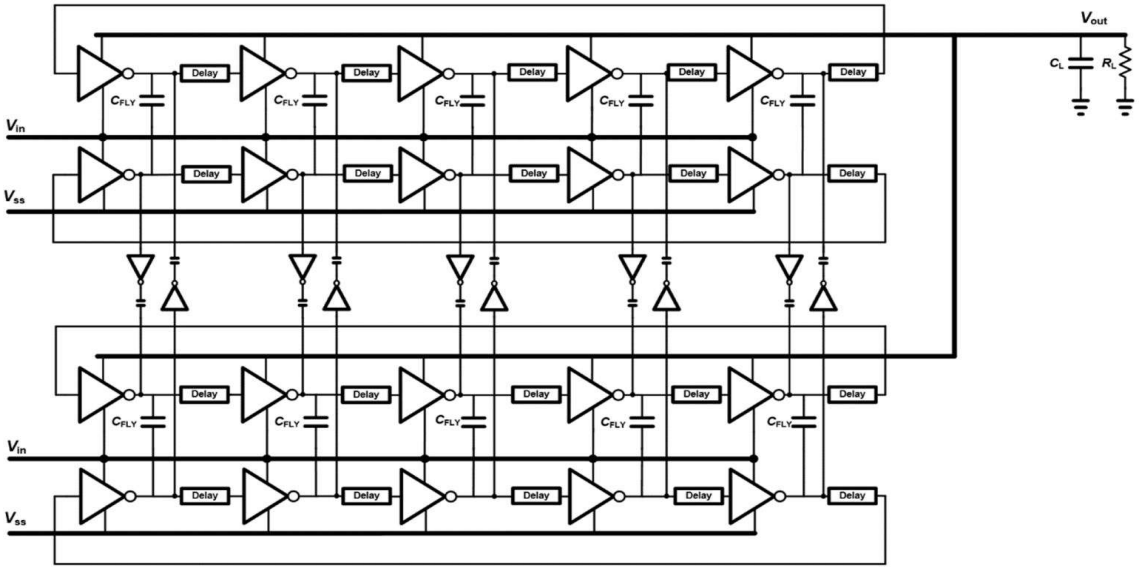
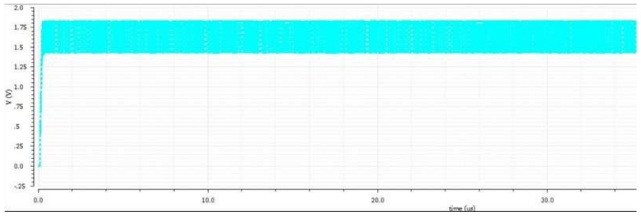
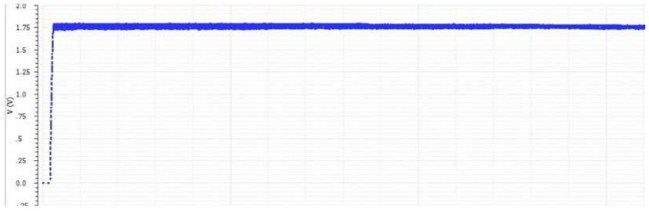


Fig. 8. Full system architecture of proposed parallelized self-oscillating voltage doubler



(a)



(b)

Fig. 9. The simulation result of the output voltage ripple; (a) without anti-phasing technique, (b) with anti-phasing technique

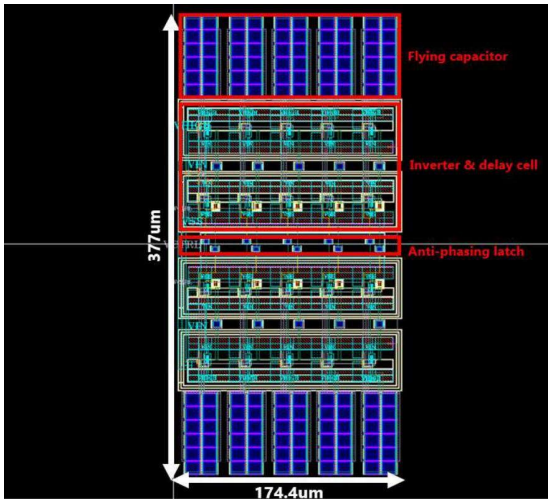


Fig. 10. The chip layout photo of the proposed parallelized self-oscillating voltage doubler

IV. SIMULATION AND MEASUREMENT RESULTS

Fabricated in a 0.18μm CMOS process, the proposed parallelized self-oscillating voltage doubler consumes the active area 0.0068mm2 - the smallest among the compared works (Fig.10). The flying capacitor and output capacitor are implemented with MOS capacitor to reduce the area consumption. The equivalent total flying capacitance is 109pF and the output on-chip 97pF capacitor is implemented for stabilizing the output voltage.

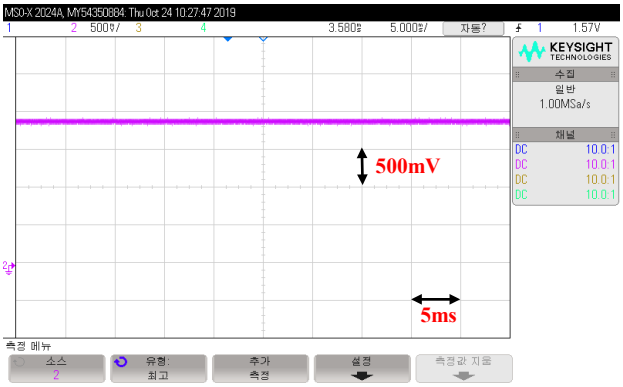


Fig. 11. The measured V_{OUT} with the transient response of the proposed system

The transient response shows that the output voltage (V_{OUT}) is locking at approximately 2V at V_{IN}=1V (Fig. 11) with the frequency of 13MHz with the frequency control voltage (V_{CTRL}) 0.7V. The proposed parallelized self-oscillating voltage doubler achieves the peak efficiency(η_{max}) of 82.2% and >72% for load resistance range of 4.5kΩ to 25kΩ (Fig. 12).

Table I shows the performance summary of proposed voltage doubler and compares it with previous studies. Proposed voltage doubler achieves area-efficient and quite high power-efficient 1:2 charge pump. Also, because anti-phasing self-

TABLE I. Comparison table

	JSSC 2010 [7]	VLSI 2010 [7]	VLSI 2009 [8]	JSSC 2014 [5]	This work
Architecture	Multi-phase	1:2 step up/down converter	Multi-phase	Self-oscillating	Parallelized self-oscillating
Conversion ratio	1:2	2:1, 1:2	1:2	1:2	1:2
Input voltage	1V-1.2V	1V	1V-1.2V	1.2V	1V
Frequency	250MHz-2GHz	100MHz	N/A	70Hz-19MHz	13MHz-31MHz
Peak efficiency	64%	90%	82%	75%	82%
Load range	0.4mA-9mA w/>40% eff.	0.5mA-5mA w/>80% eff.	0.15mA-2.2mA w/>80% eff.	1nA-0.35mA w/70% eff.	0.1mA-0.48mA w/>72% eff.
Output voltage ripple	N/A	N/A	0.5%	N/A	0.15%(min.)
Area	0.0067mm^2	0.0012mm^2	2.25mm^2	0.069mm^2	0.068mm^2

oscillating structure works for lowering ripple, the smallest output voltage ripple is 0.15% of output voltage level.

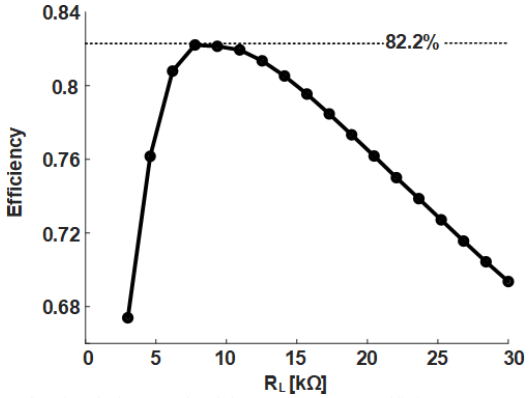


Fig. 12. The simulation result of the system power efficiency across various load conditions.

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REFERENCES

[1] J. F. Dickson, "On-chip high-voltage generation in mnos integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, June 1976.

[2] Jongshin Shin, In-Young Chung, Young June Park, and Hong Shick Min, "A new charge pump without degradation in threshold voltage due to body effect [memory applications]," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1227–1230, Aug 2000.

[3] Jieh-Tsorng Wu and Kuen-Long Chang, "Mos charge pumps for low- voltage operation," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 4, pp. 592–597, April 1998.

[4] P. Favrat, P. Deval, and M. J. Declercq, "A high-efficiency cmos voltage doubler," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 410– 416, March 1998.

[5] W. Jung, S. Oh, S. Bang, Y. Lee, Z. Foo, G. Kim, Y. Zhang, D. Sylvester, and D. Blaauw, "An ultra-low power fully integrated energy harvester based on self-oscillating switched-capacitor voltage doubler," *IEEE Jour- nal of Solid-State Circuits*, vol. 49, no. 12, pp. 2800–2811, Dec 2014.

[6] H. Lee, E. Jang, H. Saif, Y. Lee, M. Kim, M. B. Khan, and Y. Lee, "A sub- nw fully integrated switched-capacitor energy harvester for implantable applications," in *ESSCIRC 2018 - IEEE 44th European Solid-State Circuits Conference (ESSCIRC)*, 2018, pp. 50–53.

[7] D. Somasekhar, B. Srinivasan, G. Pandya, F. Hamzaoglu, M. Khellah,T. Karnik, and K. Zhang, "Multi-phase 1 ghz voltage doubler charge pump in 32 nm logic process," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 751–758, April 2010.

[8] T. V. Breussegem and M. Steyaert, "A 82fully integrated capacitive voltage doubler," in *2009 Symposium on VLSI Circuits*, June 2009, pp. 198–199.

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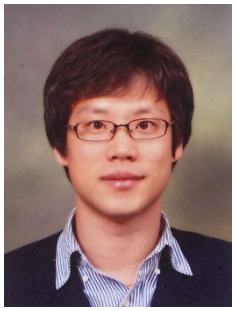

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