A 5.8 GHz DSRC Wake-Up Receiver with an Intelligent Digital Controller

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***Abstract* - In this paper, we introduce a high reliability radio frequency wake-up receiver (WuRx) for electronic toll (TEC) applications. As a final stage, an intelligent digital controller (IDC) is proposed to improve the reliability of WuRx and replace complex analog blocks. IDC achieves high reliability and accuracy by detecting and ensuring the configurable and consecutive number of wake-up signal cycles before activating power-hungry RF transceiver. Presented self-hibernation technique reduces current consumption from IDC and range communication (RC) oscillators during the non-wake-up time. To consider frequency variation of the wake-up signal and increasing WuRx accuracy, a digital hysteresis is included. A watch-dog timer is integrated for IDC self-recovery, to avoid uncertainties due to poor and false wake-up. During wake-up, the digital controller uses 34.62 nW and consumes 38.47 nA at 0.9 V supply. In self-hibernation mode, the current is reduced to 9.7 nA. It can be fully synthesized with 809 gates, and implementation at a 180 nm CMOS process in 94 x 82 µm^2 area. The measured energy consumption at WuRx is 2.48 µW, and the sensitivity is -46 dBm, the chip area is 0.484 mm^2.**

***Keywords*—5.8GHz, DSRC, IDC, Low Power, OOK, WuRx**

I. INTRODUCTION

Recently, RF has become an attractive research field for battery-driven transistors in various applications such as electronic payment collection system (ETC), wireless sensor network (WSN), wireless LAN (WBAN), IoT, and wearable devices. Currently, ETC (EtcSystem) is rapidly being introduced into automobiles as an intelligent transportation solution. DSRC is used at a speed of 5.8 GHz for high-speed wireless connection between road equipment (RSE) and onboard equipment (OBU) installed inside the vehicle. This saves time and eliminates congestion by automatically paying tolls without stopping the vehicle. In addition to the basic RF transceiver shown in Fig. 1, the Awakening Receiver (WuRx) in EUROSEAN is an auxiliary RF receiver and is required for battery shoes. WuRx is a pure asynchronous communication system that maximizes sleep time of a data transmitter. This not only reduces the power consumption of OBUs, but also reduces network latency. Fig. 2 shows the asynchronous connection between RSE and OBU and WuRx. Due to reliability, false assembly, power loss, low power consumption and good sensitivity, incorrect assembly and power supply of the main transmitter and receiver modules, battery life is shortened and overall WuRx performance is degraded. Many WuRx circuits have been studied in the literature to optimize power consumption, maximize sensitivity, and increase reliability [1]-[4].

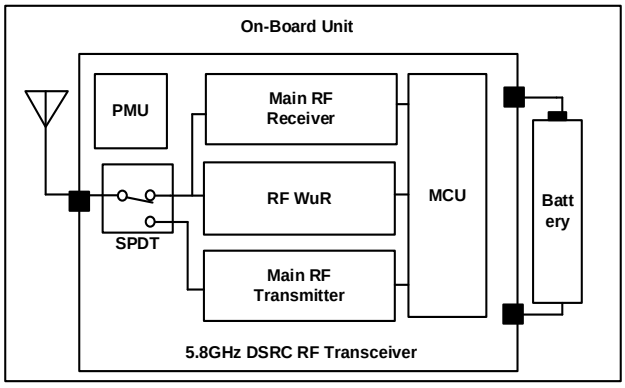

Fig. 1. The DSRC OBU system level block diagram

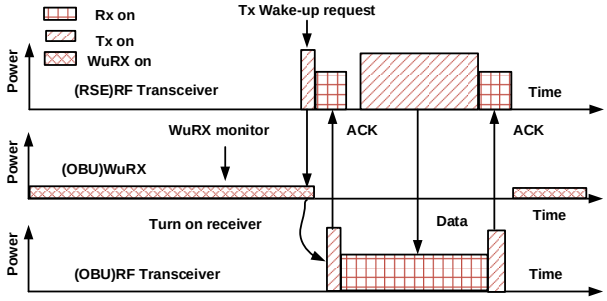

Fig. 2. the RF wake-up receiver (WuRx) pure asynchronous communication with OBU and the road side equipment (RSE)

The WuRx architectures are summarized as shown in Fig. 3. The WuRx is classified into active and passive wake-up circuits based on the power type. The active WuRx circuit monitors the normal wake-up signal by receiving power from the battery fitted to the OBU. The wake-up circuit uses the power collected from the incident RF signal from the passive receiver. In most cases, the active circuit uses the RF envelope detector (RFED) structure [5], [6], [7] shown in Fig. 3(a), (b), or the frequency conversion architectures [8],

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[9] shown in Fig. 3(c). For down conversion prior to envelope detection at intermediate frequency (IF) and amplification, by using RF amplification prior to local oscillator (LO) generation, or RF envelope detection [10], the frequency conversion-based wake-up receivers can offer higher sensitivity [11]. Because of power-hungry of phase-locked loops (PLLs) and for two-channel receptions [12] automatic channel scanning circuits, these circuits occupy a larger area and dissipate more power. Most wake-up circuits are implemented as RFED due to low power consumption using either Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) at weak inversion region or Schottky diodes [12], [13].

The WuRx structure in Fig. 3(a) uses a programmable gain amplifier (PGA) before an analog to digital converter (ADC) to occupy more area and increase power consumption. The WuRx shown in Fig. 3(b) uses Analog Bandwidth Filter (BPF) on the output interface that requires more chip space. An envelope detector [14],[15] based on a WuRx structure with a front amplifier and a bulk acoustic wave (BAV) input network is depicted in Fig. 3(c). ADC is in [16] also incorporated the WuRx at the output; However, to increase sensitivity and reduce the noise of the receiver, we use double sampling techniques by incorporating a low noise amplifier (LNA) before the envelope detector. The WuRx increases power consumption and increases chip area, but provides better sensitivity. The passive WuRx structure [17] incorporates an RF-DC (Radio Frequency to Direct Current) converter to collect energy from the incident RF signal, as shown in Fig. 3(d). To this end, we use RF-DC converters [18],[19] to efficiently convert RF carriers to DCs while generating an envelope of on-off keying (OOK) wake-up message signals. Voltage for power comparators and other WuRx circuits. This architecture is power efficient but less sensitive. It is also vulnerable to the absence of false and poor wake-up filtering.

The wake-up signal is classified into individual wake-up tones in the bit sequence [20]. Bit-sequence signals, also known as ID-based wakeups, are widely used to handle certain receiver sensor nodes in unicast in WSN and WWAN. The show has one wake-up call. The DSRC wake-up signals are 14 kHz single tone signals with a carrier frequency of 5.8 GHz [2] at 15–17 cycles.

Accurate sensitivity control is essential to the ETCS wake-up switch [5]. It was also not intended to reduce sensitivity or keep it very high. If the WuRx sensitivity is lower than the minimum, there is not enough available communication time. Although the WuRx is very sensitive, it turns on the OBU and initiates communication, even if the vehicle is far from the RSE and tollgate. In addition, very high sensitivity leads to communication failures, which interfere with other OBU devices on the road. Therefore, the WuRx sensitivity must be within a range not sensitive to process, voltage, and temperature changes [4].

The main function of the WuRx is to detect and verify that the received RF signal has a wakeup request and to determine whether the OBU turns on the low power transceiver. In most previous studies, the WuRx circuit identifies only insufficient signal amplitudes in the ETC system. If the WuRx line detects an invalid wake-up signal and an invalid wake-up signal and is not filtered, these signals will turn on the main RF transceiver module and reduce battery power. In the past, lots of WuRx architectures have been investigated to improve sensitivity and current, but the problem of false awakening and insufficient awareness remains unresolved. This article introduces the RFED-based trusted WuRx. To ensure the reliability and accuracy of WuRx, we propose an Intelligent Digital Controller (IDC). WuRx detects and rejects unwanted wake-up, invalid wake-up, and bad wake-up signals. It also reduces current consumption and area by replacing complex blocks such as ADCs or BPFs with amplifiers and compressors [1]-[3], [21]. Fully digitally synthesized, it offers a wide range of dynamic wake-up and vibration frequency ranges [22] without noise and PVT changes and is tuned for technological expansion.

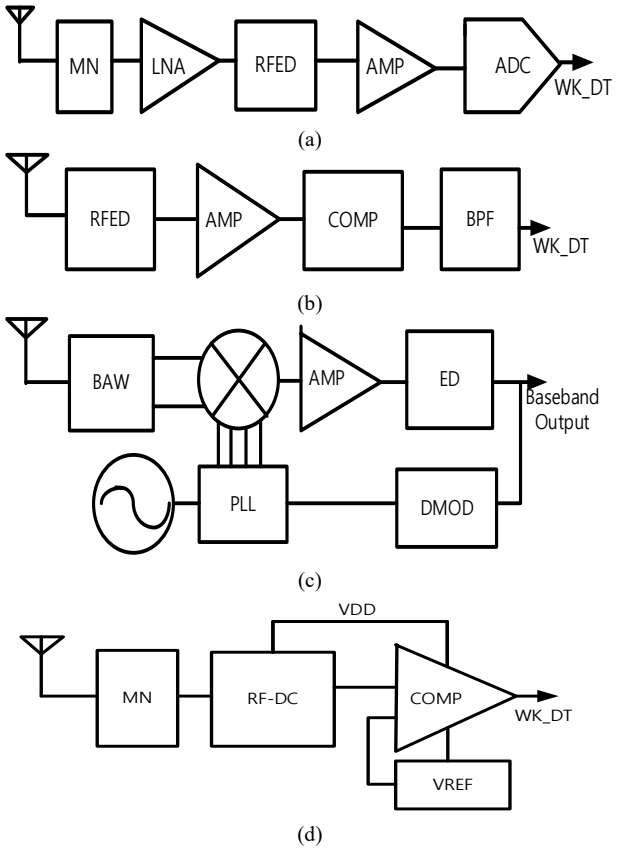


Fig. 3. The previous architecture of wake-up receiver: (a) RF envelope detector (RFED) with analog to digital converter (ADC) architecture; (b) RFED with band pass filter (BPF) architecture; (c) frequency conversion with LO architecture; (d) passive circuit with RF-DC architecture.

II. BUILDING BLOCKS

A. Proposed Wake-Up Receiver Architecture

The 5.8GHz RF WuRx to ensure reliability and accuracy by using integrated IDC is shown in Fig. 4. The antenna catches the incoming RF signal and transmits it to the pi-matching chip outside the chip. The corresponding network is a passive circuit that is essential to transmit the maximum power of the RF signal to the receiving circuit. The pi-matching network supports an antenna impedance equivalent to the proposed WuRx input impedance to enable

maximum transmission of antenna power to the WuRx circuit. Unlike [1,21], the internal chip matching network, pi-matching network outside the chip catches a RF wake-up signal, increases the voltage and increases the sensitivity or |S11|. The high-gain RF envelope detector restores the wake-up baseband signal, improves the signal-to-noise ratio (SNR) without consuming additional current. RFED is an important circuit connected to the WuRX with antenna, generating a 14 kHz baseband wake-up signal and decreasing the amplitude of modulated RF 5.8 GHz.

Because of the various programmable parameters of IDC, programmable Gain Amplifier (PGA) Comparator (COMP), Base Band Analog (BBA) and RFED was controlled by the main control unit (MCU), makes the WuRx circuit flexible. The role can be external controllable registers, an external microcontroller, or an on/off chip modem. The comparator (COMP) makes digital output signal for IDC processing. A configurable clock for the IDC block is generated by an ultra-low power communication oscillator (RC) with a dynamic tuning range. By identifying and filtering non-wake up signals, digital controller is provided to ensure the reliability and accuracy of the WuRx. It consumes very low power, requires a very small chip area and a fully synthesizable block. Large area interface blocks that has complex power consuming such as ADCs and BPFs can be replaced by the digital controller.

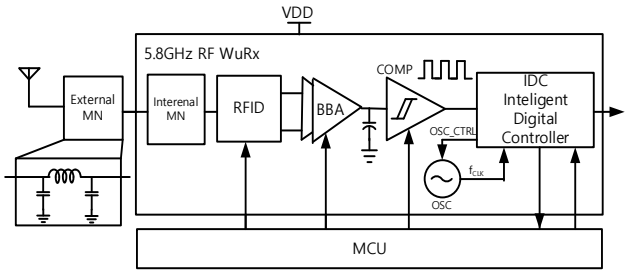


Fig. 4. Proposed RF wake-up receiver architecture

B. Configurable, Multi-Mode Intelligent Digital Controller

As much as high sensitivity and low power consumption in the DSRC WuRx design, the identification of incorrect wake-up signals is critical to prolong OBU battery life. By prohibiting turning on main power-hungry RF transceiver and filtering non-wake-up and noise signals, it can be achieved. For this, to ensuring WuRx reliability and accuracy a configurable intelligent, multi-mode, and novel digital controller is proposed. The digital controller also replaces complex high-power analog blocks such as ADCs and bandwidth-pass filters with low-power, small-area. The complete configuration of the various parameters of self-hibernation, wake-up, digital hysteresis, watchdog timers, wake-on, and self-test makes the controller architecture very flexible and adaptable. The simplified architecture of the WuRx digital controller is described in Fig. 5 and the timing diagram is described in detail in Fig. 6 for the DSRC application. The SSM (Signal Selection Multiplexer) selects WU_SIG, the base wake-up signal from the comparator output during normal operation, or selects the self-test signal st_sig generated by the self-test pattern generator (STPG) during test mode.

The signal positive edge generator (SPEG) detects an upward transition from the selected signal wu_sig and makes a pulse signal wu_pe. The Finite State Machine Controller (FSMC) is an IDC core building block designed with controls and data paths. It primarily detects, guarantees, and generates wake-up interrupts and filters out unwanted signals. Controls other blocks, such as Configurable Watch-Dog Timer (CWDT), Adaptive Frequency Measurement Unit (AFMU), and Wake-On Generator (WOG). When enabled by the FSMC (fm_en = HIGH), the AFMU estimates the frequency of wake-up signal and generates an fm_det signal to determine whether the input signal value is within the configured range.

It also ensures a valid number of consecutive wake-up signal cycles configured (WU_N). CWDT starts the timer when activated by signal wdt_en from the FSMC. The timer duration can be configured in the WDTN parameter. This helps to improve IDC reliability and avoid disruptions during frequency measurement and signal guarantees. In the event of an abnormal situation, CWDT resets the FSMC to initial state when the configured timer runs out. WOG implements pseudo-synchronous interrupt generation. When enabled, a wake-on interrupt WO_INT is created instead of a wake-up interrupt. STPG improves WuRx reliability by verifying IDC operation in its own test mode. When enabled (st_en = 1), different frequencies and period counts can be used to generate various valid and invalid signals. The output multiplexer (OM) generates WU_INT by selecting the internally generated interrupt signal int_r or the external manual control interrupt WU_EXT. The Control Decoder (CDEC) decodes mode mode_ctrl, interrupt int_ctrl, and monitor_ctrl control signals from external CTRL inputs.

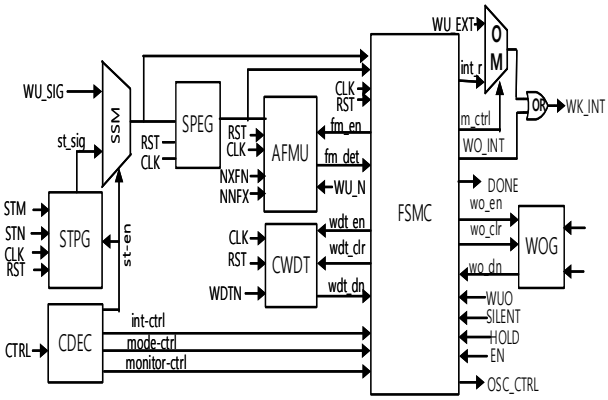


Fig. 5. RF WuRx intelligent digital controller (IDC) architecture

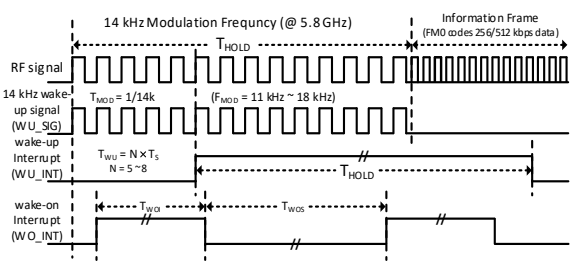


Fig. 6. RF wake-on and wake-up interrupt timing diagram

C. Ultra-Low Power Configurable RC Oscillator

The proposed WuRx incorporates an ultra-low-power configurable RC oscillator, a clock source for IDC. RC oscillator structures are adopted over crystal oscillators due to their low cost, low power consumption, fast start intervals, and easy on-chip integration [22]. The manufactured oscillator is fCLK.MIN~fCLK.It has a wide adjustment range of MAX and IDC controls capacitance values to configure for different frequencies in Wake-up, Self-hiberation, and Wake-on modes. For ultra-low power applications, it is recommended that the circuit operates in a weak inverted region, also known as a sub-threshold region [23], [24]. Therefore, the oscillator is designed to operate in areas below the threshold. Fig. 7 shows an ultra-low power RC oscillator [22]. The configurability for various frequencies is achieved by changing the resistance R and capacitance C values in IDC. The oscillator comprises a current reference, a start, a capacitor charge/discharge sensing circuit and a frequency generator.

The current source or sink circuit is preferably functioning in a weak inverted region for low power operation. The MOS transistor operates in a sub-critical region when the VGS, gate-source voltage, is lower than VTH, the threshold voltage, and the drain current ID flows. The diffusion current between the source and drain contributes primarily to this current. The starting circuit prevents the magnetic bias circuit from operating at the zero-bias point. A cascade of current mirrors is used to enhance the current sink or source output resistance. The current mirror uses the current and supplied to the capacitor, hysteresis controller M1 and the low current inverter for clock generation. When I, the drain current charges the capacitor C and the VC is equal to the hysteresis control transistor M1 VTH value, M1 is turned on. For clock frequency generator circuits, the voltage VC on capacitor C increases linearly with the increase in current I as constant current flows through the capacitor.

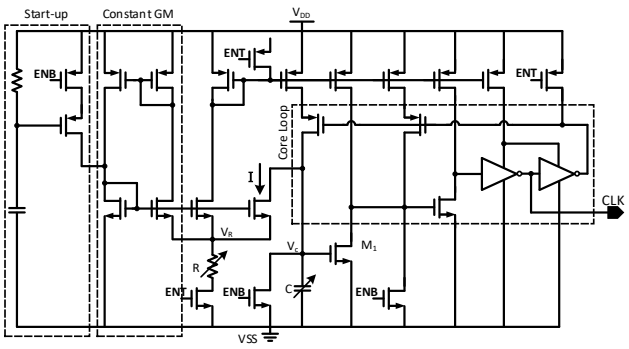


Fig. 7. Ultra--low power configurable range communication ((RRCC)) oscillator.

D. Front End Processing

The RF front end of the proposed WuRx consists of a highly sensitive RF envelope detector with built-in internal matching networks. RFED-based approaches are most common in designing WuRx circuits for low current consumption. This approach also eliminates LO generation requirements for frequency down-conversion and RF amplification at the expense of sensitivity reduction. Internal matching improves the sensitivity of the circuit. RFED is a main sub block of WuRx circuit for interfacing with the antenna over a matching network and for generating baseband output signals by down-converting input amplitude modulated RF signals. Fig. 8 shows the proposed RF envelope detector circuit with an internal matching network.

The circuit consists mainly of a nonlinear transistor element M1, an input signal DC cut-off capacitor C_{ac}, a magnetic bias feedback resistor Rf, a gate inductor Lg and an impedance matching network, and an excess capacitor C_{ex}. The impedance matching network provides manual voltage amplification. If the self-biasing resistance is large, V_{GS} of M1 MOSFET is near with V_{TH} with a very negligible bias current in the absence of an RF input signal. In this way, limited sensitivity problems due to VTH loss are compensated. Rf is designed with minimized parasitic capacitance and pseudo-resistance for small area large resistance. Fully disconnect the output voltage V0 from the RF input signal VRF and prevent envelope detector loading. When a VRF is applied, the drain current I1 increases exponentially, but the bias current from M2 is almost constant.

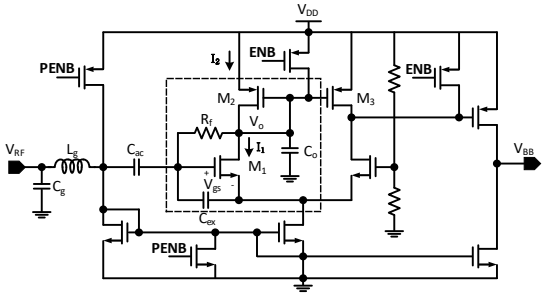


Fig. 8. RFED with matching circuit

III. RESULTS AND DISCUSSIONS

The proposed WuRx is integrated into the DSRC transceiver for ETCS applications in 180nm CMOS technology. Fig. 9 shows a microscopic photograph of WuRx and an enlarged IDC layout. The WuRx occupies 532 x 910μm^2, of which IDC accounts for only 94 x 82μm^2. WuRx is extensively measured to ensure reliability and accuracy. The laboratory environment is captured in Fig. 10(a) and the measurement board with the manufactured DSRC transceiver chip is shown in Fig. 10(b). The board is powered by an Agilent® DC power supply of 5V and the WuRx receives 0.9V power supply from LDO output circuit measured in the output pin with a digital multimeter (DMM). By using a lower supply voltage, we can minimize power consumptions and verify correct operation at the 0.9V supply voltage.

The measured wake-up OOK waveform is captured in Fig. 11. The OOK baseband wake-up signal is generated by the Tektronix® AFG3101 function generator and modulated to 5.8 GHz by the Agilent® E4438C signal generator. This modulated RF signal is fed to the RF_IN SMA input connector on the board, passes through the external pie matching network, package pins, and die PAD, and become input of WuRx circuit. The comparator output and WK_INT

signal are displayed in the Tektronix® DSA71254C digital serial analyzer. Various parameters and configurations are programmed through the SPI and graphical user interface (GUI) that runs on your computer.

The measured tuning range of the OSC is captured in Fig. 11. OSC capacitor C is implemented as a binary weighted capacitor bank controlled by the IDC's 8-bit OSC_CTRL signal. measured fCLK.MIN and fCLK. The MAX frequency is 12.16 kHz and 362.37 kHz, respectively, when both OSC_CTRL values are high and low, and the total frequency range CfCLK is 350.21 kHz. The spectrum also shows a WUM frequency consisting of approximately 140 kHz. In its own hibernation mode, the OSC frequency fSH consists of approximately 14 kHz. The WOM clock frequency depends on the parameters configured for the TWOI and TWOS intervals. It draws a 214 nA current from a 0.9 V power supply at 140 kHz, which is almost halved in its own hibernation mode.

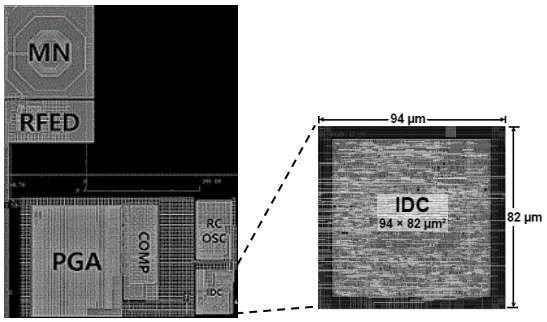
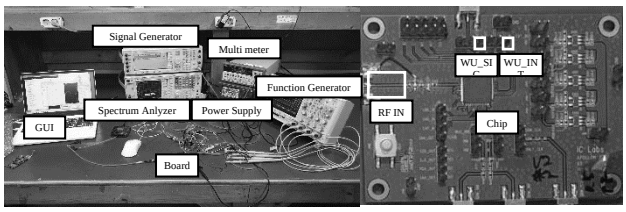


Fig. 9. WiRX amd IDC Chip Layout



(a) (b)

Fig. 10. WuRx measurement: (a) measurement equipment set (b) board and package layout

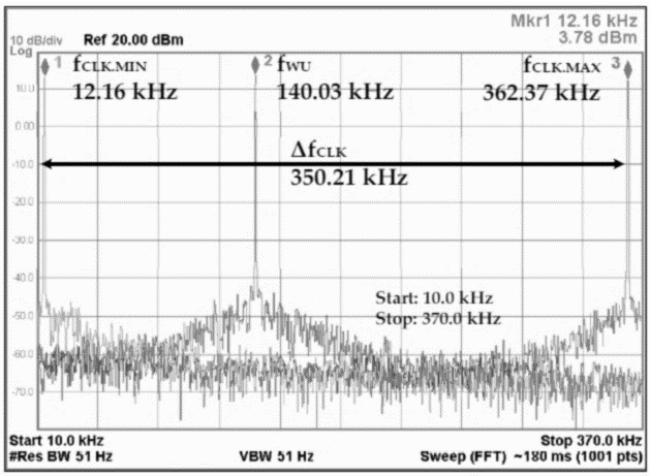


Fig. 11. Oscillator (OSC) frequency range and measurement result.

TABLE I. WuRx performance comparison

Parameter	[8]	[9]	[24]	This Work
CMOS Process (nm)	130	180	130	180
Wake-up Frequency (kHz)	14	7~42	14	1-140
Operating Frequency (GHz)	5.8	5.8	5.8	5.8
Sensitivity (dBm)	-44	-47	-45	-46
Power Consumption (µW)	36	3.8	45	2.48
Interface	BPF	FD	BPF	IDC

IV. CONCLUSION

This article provides a highly reliable RF WuRx for ETC systems. IDC is proposed as a final step to improve WuRx reliability and battery performance. IDC also acts as a filter and replaces complex and power-intensive analog blocks such as BPF, ADC, and FD. The proposed configurable digital controller provides high reliability and accuracy by detecting and ensuring the number of configurable continuous wake-up signal cycles before enabling a power-consuming RF transceiver. The proposed self- hibernation technology reduces IDC and RC oscillator current consumption and improves battery life during non-wake-up periods. Digital hysteresis accommodates wake-up signal frequency fluctuations and improves WuRx accuracy. Surveillance timers for IDC self-recovery are integrated to avoid uncertain conditions during poor and incorrect wake-ups. In Wake-up operation, digital controller consumes 34nW power and in self-hibernation mode, the current consumption reduced from 38nA to 9.5nA. A fully synthetic 180nm CMOS process with an area of 94 x 82µm2 requires 809 gates. The WuRx measured power consumption has a sensitivity of 2.48 µW, -46 dBm, and a 0.484 mm2 chip area. Through extensive measurement and validation, the proposed WuRx is an ideal solution for highly reliable DSRC wake-up circuits.

ACKNOWLEDGMENT

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