A 5-5.8 GHz Sub-2 dB NF CMOS Low Noise Amplifier with Bandwidth Extension and Noise Optimization Techniques

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Abstract – **A 5-5.8 GHz sub-2 dB noise figure (NF) CMOS low noise amplifier (LNA) with bandwidth extension and noise optimization techniques is proposed for WiFi applications. The proposed LNA was based on the cascode feedback topology for broadband input impedance matching characteristic, and adopted the double-stacked LC resonators as an output load in order to extend the gain-bandwidth from 5 to 5.8 GHz. In addition, the input matching network was designed to provide the optimum source impedance for the minimum noise figure (NF_{min}) over wide frequency range (5-5.8 GHz) using the source-pull simulation. Owing to the proposed noise optimization technique, the NF of the LNA can be close to NF_{min} over wide operating frequency range. The proposed LNA was designed using a 65-nm CMOS process. It showed a NF of less than 2 dB, a power gain (S_{21}) of greater than 15 dB, and an input and output return loss (S_{11} and S_{22}) of less than -10 dB over 5-5.8 GHz in the post-layout simulation. The simulated 2 dB gain bandwidth and input-referred third-order intercept point (IIP3) were 1399 MHz and -4.1 dBm, respectively, with dc power consumption of 7.4 mW.**

Keywords—Cascode, double-stacked resonators, feedback, LNA, minimum noise figure, noise optimization, optimum source impedance, source-pull, sub-2 dB NF, wideband, WiFi

I. INTRODUCTION

The WiFi standard has been considered to be the most promising wireless connectivity technology for Internet of Things (IoT) applications, and as a result, its market has grown explosively in recent years. Many researches have focused on the development of highly integrated CMOS WiFi transceivers supporting multiband and multimode for low cost. Recently, 2.4/5 GHz dual-band CMOS SoC transceivers supporting IEEE802.11a/b/g wireless local area network (WLAN) applications have been demonstrated successfully. In contrast to 2.4 GHz WLAN, which uses the same frequency band as microwave ovens and medical equipment, IEEE802.11a WLAN occupying 5 GHz frequency band experiences little radio interference, and as a result, is more appropriate for high data rate applications [1]. In addition, the new IEEE802.11ac standard operated in 5 GHz UNII band has been proposed to increase a maximum data throughput up to 80 or even 160 MHz by providing more channel bonding. Unfortunately, however, this new standard requires a high performance low noise amplifier (LNA) with wide bandwidth (> 1 GHz) and low noise figure (< 2 dB).

In this paper, a 5-5.8 GHz broadband CMOS LNA with bandwidth extension and noise optimization techniques is proposed to support advanced WiFi applications. In Section II, the circuit technique for the proposed LNA is presented. Section III presents the post-layout simulation results of the proposed LNA, followed by the conclusions in Section IV.

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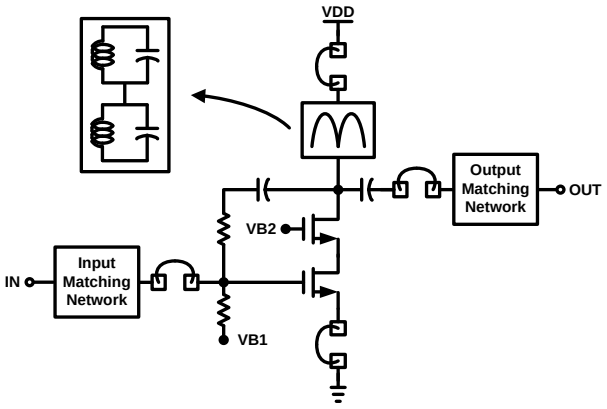


Fig. 1. Circuit schematic of the proposed LNA with bandwidth extension and noise optimization techniques.

II. CIRCUIT DESIGN OF PROPOSED LNA

Figure 1 shows the circuit schematic of the proposed LNA with bandwidth extension and noise optimization techniques. It is based on the cascode inductive source degeneration LNA employing resistive feedback in order to achieve wideband input impedance matching characteristic with low noise figure (NF). The source degeneration inductor is implemented using a bond wire because of relatively small inductance value at 5 GHz frequency band. The relatively high quality factor (Q-factor) of bond wire greatly reduces the silicon area and improves the NF of LNA.

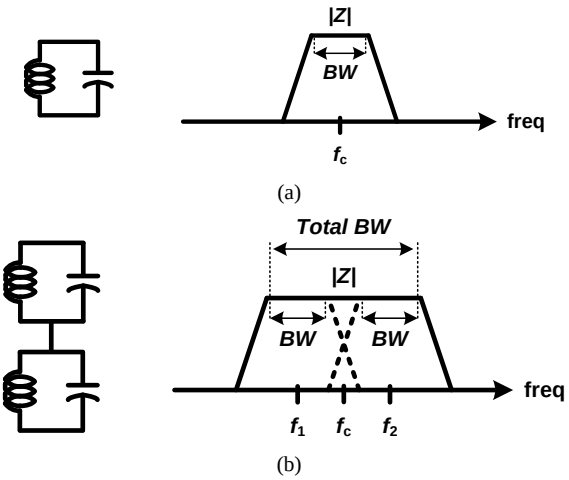


Fig. 2. Frequency characteristic of the (a) single LC resonator and (b) double-stacked LC resonators.

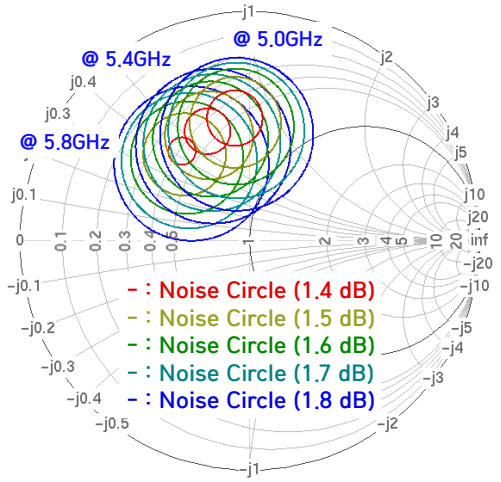


Fig. 3. Noise contour plot of the proposed LNA through source-pull simulation over 5-5.8 GHz frequency band.

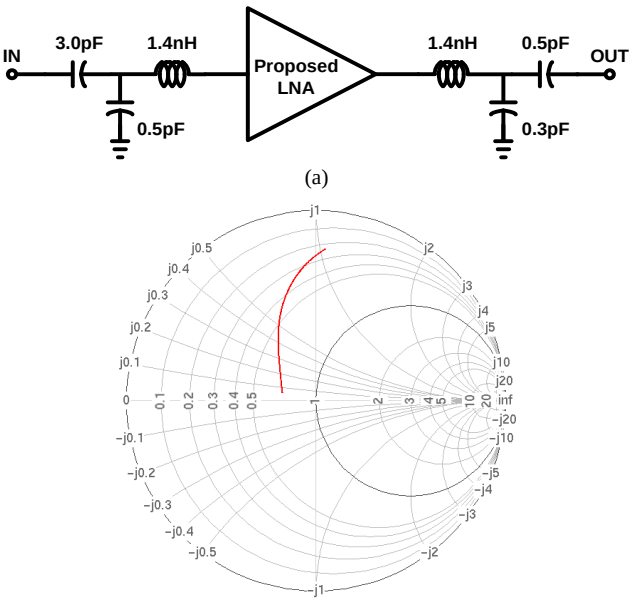


Fig. 4. (a) Schematic of the designed input and output matching networks, (b) trace of the impedance looking back into the input matching network form the gate node of the input transistor of the LNA.

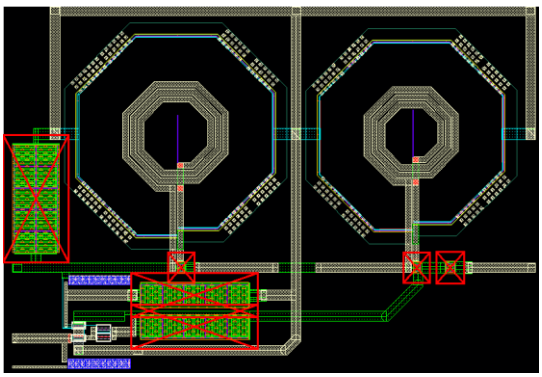


Fig. 5. Layout photograph of the proposed LNA.

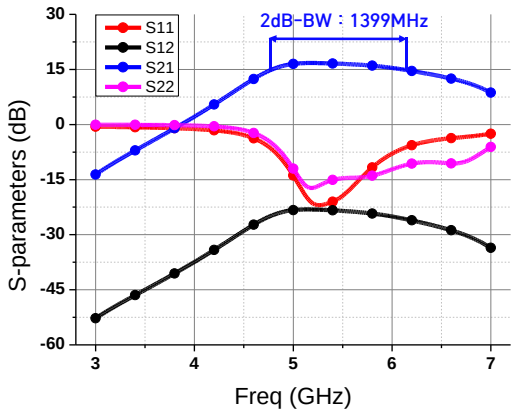
Figures 2(a) and (b) present the frequency characteristic of the single LC resonator and double-stacked LC resonators. The double-stacked LC resonators-based output load was already reported in the design of 2.4/5.2 GHz concurrent dual-band LNA [2]. Compared to the conventional work in [2], this design adopts the double-stacked LC resonators as an output load of the LNA in order to extend the bandwidth with sufficiently high gain and good gain flatness. By combining the two close resonance frequencies of the double-stacked LC resonators and adopting it as the load of the LNA, the gain bandwidth of the LNA is significantly extended. With the resistive feedback technique, the proposed LNA can achieve sufficiently high gain, good input impedance matching, and low NF performances in wideband.

Figure 3 shows the noise contour plot of the proposed LNA through source-pull simulation over 5-5.8 GHz frequency band. In the simulation, the minimum noise figure (NF_{min}) of the proposed LNA is around 1.4 dB over 5-5.8 GHz frequency band. In order to achieve NF performance close to NF_{min}, the impedance looking back into the input matching network from the gate node of the input transistor of the LNA should be matched to the optimum source impedance for NF_{min} over wide frequency range (5-5.8 GHz).

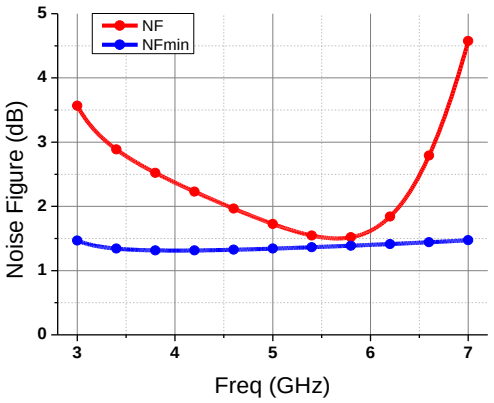
Figure 4(a) shows the schematic of the designed input and output matching networks. The off-chip LC components were used for the matching networks to provide some degrees of freedom for tuning while maintaining low NF performance. Figure 4(b) shows the trace of the impedance looking back into the input matching network form the gate node of the input transistor of the LNA. The impedance trace passes through the optimum source impedance points for NF_{min} over 5-5.8 GHz frequency band, as shown in Figure 3. This enables the proposed LNA to achieve low NF performance close to NF_{min} over wide operating frequency band, with good input impedance matching characteristic.

III. (POST-LAYOUT) SIMULATION RESULTS

The proposed LNA was designed using a 65-nm CMOS process. Figure 5 shows the photograph of the designed LNA. In the simulation, the spice models for ESD protection



(a)



(b)

Fig. 6. Post-layout simulated (a) S-parameter results and (b) NF performance of the designed LNA.

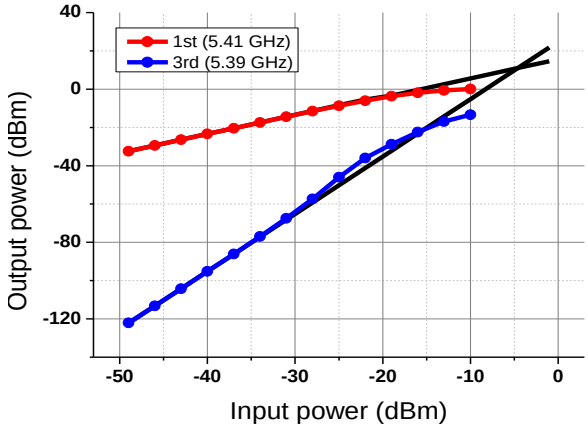


Fig. 7. Post-layout simulated input-referred third-order intercept point (IIP3) performance of the designed LNA.

diodes and bond wires were included for high accuracy simulation results. The off-chip LC components were employed for the input and output impedance matching networks to minimize NF degradation resulting from poor *Q*-factors of on-chip inductors, and real spice models for them were considered for the simulation.

Figure 6(a) shows the (post-layout) simulated S-parameter results of the proposed LNA. Both input and output return loss (S_{11} and S_{22}) are less than -10 dB over 5-5.8 GHz. The power gain (S_{21}) of the LNA becomes a maximum value of 16.8 dB at 5.2 GHz, and is about 16.5 dB and 16 dB at 5 GHz and 5.8 GHz, respectively. The simulated 2 dB gain bandwidth of the LNA is about 1399 MHz, and this is wide enough to cover the whole operating frequency band. Figure 6(b) shows the (post-layout) simulated NF performance of the designed LNA. The minimum NF is around 1.5 dB at 5.5 GHz, and the simulation result is less than 2 dB over 5-5.8 GHz frequency band. Owing to the proposed noise optimization technique, the simulated NF performance is quite close to NF_{min} over whole operating frequency band.

Figure 7 shows the (post-layout) simulated input-referred third-order intercept point (IIP3) performance of the designed LNA. In the simulation, two-tone spacing was 20 MHz. The value of IIP3 is about -4.1 dBm at 5.4 GHz frequency. The dc power consumption of the designed LNA is about 7.4 mW at a supply voltage of 1.2 V.

Table I summarizes and compares the performances of the proposed LNA with those of the previously published reports of LNAs [3]-[6]. Compared with the state-of-the-art in Table I, the proposed LNA achieved a lower NF with lower power consumption.

TABLE I. Comparison with previously published reports of LNAs

LNA	This Work*	[3]	[4]*	[5]	[6]
CMOS Technology (nm)	65	65	130	90	65
Frequency (GHz)	5-5.8	4.6-5.8	0.3-6	0.5-6.5	0.1-4.3
S_{11} (dB)	< -11.7	< -8	< -10	< -10	< -6
S_{21} (dB)	> 16	> 27	> 16.2	> 15	> 18
NF (dB)	< 1.74	< 1.9	< 2	< 3.2	< 4
Power consumption (mW)	7.4	16	19.2**	21.3	2
IIP3 (dBm)	-4.1	-10.3	-19.2	-9.5	-7.7
2 dB gain bandwidth (MHz)	1399	-	> 5000	> 5000	> 2900

(* : Simulation results, ** : Including output buffer)

IV. CONCLUSIONS

In this paper, a 5-5.8 GHz sub-2 dB noise figure (NF) CMOS low noise amplifier (LNA) with bandwidth extension and noise optimization techniques is proposed for WiFi applications. The cascode feedback and double-stacked LC resonator-based output load were adopted for good input impedance matching and sufficiently high gain over wide frequencies ranging from 5 to 5.8 GHz. The proposed LNA was designed using a 65-nm CMOS process, and showed an excellent simulated NF performance of 1.5 dB with lower

power consumption than conventional LNAs operating in the same frequency band.

ACKNOWLEDGMENT

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