Design of Power Management Integrate Circuit Implemented at the Active EMI Filter

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Abstract **- This paper proposes the design of power management integrated circuit (PMIC) within the active EMI filter (AEF). The buck converter has been implemented with AEF circuit. The designed IC is fabricated by TSMC 180nm BCD process. Semiconductor layout design including the above PWM signal generation circuit, 45V Power NDMOS and gate driver, and the overall size of the Buck converter is 2500μm*2500μm. The performance of the buck converter has been measured by oscilloscope after chip on board (COB) process. Input voltage range was 15v to 36v to generate 12V, and peak efficiency was measured as 66%. The AEF achieves better noise attenuation performance than 2stage L-C passive EMI filter (PEF) as about 6dB at 150khz, and the designed 1stage AEF totally attenuates 36dB from the bare noise without any resonance peak at over 1Mhz unlike the case of 2 stage L-C PEF. The active EMI filter with PMIC has been achieved better performance than larger size of passive EMI filter.**

Keywords**—Active EMI Filter (AEF), Bipolar-CMOS-DMOS (BCD) process, Conducted Emission (CE), Electromagnetic Interference (EMI), Integrated Circuits (ICs), Power Management IC (PMIC)**

I. INTRODUCTION

In the power conversion system, with higher power and smaller size, noise countermeasures (Conducted or radiated electromagnetic interference, EMI) due to conductive or radiated electromagnetic interference are being taken seriously. In the case of conductive noise, since it may cause electromagnetic malfunction or performance degradation in the connected power grid or other systems, various international standards limit the size. In order to suppress the EMI, an EMI filter is designed and usually installed at the entrance of the power line. The EMI filter blocks the noise by maximizing the impedance mismatch on the transmission path from the noise source. However, in the case of a passive EMI filter, the size and price of a device used due to a heat problem increases rapidly as the power capacity increases.

Recently, in addition to passive noise blocking, an attempt has been made to remove EMI noise by actively canceling noise as shown in Fig. 1. Thus, if conductive noise is sensed and a signal of the opposite phase is generated and emitted, each noise is canceled, and the noise can be removed. Compared with the conventional passive EMI filter, the active EMI filter has the advantage that the size and heat generation increase according to the increase in power is insignificant. However, if an accurate power supply is not made to the active EMI filter, it is difficult to expect a malfunction of the active EMI filter and thus a noise reduction effect. Therefore, it is intended to solve the power supply problem in the active EMI filter through the design of the dc-dc converter.

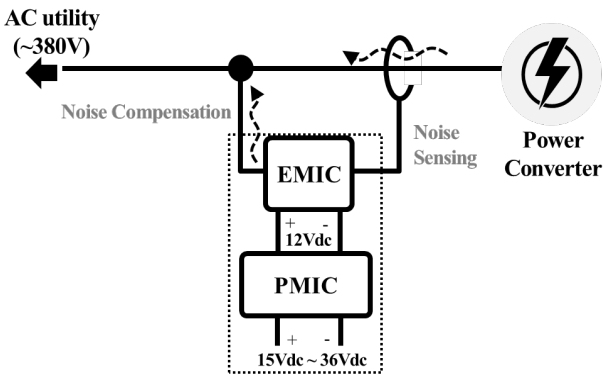

Fig. 1. Operation concept of active EMI filter with PMIC

II. DESIGN SEPCIFICATION

Fig.2 shows the simplified structure of the buck converter, which is one of the dc-dc converters, and is largely divided into an off-chip part and an on-chip part. Off-chip part consists of LC filter and compensator, and on-chip part is again divided into power stage and controller block. For example, the designed converter circuit aims to make an output voltage of 12V by receiving an input voltage of 24V from the outside. In consideration of the operation of the active EMI filter existing in the load stage, the specification at the time of design is first determined as shown in Table 1. The ripple of the output voltage is caused by the switching operation in the buck converter, and it is limited to within 5% of the maximum output voltage in consideration of the power supply stability in the load. Also, since the output voltage from the buck converter becomes the power supply

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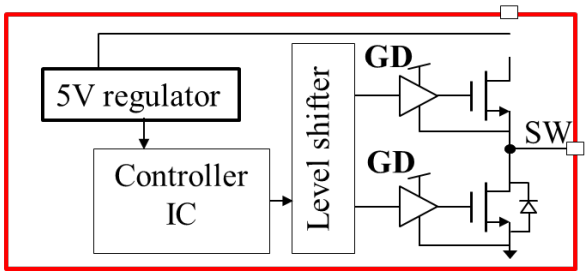


Fig. 2. Simplified diagram of PMIC block

of the active EMI filter, the maximum output current is determined to be 500mA to supply sufficient current during operation. Main circuit components were designed as following lists; Main buck converter: Wide Input Voltage Range from 12.5 V to 36 V, 12-V output voltage, Voltage Mode Control with Voltage Feed Forward, Programmable Frequency Between 500 kHz and 1MHz (Optional. Typ. = 1 MHz), 1.2 V Reference Voltage with 1% Accuracy, Programmable Closed Loop Soft-Start, ENABLE with 1-μA Low Current Shutdown Integrated Bootstrap Diode. Moreover, Monitoring circuit and Thermal protection circuit with Integrated Thermal Shutdown at 85°C with Hysteresis.

TABLE I. Specifications for buck converter considering active EMI filter

Parameter	Target value or range
Input voltage	12V to 36V
Output voltage	11V to 12V
Maximum output Voltage ripple	± 5% (0.6V for 12V output)
Maximum output current	500 mA
Power efficiency	> 80%

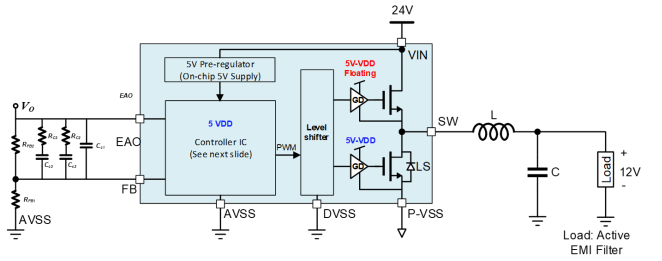
III. CIRCUIT SIMULATION

The design of the buck converter circuit in Section II starts with determining the required specification. In the case of LC filter and compensator, which are off-chip parts, device values are determined through MATLAB and simulation is performed through PSIM program. Other circuit parts are designed using Cadence Virtuoso program and simulated using Specter program. If the given specification is not satisfied, the circuit design is modified. We plan to use Cadence Virtuoso program for layout and routing, and plan to verify DRC and LVS using Mentor Caliber Tool. After that, post-layout simulation is performed using the Specter program, and if all requirements are satisfied, the design process is completed.

The structure of Buck converter for the integrated circuit is introduced. Representatively, there are controller IC, 5V pre-regulator, power switch, and drivers. The task for IC design block should be distributed depending on the time-schedule. The Off-chip area and On-chip area part are divided for practical use, and the device characterization should be also required for the simulation in case of the off-chip devices. PSIM simulation has been done and next moves to the cadence simulations.

As mentioned above, in the case of the LC filter and compensator part, the device value can be calculated through the related formula. Fig. 3 shows the simulation setup and results in the PSIM program. At this time, the parts other than the calculated device were replaced with ideal behavior modeling. It was confirmed that the simulation results were consistent with the expected results and satisfied the specification.

Basic design specification of the Buck converter has been decided and confirmed. Input voltage range of the buck converter is confirmed as 12.5V ~ 36V, while the output



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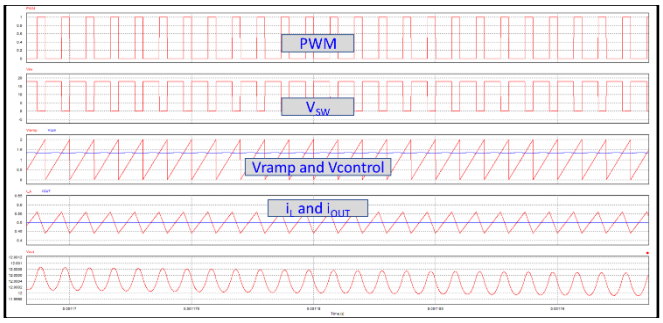
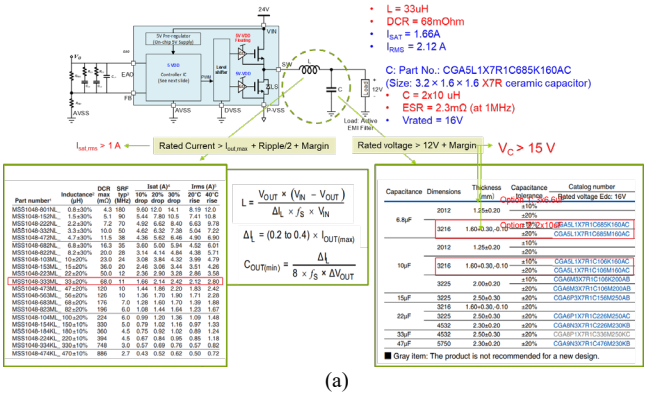
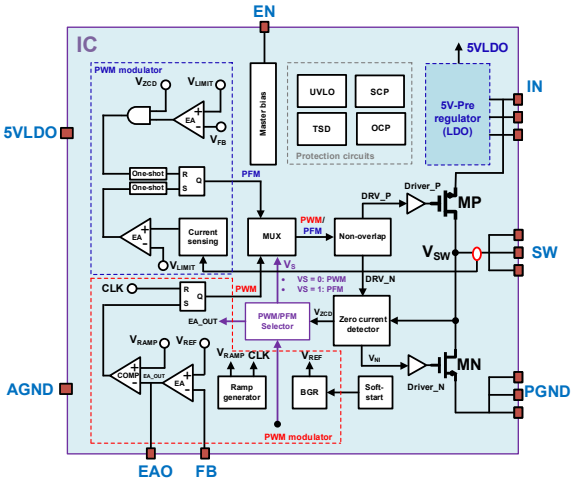


(b)

Fig. 3. (a) Circuit of the power stage setup (b) Simulation results



(a)



(b)

Fig. 4. Block diagram for on-chip part in buck converter

voltage should be 12V. Output current specification is confirmed as 500mA. The TSMC 0.18μm BCD process was employed to implement the Buck converter design, and the corresponding PDK will be utilized for the design. Fig. 4 shows the block diagram of the on-chip part of the buck converter. There are several circuits in the power stage and controller block, and we plan to design them to show optimal performance by referring to various papers and materials.

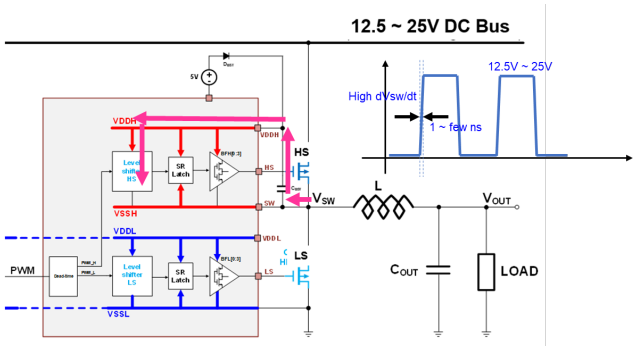


Fig. 5. Level shifter schematic and operation

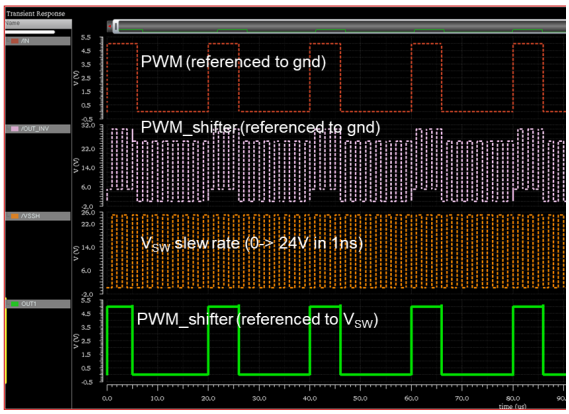


Fig. 6. Level shifter simulation

Several detail configurations of layout have been demonstrated and confirmed. The detail circuit diagram including digital circuits and analog circuits are confirmed.

Fig. 5 shows the circuit of the level shifter block with external bootstrap capacitor and diodes. The function of the level shifter was verified by simulation as shown in Fig. 6. LVS and DRC are also simultaneously checked. Over-current detection circuit are confirmed at the total system checking progress by using total circuit diagram. Other detail tuning has been performed at the LDO and BGR. Several detail configurations of layout have been demonstrated and confirmed.

Ramp generator and level shifter has been designed to achieve more accuracy for rising slope and falling slope. Those operation can be controlled by the bias current to each comparator inside the Ramp generator. Rail-to-rail Op-amp has been confirmed.

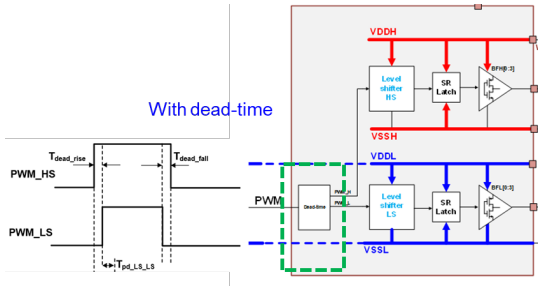


Fig. 7. PWM Controller test setup

In DC-DC converter design, the key design is the PWM signal generation circuit, and Fig.7 shows the PWM signal generation circuit diagram. An IC that can operate from 5% to 95% of duty ratio with a 1Mhz cycle is designed through a ramp generator, rail-to-rail operation-based op-amp, and various logic circuit diagrams.

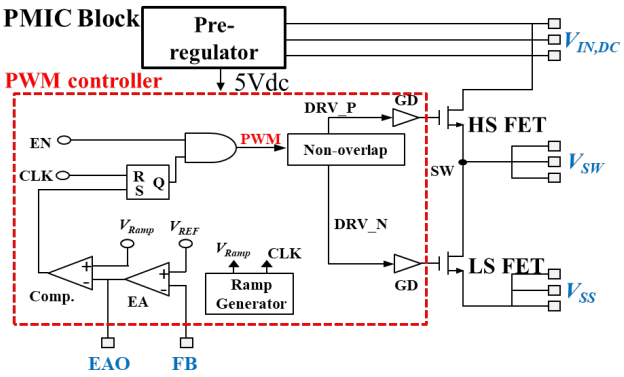


Fig. 8. Schematic of overall PMIC block

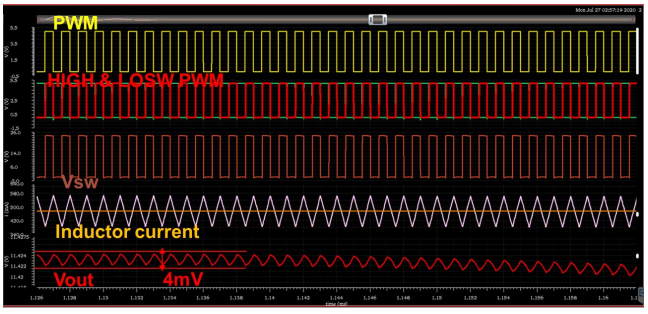


Fig. 9. PMIC simulation tests

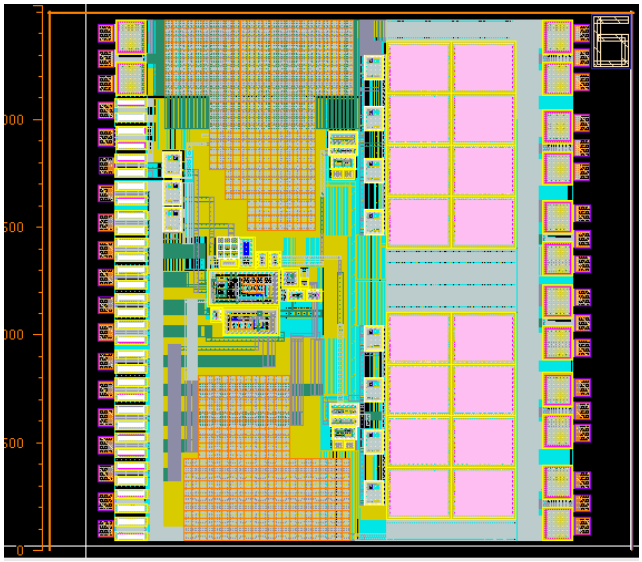


Fig. 10. Total layout of buck converter including power MOSFETs.

Fig. 8 demonstrates the overall PMIC block in the designed buck converter. The circuit includes power FETs, and the function was verified by post-layout simulation as shown in Fig. 9. Output voltage ripple was measured as 4mV and it can verify the AEF performance. Fig.10 shows the semiconductor layout design including the above PWM signal generation circuit, 45V Power NDMOS and gate driver, and the overall size of the Buck converter is 2500μm*2500μm. In this case, the maximum output current was designed as 1 $A_{rms,max}$.

IV. EXPERIMENTAL RESULTS

Fig. 11 depicts the chip-on-board process following the actual semiconductor fabrication. It has been verified that the generated PWM signal aligns with the simulation outcomes, and field test validation is currently being conducted to assess the functionality of the actual Active EMI Filter as a load in power electronics applications.

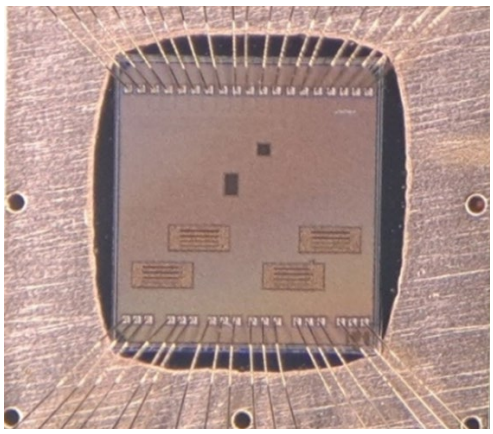


Fig. 11. Photograph of chip on board

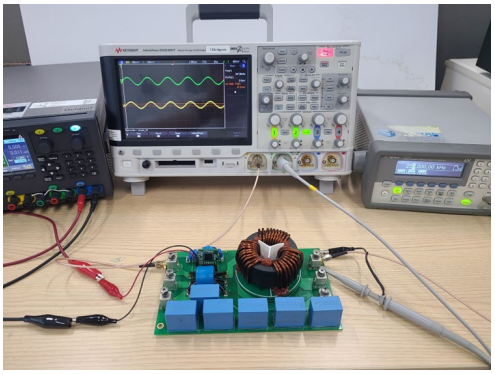


Fig. 12. Photograph of test set-up

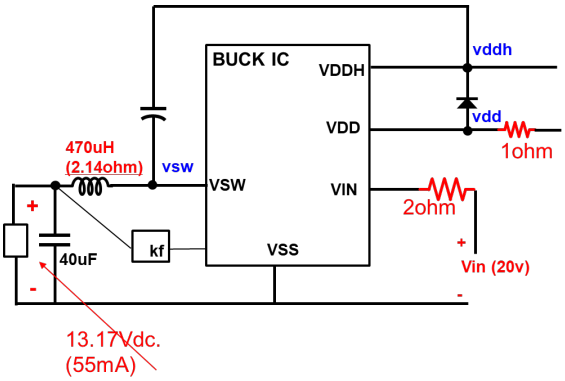


Fig. 13. Configuration of Test set-up

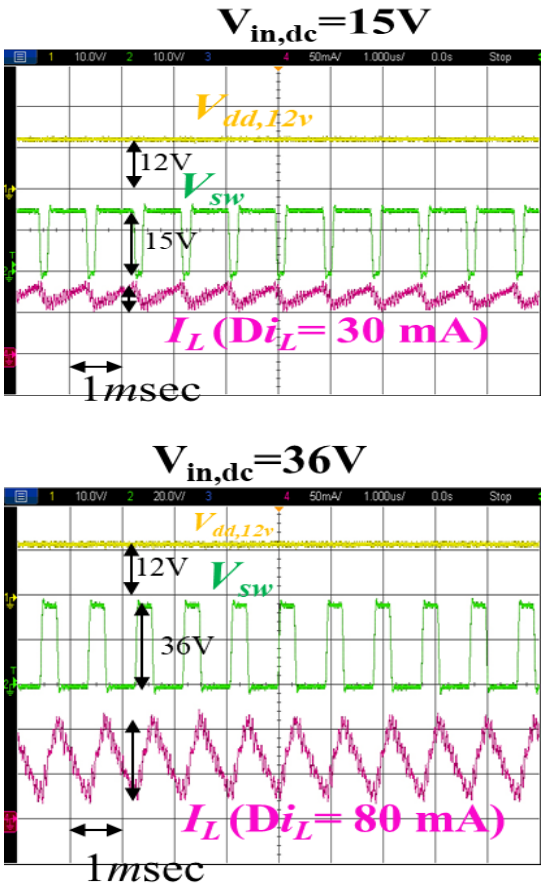


Fig. 14. Waveform of buck converter PMIC at operation of (a) $V_{in,dc}$=15V, and (b) $V_{in,dc}$=36V.

Fig.12 shows the photograph of test set-up for measuring the voltage and current at PMIC block. Fig. 13 shows the configuration of the test-setup to initialize the buck converter operation. Fig. 14 shows the measured waveform about the PMIC operation. Output inductor of 47uH and output capacitor of 20uF were designed at off-chip region. Feedback resistors and capacitors at error amplifier were also implemented at off-chip area tuned to achieve sufficient loop gain as shown in the figure. Output load of PMIC block is EMIC circuit block and 12V-region circuit at MD circuit block, and load current is estimated as 68mA at 12V supply. The designed buck converter operates based on PWM control with a fixed 1MHz switching frequency. Waveform of output voltage, switching node, and inductor current were simultaneously measured by oscilloscope when the input dc voltage is supplied by 15V and 36V, respectively. The duty ratio is well controlled according to the ratio of input voltage to fixed 12V output. Peak efficiency of total buck converter system was measured as 66.3% with input 15V and output 12V condition. Most of loss was caused to drive the initializing circuit and pre-regulator to drive the controller IC rather than switching loss. Especially pre-regulator needs to be improved.

As a result, it is possible to apply an arbitrary DC voltage up to 36V to the active EMI filter, which previously had to input only 12V, so that various system power sources can be used in practice.

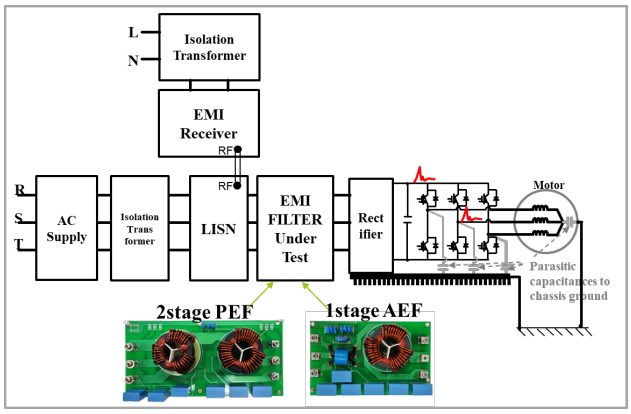


Fig. 15. Configuration of conducted emission measurement set-up

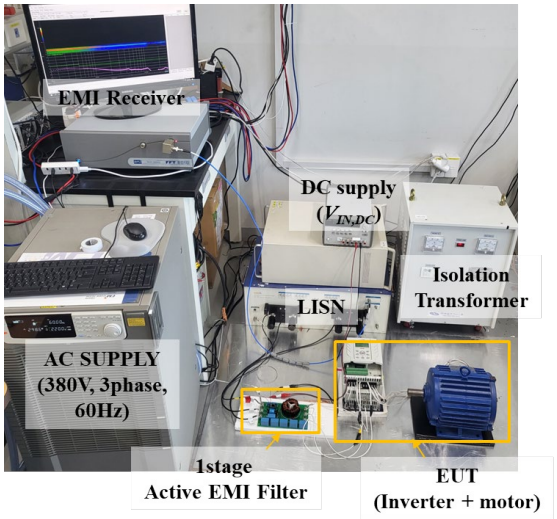
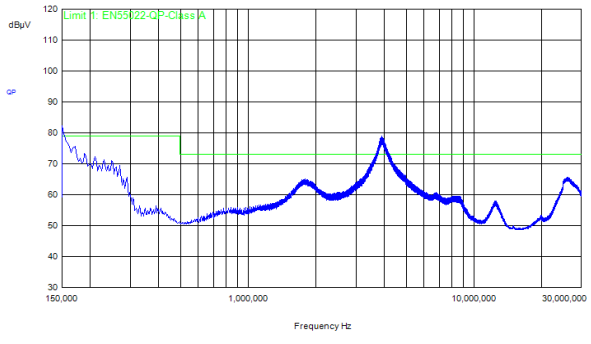


Fig. 16. Photograph of conducted emission measurement set-up



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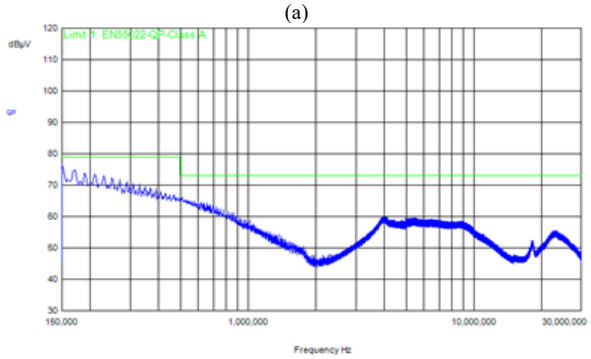

(b)

Fig. 17. Measured conducted emission of (a) 2-stage PEF and (b) 1-stage AEF with PMIC

Fig. 15 demonstrates the test set-up of the conducted emission. The noise attenuation performance of the proposed AEF with EMIC and PMIC was verified by the CE measurement with 34kW inverter and motor system as shown in Fig. 16. Bare noise of the EUT is measured as 112dBuV at 150khz, and the noise drastically decreases after 10Mhz. To compare the noise attenuation performance with PEF, 2stage L-C passive EMI filter (PEF) and stage L-C-L PEF were compared with 1stage AEF, where the stage counts the set of CM choke and Y-capacitor. In Fig. 17, the measured CE results are summarized. The AEF achieves better noise attenuation performance than 2stage L-C PEF as about 6dB at 150khz, and the designed 1stage AEF totally attenuates 36dB from the bare noise without any resonance peak at over 1Mhz unlike the case of 2 stage L-C PEF.

V. CONCLUSION

The manufactured chip will contribute to maximizing the noise reduction effect of the active EMI filter by solving this power supply problem. The designed buck converter operates from input voltage of 15V-36V, to generates 12V dc output voltage. Noise attenuation performance has been measured by conducted emission measurement with inverter motor, and the active EMI filter with PMIC has been achieved better performance than larger size of passive EMI filter.

ACKNOWLEDGMENT

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