A Leakage-Tolerant 4.58μJ·ppm$_2$ -FoMs Reconfigurable RC-to-Digital Converter for Multi-Sensor Readout

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Abstract **- This brief presents a leakage-tolerant high-resolution reconfigurable RC-to-digital converter (R^{2}CDC) that can readout multiple resistance/capacitance sensors using swing boosted period-modulation (SB-PM) front-end. This R2CDC employs SB-PM front-end and first-order noise shaping block that results in 23.03aF Abs. Resolution. Compared to the conventional design, the leakage current was reduced by at least 15.67 times. Implemented in a 0.18μm standard CMOS process, the proposed (R^{2}CDC) consumes 56.38μA from a 1V supply, occupying an active area of 0.0275 mm^2, achieving FoM$_S$=4.58μJ·ppm$_2$, FoM$_W$=0.359pJ/Step efficiency at a measurement time of 500μs.**

Keywords**—Low phase noise, Jitter, Relaxation oscillators, Swing-boosting**

I. INTRODUCTION

Major industries such as IoT and electronics are developing rapidly, using sensors to automate and improve human life. For example, various wearable devices and smartphones detect information such as a user's heart rate and exercise environment through sensors and provide convenience. With the release of devices utilizing these sensors, the IoT era will come, and the trillion sensors era will soon arrive, in which trillions of sensors will be placed around people. Hence, the future sensor system's sensing factors such as bio signals and temperature are low-cost, low-power, and low-area. However, looking at the sensor systems developed so far, different sensor ICs are used for various types of sensing such as temperature, gas, humidity, and touch. These sensor ICs usually use a digital converter to sense resistance (temperature, gas, etc.) or capacitance (humidity, touch, etc.). Due to this different R or C sense, it is tough to miniaturize the system and low power. In addition, each sensor IC development requires a lot of money and time, and each time a new sensor is added, a new IC needs to be developed, which increases the production cost. Therefore, a reconfigurable sensor system capable of various sensing types through one semiconductor IC is suitable for the IoT industry or trillion sensor eras to come. For this, there are many elements that a reconfigurable sensor must have.

As mentioned earlier, the first is low-cost, low-power, and low-area. Therefore, in the case of the reconfigurable RC-to-digital converter (R2CDC) [1], R and C can be measured with one IC instead of each, so inherently low-cost, low-power, and low-area are possible. Second, the wide input range of the sensor element must be secured to satisfy the operating range. Third, high resolution is required to convert accurate sensing values to digital. Finally, for reconfigurability, multi-sensor readout is needed rather than single sensing. In particular, when sensing one sensing factor for multi-sensor readout, the other off-sensing factors should have little effect. Due to negative effects such as leakage current, the accuracy of the sensing factor is lowered. Hence, it is essential to reduce the leakage current for the off-sensing factor.

In this brief, we proposed a leakage-tolerant relaxation oscillator-based RC-to-digital converter (R^{2}CDC) that achieves a 3x3 sensing branch for multi-sensor readout. Multi-sensing is possible by reducing the off-state leakage current by at least 15.67 times. The proposed R^{2}CDC uses a swing-boosted period modulation (SB-PM) front end whose phase noise performance allows for an absolute resolution of 23.03aF. Additionally, based on high-resolution achieving FoMs = 4.58μJ·ppm$_2$, FoMw = 0.359pJ/Conversion.Step efficiency at a measurement time of 500μs, respectively. And the active area occupies only 0.0275mm^2 in a 180nm standard CMOS process.

This brief is organized as follows. Section II discusses the proposed reconfigurable RC-to-digital converter and design considerations. Section III presents implementation details of the proposed R^{2}CDC. Measurement results are shown in Section IV, and Section V concludes this brief.

II. PROPOSED RECONFIGURABLE RC-TO-DIGITAL CONVERTER

A. Design Considerations for Reconfigurable RC-to-Digital Converter

Fig. 1 shows a conceptual overview and key considerations of the reconfigurable RC-to-digital converter, the key considerations are as follows:

1) High-resolution to accurately digitize C/R sensing.
2) Wide input range that satisfies the sensor operating range.

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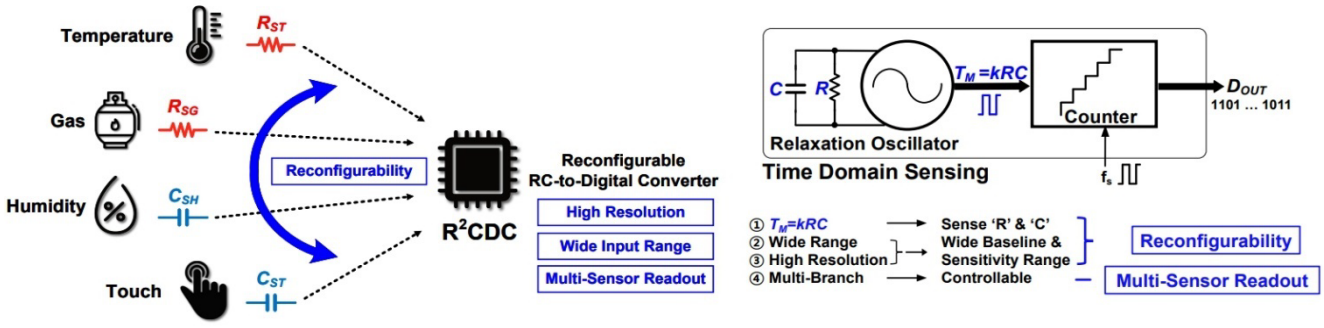


Fig. 1 Conceptual overview of the reconfigurable RC-to-digital converter (R^2CDC)

3) Controllable multi-sensor readout that can perform various sensing, the effect on off-sensing branch should be small.

As shown in Fig. 1, in time domain sensing using a relaxation oscillator, the period is proportional to R or C, respectively, so it can be easily digitized using a counter. Also, an inherently wide input range is achieved by direct RC-to-time conversion through the period. High resolution is achieved using the swing-boosted period modulation front-end that phase-noise performance is close to the fundamental limits [2]. In addition, the resolution of R^2CDC is maximized by quantization noise reduction by using a first-order noise shaping block. Furthermore, multi-branch is possible by using the controllable switch. hence multi-sensor readout is achieved.

B. R^2CDC Architecture

The overall architecture and sensor oscillator (SOSC) of the R^2CDC is shown in Fig. 2. The SOSC period T_M is proportional to the external capacitive sensor and the resistive sensor by 3x3 multi-sensor readout. And it comprises the 8-bit up counter and the first-order noise - shaping digital block. The digital output is determined by the inverse of the SOSC period and the external sampling frequency f_S:

$$D_{OUT} = \frac{f_M}{f_S} \quad (1)$$

Fig. 2(b). shows the schematic of the swing-boosted sensor oscillator (SOSC). The controllable switch is composed of the tri-state inverter and is operated by an 8-bit control signal. And the voltage swing of V_{MID} which is the input of the comparator inverter (INVC) is $2V_{DD}$ from $-V_{TH}$ to $V_{DD}+V_{TH}$. Phase-noise FoM close to the fundamental limits by using swing-boosted node V_{MID}. The SOSC can readout the external capacitive sensors (C_0, C_1, C_2) and the external resistive sensors (R_0, R_1, R_2). To configure the SOSC to capacitive sensing mode, along with the switch signal S_0, one of the three capacitive sensors signal ($S_{5\text{-}7}$) to be sensed is selected and driven, and the off-sensing switches are disabled. The period of capacitive sensing mode is given as [2]:

$$T_{M\_Capacitive} = 2R_{ZTC}C_{0\text{-}2}ln(3). \quad (2)$$

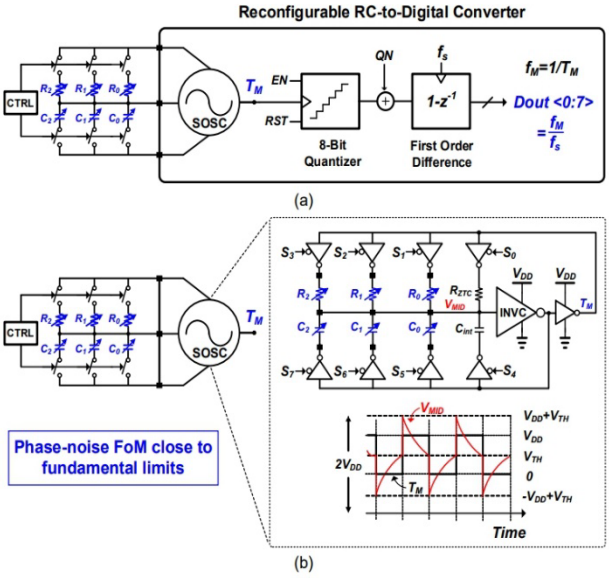


Fig. 2 Proposed R^2CDC system architecture (a) and sensor oscillator (SOSC) (b)

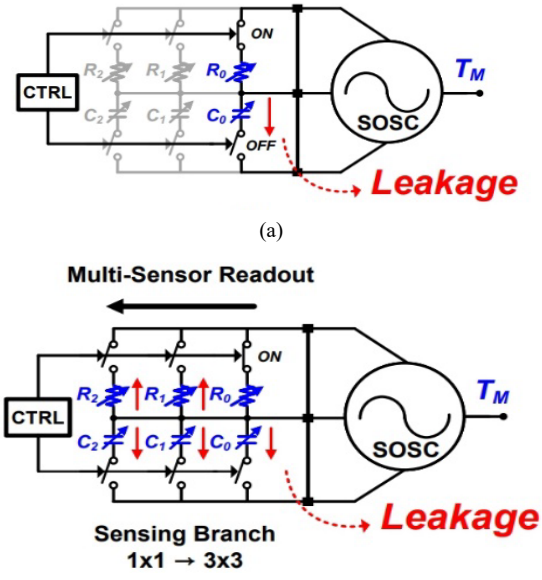


Fig. 3 Leakage current problem on 1x1 branch (a) and leakage current on multi-sensor readout (b)

The period is determined by the capacitive sensors $C_{0\text{-}2}$ and the on-chip zero temperature-coefficient (R_{ZTC}) [1]. The resistive sensing mode is an operation similar to the capacitive sensing mode, along with the switch signal S4, one of the three resistive sensors signal (S1-3) to be sensed is selected and driven. The period of resistive sensing mode is:

$$T_{M\_Resistive} = 2R_{0\text{-}2}C_{int}ln(3). \quad (3)$$

The period is determined by the resistive sensors $R_{0\text{-}2}$ and the on-chip capacitor C_{int}. Hence, reconfigurable sensing is achieved by simultaneously measuring capacitive and resistive sensors via two readout operations.

III. IMPLEMENTATION DETAILS OF THE PROPOSED R2CDC

In designing the multi-sensor readout of SOSC, the effect of the off-sensing branch should be reduced. However, there is a design issue that leakage current. Fig. 3(a). shows the leakage current problem in single-sensor readout, that is, 1x1 branch. To sense resistive sensor R_0, turn on R_0 and turn off C_0. When the multi-sensor readout is 3x3 branch, the leakage current flow is proportional and can be seen in Fig. 3(b). At this time, the leakage current deteriorates the sensing value T_M of SOSC and lowers the sensing accuracy. As a result, the T_M variation becomes 5.94% from 1x1 to 3x3 branches. Fig. 4. shows a conventional tri-state inverter and the path through which leakage current flows, and switches exist in the path of leakage current. And a large-size transmission gate to reduce turn on resistance is the dominant source of leakage current. To overcome the problem, it is solved by sending the switches in the path to the input node.

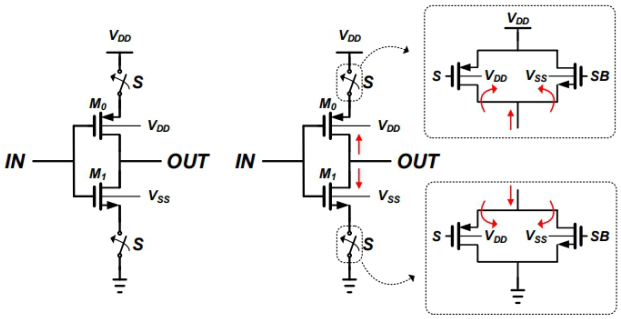


Fig. 4 Conventional tri-state inverter (a) and path through leakage current flows (b)

First, switches do not exist in the leakage current path. Second, the effect on the V_{MID} node is reduced, no need for large size switches. Fig. 5. shows the proposed tri-state inverter [3], and has a structure with switches at the input node that overcomes the aforementioned problems. Furthermore, since the output is the swing-boosted node, the input must not be floating. However, proposed tri-state inverter inherently prevents it. Fig. 6(a). shows the conventional and proposed RMS leakage current simulation results. At 6pF, the leakage current of the conventional design is 37.55μA, and the proposed design is 2.4 μA, which has been reduced by at least 15.67 times in the sensing range 6pF to 101pF. Also, in the case of peak current, it was reduced by 38time from 728.1 μA to 19.15 μA. Fig. 6(b). shows simulation results for measured frequency according to sensing branches. As the branch increases due to leakage current, the sensing accuracy deteriorates from 4.781MHz to 4.497MHz. In the case of the proposed design, the frequency variation is only 0.44% from 4.84MHz to 4.827MHz by effectively reducing the leakage current.

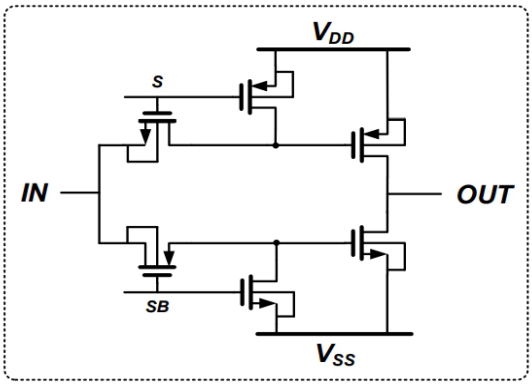
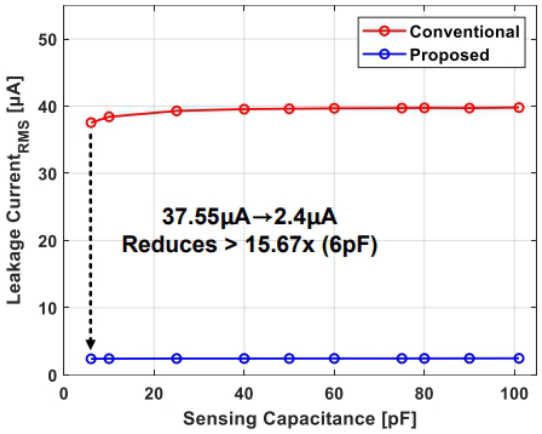
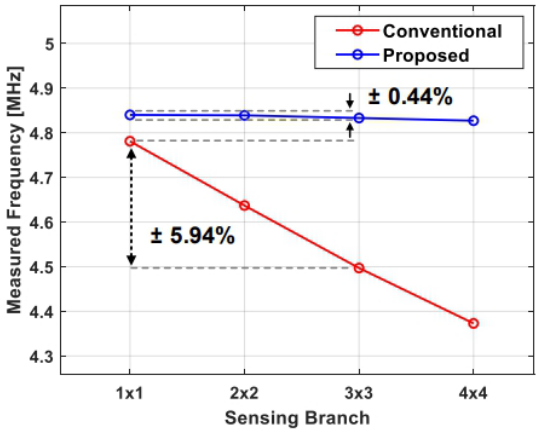


Fig. 5 Schematic of proposed tri-state inverter



(a)



(b)

Fig. 6 Simulation results for conventional and proposed RMS leakage current (a) and frequency variation of sensing branch (b)

TABLE I. Performance Summary and Comparison

	[1]	[4]	[5]	[6]	This Work
Technology [nm]	180	180	180	180	**180**
Architecture	SB-PM	2nd ΔΣ	Zoom SAR + TD ΔΣM	Self-Cal. Ring Oscillators	**SB-PM**
Supply [V]	1	1.5	1.1	0.3 – 1.8	**1**
Sensor Types	Cap / Res	Cap	Cap	Cap	**Cap / Res**
Area [mm^2]	0.175	0.11	2.94	0.2	**0.00275**
Input Range	0-40nF 15k-10MΩ	1p-10nF	0-18.12pF	0-30pF	**3.25-100.1pF 8.2k-64kΩ**
Power [μW]	140	15	2.92 – 3.09	0.00137	**56.38 [@6.25pF]**
Meas. Time [μs]	2930	130	850	1040000	**500**
ENOB	16.63	11.44	6.84	14	**16.26**
Abs. Resolution [aF]	114	207	116 [@40fF] - 1240 [@17.1pF]	67000	**23.03 [@6.25pF]**
FoMs [μJ·ppm^2]	39.88	250	165	86963	**4.58 [@6.25pF]**
FoM$_w$ [pJ/c-s]	4.044	0.7	0.66	11.1	**0.359 [@6.25pF]**
# of Sensing Branches	1x1	-	-	-	**3x3**

IV. MEASUREMENT RESULTS

The proposed leakage tolerant R^{2}CDC is implemented in a 0.18 μm standard CMOS process and occupies an active area of 0.0275mm^2. Compared with the conventional R^{2}CDC [1], although the sensing branch increased from 1x1 to 3x3, the area decreased six times. The chip photograph is shown in Fig. 7. The proposed R^{2}CDC consumes 56.38μW power from a 1V supply at a measured capacitance of 6.25pF. Fig. 8 shows the measured capacitance digital output and input capacitance range. The input sensing range of the capacitor is 6.25pF to 100.1pF. Fig. 9 shows the measured resistance digital output and input resistance range. An input range of 8.2kΩ to 64kΩ is measured. The measured phase noise of the SOSC is shown in Fig. 10. Based on the phase-noise FoM$_{OSC}$ of the sensor oscillator is higher than 158 dBc/Hz at offset frequency over 1kHz. The absolute capacitance resolution of the R^{2}CDC over 6.25pF to 35pF is shown Fig. 11. From a measured phase noise of SOSC, the absolute capacitance resolution is achieved 23.03aF at 6.25pF. The measured noise spectrum of the proposed R^{2}CDC is shown in Fig. 12. It can be seen that the proposed R^{2}CDC achieves lower noise power by using high-resolution SOSC and first-order noise shaping block. The figure of merits (FoM$_w$, FoM$_s$) of the capacitance-to-digital converter are defined as follows:

$$\text{FoMw} = \frac{\text{Power} \times \text{Meas. Time}}{2^{\text{ENOB}}} \tag{4}$$

$$\text{FoMs} = \text{Power} \times \text{Meas. Time} \times \left(\frac{10^6}{2^{\text{ENOB}}}\right) \tag{5}$$

The proposed R^{2}CDC achieves FoMw and FoMs of 0.359pJ/conv.step and 4.58μJ·ppm$_2$, respectively, at a measurement time of 500μs and an input capacitance of 6.25pF. The performance of R^{2}CDC is summarized in Table I and compared to other digital converters having high-resolution and improved FoM. Furthermore, compared with conventional R^{2}CDC [1], the resolution is improved by 5 times, and for FoM$_w$ and FoM$_s$ by about 11 times and 8 times, respectively, it is more suitable for reconfigurable RC-to-digital converter.

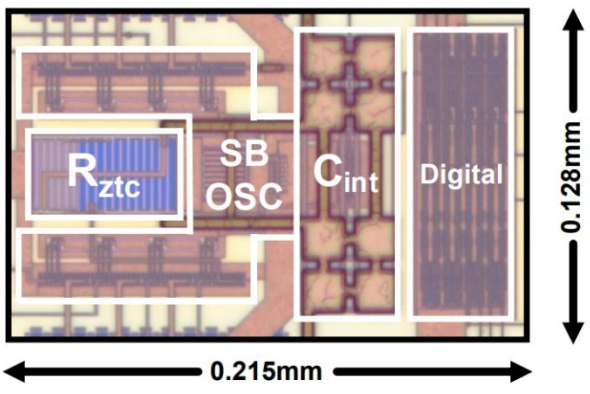


Fig. 7 Chip Photograph

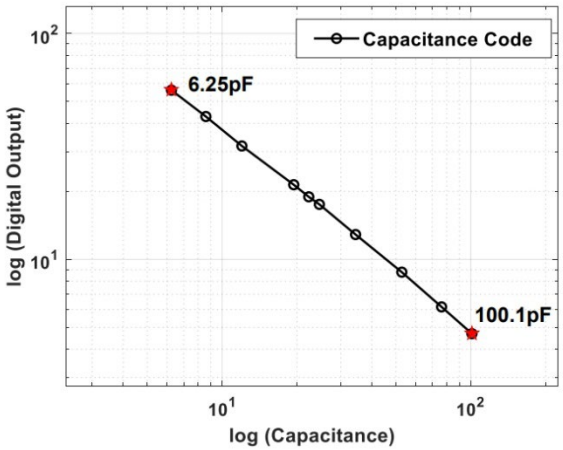


Fig. 8 Measured capacitance digital output

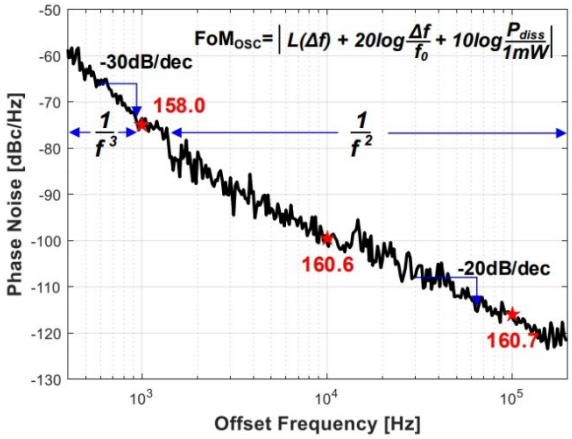


Fig. 10 Measured phase noise

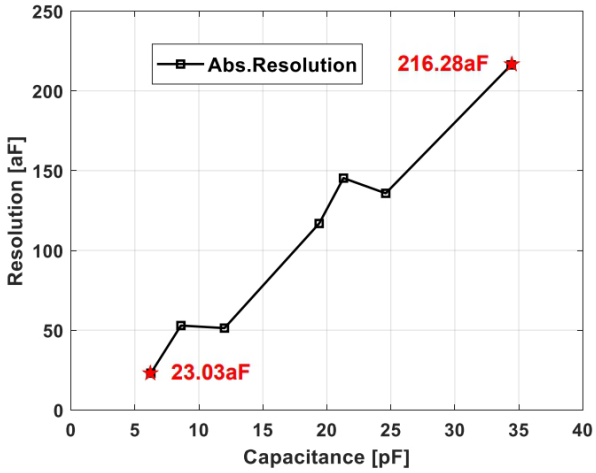


Fig. 11 Measured absolute capacitance resolution

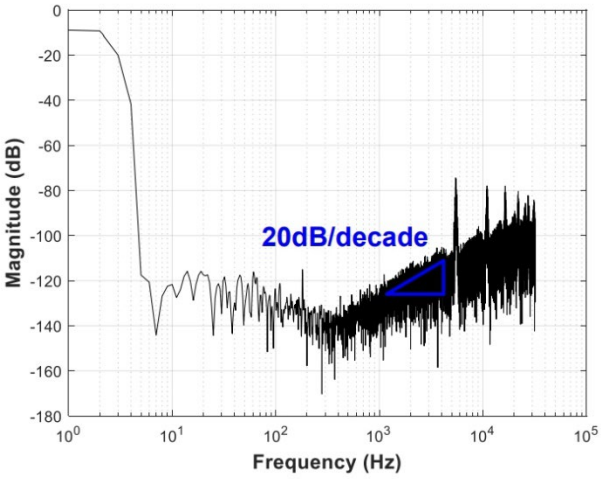


Fig. 12 Measured noise spectrum of the R^{2}CDC

V. CONCLUSION

This brief presents a leakage-tolerant, high-resolution, improved FoM, reconfigurable RC-to-digital converter. Multi-sensor readout is possible by effectively reducing leakage current for off-sensing branches, and area-saving is also achieved. Furthermore, it is suitable for reconfigurable sensing based on high-resolution by employing swing-boosted period modulation front-end and first-order noise shaping block. Based on improved performance and to sense multiple R or C sensors, the proposed R^{2}CDC is suitable for reconfigurable sensing and emerging IoT applications.

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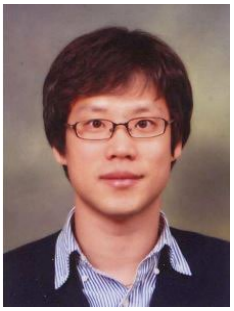

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