A Millimeter-wave Up-converter for 28-GHz 5G Mobile Systems in 65-nm CMOS Technology

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***Abstract* – 5G dual-conversion transmitter has an issue that the frequency of local-oscillator second-harmonic signal is placed near that of the desired RF output signal. A millimeter-wave up-conversion mixer utilizing an on-chip transformer with capacitance compensation at the output stage of the up-conversion mixer is proposed for 28 GHz 5G dual-conversion transmitter in order to suppress local-oscillator second-harmonic signal at the output of the up-conversion mixer. An IF amplifier and an up-conversion mixer with local-oscillator buffer was implemented in a 65-nm CMOS process. It consumes a power of 32 mW from a 1-V supply voltage. It provides a gain greater than 19.5 dB, a third-order output intercept point higher than 3.7 dBm, and a local-oscillator second-harmonic leakage signal less than -44 dBm in the frequency ranges from 26.5 GHz to 29.5 GHz.**

***Keywords*—28 GHz. 5G, CMOS, Millimeter-wave, Up-converter**

I. INTRODUCTION

As data traffic is increasing explosively due to the proliferation of smart devices and the activation of the internet of things (IoTs), millimeter-wave (mmWave) 5G technology is attracting attention. 5G has been designed to deliver higher multi-Gbps peak data speeds, ultra-low latency, and more reliability [1]. In addition, 5G technology that can process large amounts of data in real time without delay is essential for the realization of autonomous vehicles, smart cities, and smart factories, etc.

The 28-GHz band is 5G mmWave band in South Korea [2]-[5]. Since the mmWave band signal is greatly attenuated in air, beamforming is required to obtain a large array gain [6]-[7]. 5G transceivers that support mmWave beamforming in mobile phones can be implemented using a dual-conversion single-quadrature. 5G dual-conversion single-quadrature transmitter up-converts the quadrature baseband signal to the same intermediate frequency (IF) signal with frequency f_{IF} as the local-oscillator (LO) signal using the quadrature LO signal with frequency f_{LO1}, and then converts it the radio frequency (RF) signal with $f_{IF} + f_{LO2}$ by the up-conversion mixer using another LO frequency with f_{LO2}. If the LO second-harmonic (2LO) leakage signal with the frequency $2f_{LO2}$ is placed near the desired RF signal with $f_{IF} + f_{LO2}$, it is difficult to reject the unwanted LO second-harmonic leakage signal with on-chip band-pass filter and then the LO second-harmonic leakage signal can cause the degradation of the adjacent channel power ratio (ACPR). Therefore, it is essential that the up-conversion mixer suppresses LO second-harmonic leakage signal that can meet the required ACPR performance [8]. A 28 GHz power amplifier (PA) coming after an up-converter can attenuate the power level of 2LO leakage signal by more than 10 dB. Therefore, the up-converter should achieve 2LO rejection ratio of at least 15 dBc to meet ACPR performance of more than 25 dBc in a 28 GHz 5G transmitter. Since the PA can handle an RF input signal of -25 dBm or more in our system budget, our design specification for the power of 2LO signal at the RF up-converter is lower than –40 dBm when the power of the desired RF signal is greater than –25 dBm.

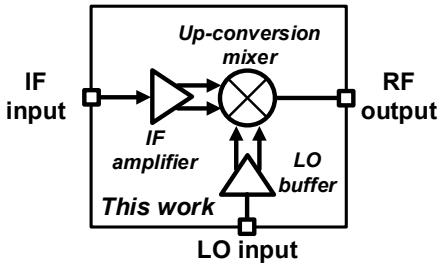

Fig. 1. Block diagram of the presented 28-GHz RF up-converter composed of an IF amplifier, up-conversion mixer, and LO buffer.

In this paper, an up-conversion mixer employing an on-chip transformer with capacitance compensation at the output stage of the up-conversion mixer is proposed for 5G dual-conversion single-quadrature transmitter. It has been implemented in a 65 nm CMOS process and has good LO second-harmonic leakage signal suppression achieving large conversion gain and high linearity.

II. CIRCUIT DESIGN

Fig. 1 presents the block diagram of the proposed 28 GHz RF up-converter composed of an IF amplifier, an up-conversion mixer, and an LO buffer. The IF amplifier is employed in the RF up-converter to achieve conversion gain of more than 20 dB. The LO buffer is adopted in order to minimize the conversion loss in the switching pair of the up-

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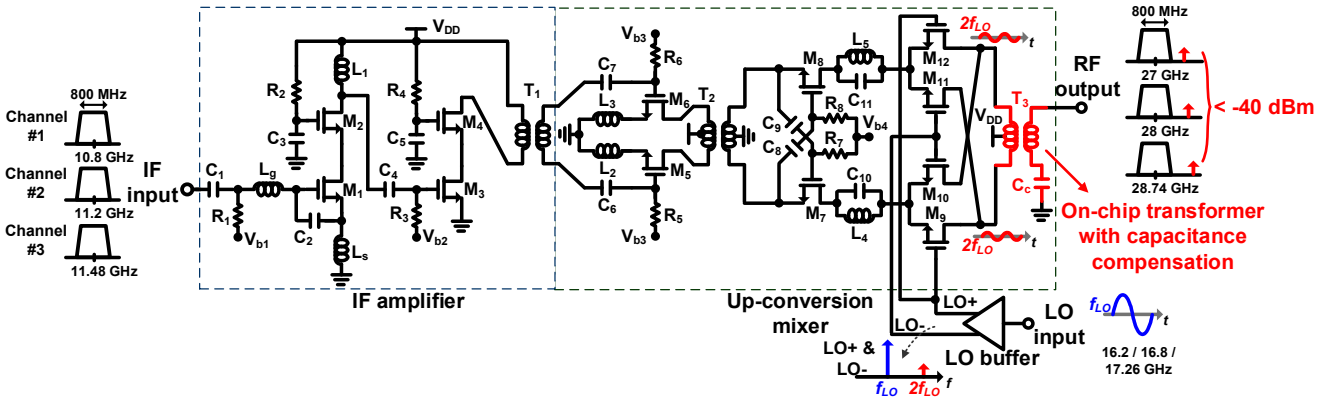


Fig. 2. Simplified schematic of the proposed up-converter utilizing an on-chip transformer with capacitance compensation at the output stage of an up-conversion mixer.

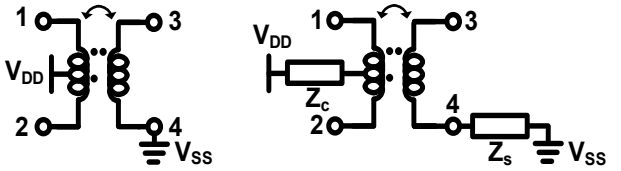
conversion mixer using the LO input signal with the input power of −10 dBm. The IF input frequencies are 10.83, 11.17, and 11.51 GHz with a 3-dB bandwidth of 800 MHz, respectively. The RF output, LO input, and IF input have single-ended 50-Ω terminations.

Fig. 2 shows the simplified schematic of the proposed up-converter that consists of an IF amplifier, an up-conversion mixer, and an LO buffer. The IF amplifier is composed of two cascode amplifiers. To cover 3-dB bandwidth of 3 GHz at the RF output of the up-converter, the center frequency with peak gain of two cascade CS amplifier is set as approximately 10.7 and 11.6 GHz, respectively. The input impedance $Z_{in}(j\omega)$ of the IF amplifier can be approximately expressed as

$$Z_{in}(\omega) \approx \frac{g_{m1}L_s}{C_2+C_{gs}} + j\omega\left(L_g+L_s\right) + \frac{1}{j\omega\left(C_2+C_{gs}\right)} + \frac{1}{j\omega C_1} \quad (1)$$

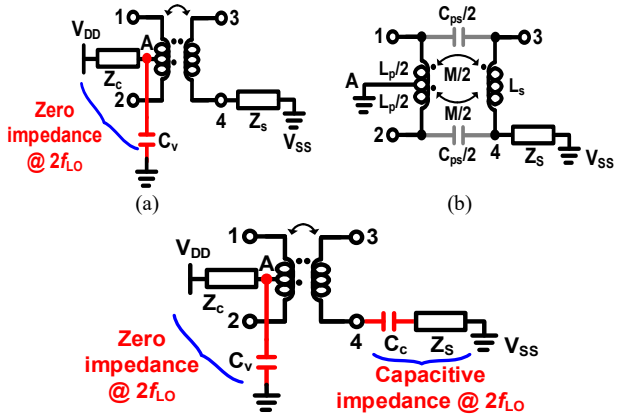
where g_{m1} and C_{gs} are the transconductance and the gate-to-source capacitance of transistor M_1, C_1 is the ac-coupling metal-insulator-metal (MIM) capacitance, and C_2 is the MIM capacitance to alleviate the input matching condition, respectively [9]. In order to meet 50-Ω input impedance matching at the IF operating frequency, the design parameters of (1) are set so that the value of $Z_{in}(\omega)$ becomes 50-Ω.

As shown in Fig. 2, the up-conversion mixer consists of a one-stage pseudo-differential amplifier with on-chip transformer T_2 and a Gilbert double balanced mixer with a capacitor cross-coupled common-gate (CG) input stage that can reduce the power consumption and improve the noise figure retaining the advantages of the conventional CG input stage [10]. The center frequency with peak gain of the one-stage CS amplifier is set as approximately 11.2 GHz. The output voltage signal of the IF amplifier is converted to the single-ended current signal by the transistor M_5 and M_6 of the up-conversion mixer. The on-chip transformer T_2 converts the differential current signal to differential current signal delivers it to the capacitor cross-coupled CG input stage of the following Gilbert double balanced mixer. Switching loss and linearity of the up-conversion mixer depends on the amplitude of LO signal. In typical, large LO driving signal is required in mmWave up-conversion mixer



(a) (b)

Fig. 3. (a) Ideal on-chip transformer, (b) practical on-chip transformer considering inductive impedances by routing lines.



(a) (b) (c)

Fig. 4. (a) An on-chip balun transformer with an approximately zero impedance of the center-tap at $2f_{LO}$ frequency using capacitance, (b) simplified equivalent circuit of Fig. 4(a) for CMRR analysis at $2f_{LO}$ frequency [8], (c) complete proposed on-chip balun transformer with capacitance compensation for CMRR improvement. L_p and L_s represent the self-inductances of the primary and secondary windings, respectively, M is the mutual inductance, and C_{ps} is the parasitic capacitance between the primary and secondary windings [8].

to reduce switching loss and obtain high linearity [8]. Because the amplitude of LO signal from LO generation circuit is not sufficiently large, an LO buffer composed of two-stage CS amplifier is used to drive the switching pair of the up-conversion mixer. However, since the switching pair in the mmWave band does not operate ideally, there is a transition region in which the switching operation is on-off. In this region, the switching pair operates as a differential pair having an amplification function [11]. Therefore, the LO signal and its harmonic components can appear at the output of the up-conversion mixer by the switching pair of the up-conversion mixer. The LO fundamental signal and other LO harmonics signals having a frequency separated from the

frequency of the RF output signal can be attenuated at the output of the up-conversion mixer due to the balancing characteristic of the double-balanced Gilbert mixer and output load with the bandpass characteristic of the up-conversion mixer. In the case that the frequency of LO second-harmonic signal in a dual-conversion single-quadrature transmitter is close to that of the desired RF output signal, it is difficult to reduce the power level of LO second-harmonic signal. However, because the LO second-harmonic signal is a common-mode signal, the LO second-harmonic signal can be attenuated by utilizing a balun transformer with high common-mode rejection ratio (CMRR) at $2f_{LO}$ frequency, which is shown in Fig. 3(a), at the output load of the up-conversion mixer.

However, it is difficult for a practical on-chip transformer shown in Fig. 3(b) to achieve high CMRR due to parasitic capacitive coupling between primary winding and secondary winding of the on-chip transformer and parasitic inductive impedances by routing lines at mmWave frequency band [8][12]. As shown in Fig. 4(a), a capacitance C_v is added at the center tap named A node through electromagnetic (EM) simulation, resulting in an impedance of near zero from node A to ac ground at a frequency of $2f_{LO}$. Fig. 4(b) shows the simplified equivalent circuit of Fig. 4(a) for CMRR evaluation. Equation (2) was derived in [8] to maximize the CMRR of Fig. 4(b).

$$Z_s = -j\omega \frac{\omega^2 \frac{L_p}{2}\frac{C_{ps}}{2}\left(\frac{L_pL_s - M}{2}\right) + \frac{L_pL_s}{2}}{L_p\left\{\omega^2 \frac{C_{ps}}{2}\left(\frac{L_p + L_s - 2M}{2}\right) - 1\right\}} \quad (2)$$

Because Z_s is the inductive impedance by routing line from fourth terminal of the on-chip transformer to ground, the condition of (2) cannot be satisfied at $2f_{LO}$ frequency. Therefore, as shown in Fig. 4(c), a capacitor is connected at fourth terminal to meet the condition of (2) through EM simulation so that the impedance from fourth terminal of the on-chip transformer to ground can have capacitive impedance effectively.

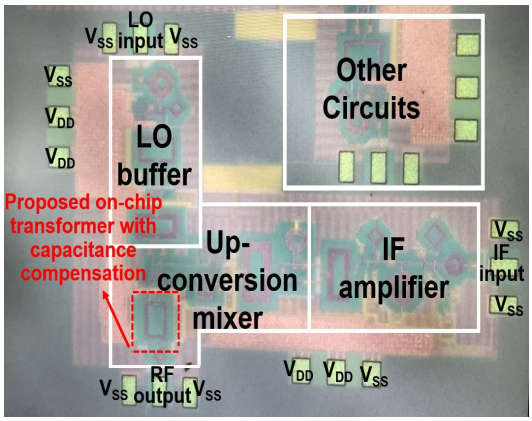


Fig. 5. Chip microphotograph of the proposed RF up-converter.

III. EXPERIMENTAL RESULTS

The RF up-converter, which employs the proposed on-chip transformer with capacitance compensation for attenuating LO second-harmonic leakage signal, consisting of an IF amplifier, an up-conversion mixer, and an LO buffer was implemented in a 65nm CMOS process. Fig. 5 shows the chip microphotograph of the proposed RF up-converter. The effective silicon area of the IF amplifier, up-conversion mixer, and LO buffer excluding PADs is approximately 0.52 mm^2, 0.74 mm^2, and 0.39 mm^2, respectively. The RF up-converter was measured by on-wafer probing after attaching the chip to an external printed circuit board. The total power consumption of the RF up-converter is 32 mW from a 1-V supply voltage. For the measurement, −8 dBm of LO power was applied to the LO input of the LO buffer.

Fig. 6 presents the measured $|S_{11}|$ at the IF input, LO input, and RF output of the RF up-converter, respectively. All measured $|S_{11}|$ at the IF input, LO input, and RF output are below −10 dB.

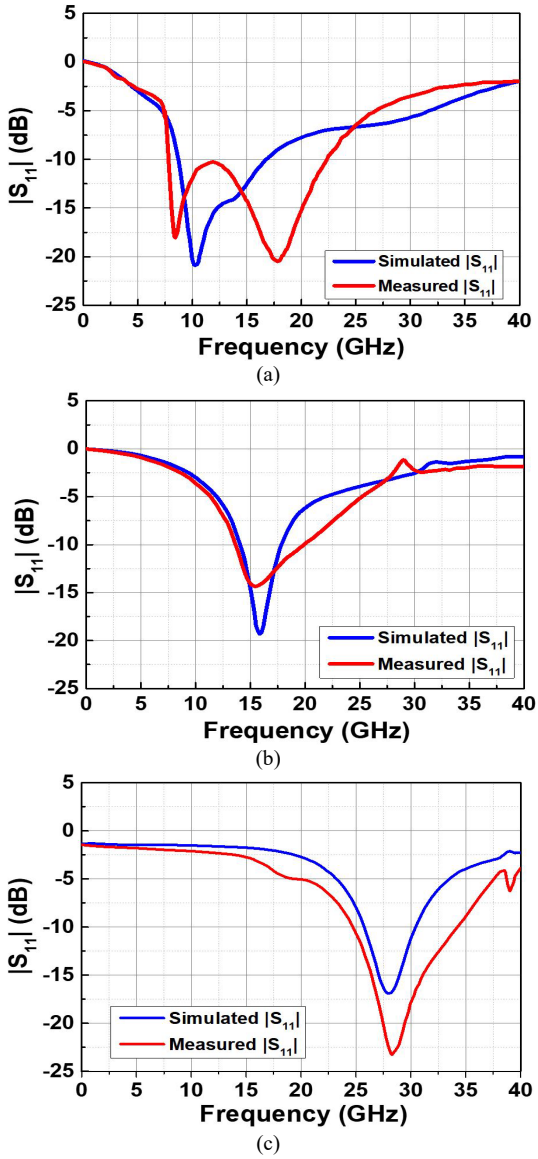


Fig. 6. Measured $|S_{11}|$ at (a) IF input port, (b) LO input port, and (c) RF output port.

TABLE I. Measurement Summary and Comparison of Performance

	[13]	[14]	[15]	This work
Operating frequency (GHz)	22-44	23.4-29.2	17-29	26.5-29.5
Conversion gain (dB)	6-10.5	–1.9	–6.4	> 19.6
OIP3 (dBm)	N.A.	N.A.	10.2	> 3.7
$OP_{1\text{-}dB}$ (dBm)	-11.5	0.3	–2.2	–4.7
Power consumption (P_{DC}) (mW)	225 (IF amplifier + Mixer + RF pre-amplifier)	39.3/22.8* (Mixer + LO buffer)	19 (Only mixer)	32/27* (IF amplifier + Mixer + LO buffer)
LO power (dBm)	11	0	2	–8
2LO leakage (dBm)	N.A.	N.A.	N.A.	< –44.21
Technology	150 nm GaAs pHEMT	130 nm CMOS	28 nm CMOS	65 nm CMOS
Area	1.09 mm^2	0.86 mm^2	0.48 mm^2	1.65 mm^2
FoM[b] [16]	–9.1 @ 31 GHz	–2.94/–0.58* @ 24 GHz	–4.42 @ 28 GHz	7.27/8* @ 28 GHz

N.A.: Not Available, *Value excluding LO buffer, [a] $OP_{1\text{-}dB} \approx OIP3 - 10$ dB,

[b] $$FoM(dB) = 10\log\left[\left(10^{\frac{Gain}{20}} \times 10^{\frac{OP_{1\text{-}dB}}{20}}\right)\left(f_o/1\text{GHz}\right)\Big/\left(P_{DC}/1\text{mW}\right)\right]$$

As shown in Fig. 7, the measured conversion gain of the proposed RF up-converter is larger than 19.5 dB over entire RF operating frequencies. The measured output-referred third-order intermodulation point (OIP3) is more than 3.7 dBm from 26.5 to 29.5 GHz band.

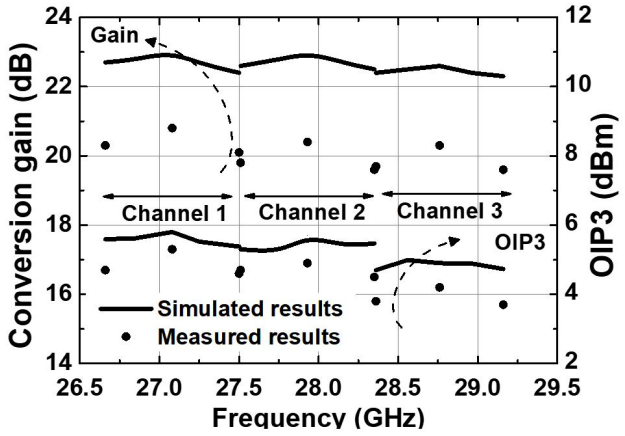


Fig. 7. Measured conversion gain and OIP3 versus RF output operating frequencies

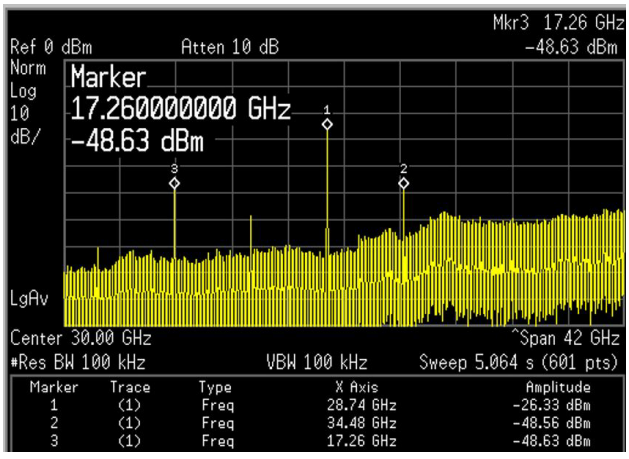


Fig. 8. Measured RF output spectrum of the proposed RF up-converter. IF Input power was set to -45 dBm and total loss by cables and probe tips is approximately 1.6 dB.

Fig. 8 presents the RF output spectrum of the proposed RF up-converter when IF input frequency is 11.48 GHz, LO input frequency is 17.26 GHz, and IF input power is set to –45 dBm. Considering the total loss due to cables and probe tips in the measurement, the power of 2LO leakage signal at the RF output of the RF up-converter is approximately –47 dBm. Fig. 9 shows the measured power of 2LO signal at the output of the proposed RF up-converter.

Table I summarizes and compares the measured results of the proposed up-converter with those of other published mmWave up-converter [13]-[15]. The proposed up-converter mixer shows higher figure of merit (FOM) compared to the previous mmWave up-conversion mixers showing good 2LO leakage signal rejection.

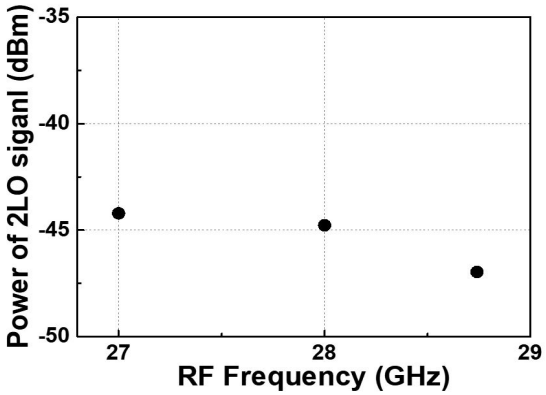


Fig. 9. Measured power levels of 2LO leakage signal of the proposed RF up-converter at the RF output.

IV. CONCLUSION

A 28-GHz up-converter composed of an IF amplifier, a LO buffer, and an up-conversion mixer was implemented and proposed for 5G mmWave mobile applications. The proposed up-converter shows excellent FOM with 2LO leakage signal rejection. Therefore, the RF up-converter could be employed to 5G mmWave cellular phones.

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REFERENCES

[1] https://qualcomm.com/5g/what-is-5g.

[2] W. Roh, J.-Y. Seol, J.-H. Park, B. Lee, J. Lee, Y. Kim, J. Cho, and K. Cheun, "Millimeter-wave beamforming as an enabling technology for 5G cellular communications: Theoretical feasibility and prototype results," *IEEE Communications Mag*azine, vol. 52, no. 2, pp. 106-113, Feb. 2014.

[3] H.-T. Kim, B.-S. Park, S.-S. Song, T.-S. Moon, S.-H. Kim, J.-M. Kim, J.-Y. Chang, and Y.-C. Ho, "A 28-GHz CMOS direct conversion transceiver with packaged 2 × 4 antenna array for 5G cellular system," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1245-1259, May 2018.

[4] C. Kim, M. Kim, Y. Jeon, O. Lee, H. H. Son, and I. Nam, "A 28-GHz CMOS Down-conversion Mixer with Low-magnetic-coupled Source Degeneration Inductors for 5G Applications," *Journal of Semiconductor Technology and Science*, vol. 19. no. 4, pp. 373-377, Aug. 2019.

[5] H. Ahn, K. Oh, I. Nam, and O. Lee, "A highly efficient and linear mm-wave CMOS power amplifier using a compact symmetrical parallel-parallel power combiner with IMD3 cancellation for 5G applications," *IEEE Access*, vol. 9, pp. 150304-150321, 2021.

[6] G.-S. Shin, J.-S. Kim, H.-M. Oh, S. Choi, C. W. Byeon. J. H. Son, J. H. Lee, and C.-Y. Kim, "Low insertion loss, compact 4-bit phase shifter in 65 nm CMOS for 5G applications," *IEEE Microw. Wireless Compon. Lett.,* vol. 26, no. 1, pp. 37-39, Jan. 2016.

[7] C. Choi, J. H. Son, O. Lee, and I. Nam, "A +12-dBm OIP3 60-GHz RF downconversion mixer with an output-matching, noise- and distortion-canceling active balun for 5G applications," *IEEE Microw. Wireless Compon. Lett*., vol. 27. no. 3, pp. 284-286, Mar. 2017.

[8] S. Lee, Y. Jeon, D.-Y. Yoon, O. Lee, D. Im, and I. Nam, "28-GHz CMOS up-conversion mixer with improved LO second-harmonic leakage signal suppression for 5G applications," *IEEE Access*, vol. 10, pp. 57003-57011, May 2022.

[9] P. Andreani and H. Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Trans. Circuits Syst. II., Analog Digit. Signal Process.,* vol. 48, no. 9, pp. 835-841, Sep. 2001.

[10] W. Zhou, X. Li, S. H. K. Embabi, J. Pineda de Gyvez, D. J. Allstot, and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 12, pp. 875-879, Dec. 2005.

[11] H. Darabi and J. Chiu, "A noise cancellation technique in active RF-CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2628-2632, Dec. 2005.

[12] D. E. Bockelman and W. R. Eisenstadt, "Combined differential and common mode scattering parameters: Theory and simulation," *IEEE Trans. Microw. Theory Techn*., vol. 43, no. 7, pp. 1530-1539, Jul. 1995.

[13] C.-C. Su, C.-H. Liu, C.-M. Lin, Y.-L. Tsai, and Y.-H. Wang, "A 24-44 GHz broadband subharmonic mixer with novel isolation-enhanced circuit*," IEEE Microw. Wireless Compon. Lett.*, vol. 25. no. 2, pp. 124-126, Feb. 2015.

[14] Y.-S. Won, C.-H. Kim, and S.-G. Lee, "A 24 GHz highly linear up-conversion mixer in CMOS 0.13 μm technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 25. no. 6, pp. 400-402, Jun. 2015.

[15] Z.-H. Wang, C.-N. Chen, T.-W. Huang, and H. Wang, "A 28-GHz high linearity up-conversion mixer using second-harmonic injection technique in 28-nm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 31. no. 3, pp. 276-279, Mar. 2021.

[16] H.-K. Chiou and H.-T. Chou, "A 0.4 V microwatt power consumption current-reused up-conversion mixer," *IEEE Microw. Wireless Compon. Lett.*, vol. 23. no. 1, pp. 40-43, Jan. 2013.

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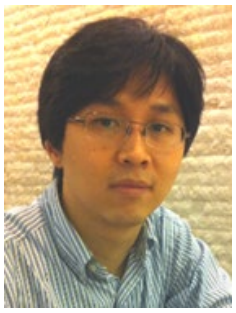

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