A 7 – 8.5 GHz LC Voltage-Controlled Oscillator with –111.7 dBc/Hz Phase Noise at 1-MHz offset for Ultra-Low-Jitter Phase-Locked Loop

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***Abstract* - This work presents an area efficiency LC voltage-controlled oscillator for an ultra-low-jitter phase-locked loop. Using a 3-turn area-compact spiral, the VCO achieve area-efficient without degrading *LC*-tank quality factor. The negative transconductance cell was NMOS type so that the start-up was done in 3ns. This work also includes a tail inductor for the noise filtering. As a result, the measured phase noise at 8 GHz was -111.7 dBc/Hz with 1 MHz offset and -134.9 dBc/Hz with 10 MHz offset. The power consumption was only 2.7 mW at 8 GHz. Also, the die area was less than 0.03 mm^2.**

***Keywords*—Area-efficient, Jitter, LC-Oscillator, Phase-Locked Loop, Tail inductor, Voltage-Controlled Oscillator (VCO)**

I. INTRODUCTION

In accordance with a soaring of the communication data rate, the design of phase-locked loop (PLL) has become very important. However, the design of PLL is extremely hard since the jitter requirements become more stringent as the communication standards evolve while satisfying the limited silicon area and power budget simultaneously. The noise of the PLL can be divided into the in-band noise and the out-of-band noise. For the PLL to have the best jitter performance, it must have optimal bandwidth, i.e. the in-band noise and the out-of-band noise are well balanced. The in-band noise is the combination of the reference clock noise and other blocks such as phase-frequency detector (PFD) and charge-pump (CP). The out-of-band noise is mostly determined by the oscillator. The PLL in [1] successfully reduced the in-band noise by removing the frequency divider. In conventional PLL, the noise of PFD and CP is amplified by 20logN (N is frequency division number). However, in sub-sampling PLL (SSPLL), due to sub-sampling phase detector (SSPD), frequency divider can be eliminated, so the noise of PFD and CP is not amplified by 20logN. Thereby the in-band noise is solely determined by the reference clock. The reference clock is fixed upon the application of the PLL, so the reference clock noise is not controllable. For the PLLs with extremely low in-band noise such as SSPLLs, the design efforts to improve jitter performance is focused on the oscillator.

Recently, many ring oscillator (RO) PLLs are introduced [2], [3] since RO has compact area and high compliance with process scaling. However, due to the mechanism of the oscillation, i.e., time delay of the delay cell, the achievable max frequency, f_{MAX} is far lower than that of *LC*-Voltage-Controlled Oscillator (*LC*-VCO). Moreover, due to the mechanism, the phase noise is far inferior than that of *LC*-VCO. By extending the loop bandwidth of the PLL, the RO phase noise can be suppressed. But, excessively extended bandwidth can easily exceed loop stability limit, which is 1/10 of the reference frequency [4]. Conventional *LC*-VCO based PLL [5] shows superior jitter performance even below 100-fs$_{rms}$. However, the use of area-hungry inductor increases the chip cost and the area of the inductors generally does not follow the process scaling trend (inductance is determined by physical dimension).

In this work, we propose an area-efficient *LC*-VCO with compact tail inductor for ultra-low-jitter PLL. The inductors in this work are carefully designed to save the silicon area. Section II provides design details of the *LC*-VCO including inductors, capacitor bank, negative transconductance cell. Section III describes the simulation results and measurement results of *LC*-VCO and conclusions in Section V.

II. DESIGN OF AREA-EFFICIENT LC-VCO

A. Main Inductor

The main inductor occupies the largest silicon area in *LC*-VCO. Minimizing the inductor size is the most effective in reducing overall area. However, when the inductor is manipulated, the inductance and quality factor also changed, which is strongly related to the target requirements, such as oscillation frequency, frequency tuning range and phase noise. Therefore, inductor design has very few degrees of freedom. The turns of the inductor are the major factor that affecting the size, the inductance, and the quality factor. As the number of the turns of the inductor increases, the inductance per unit area increase, i.e., the inductor size is minimized. But, the quality factor is inversely proportional to the turns because of the parasitic capacitors between inner circle and outer circle which diminish self-resonance

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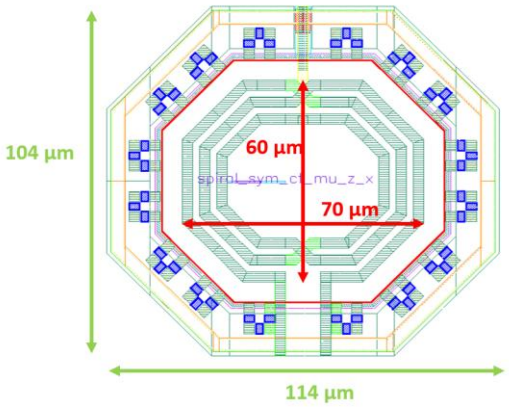
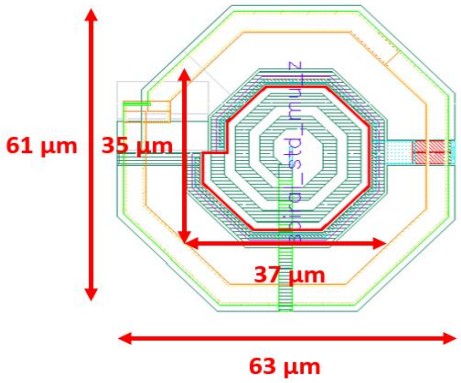
frequency (SRF) of the inductor and also exacerbate the phase noise and start-up margin. This work, three turns spiral inductor was used as shown in Fig. 1(a). The area of this inductor is 104 μm x 114 μm.



(a)



(b)

Fig. 1. Layout of (a) three turns spiral inductor with center tap; (b) noise filtering tail inductor

Fig. 2 shows plot of inductance according to the frequency. At 8 GHz, which is the target oscillation frequency, the inductance was 557 pH. Fig. 3 shows plot of quality factor according to the frequency. The quality factor was 16.5 at 8 GHz which is enough number for the low phase noise performance. Self-resonance frequency is near 25 GHz, so, it does not affect the operation near 8 GHz.

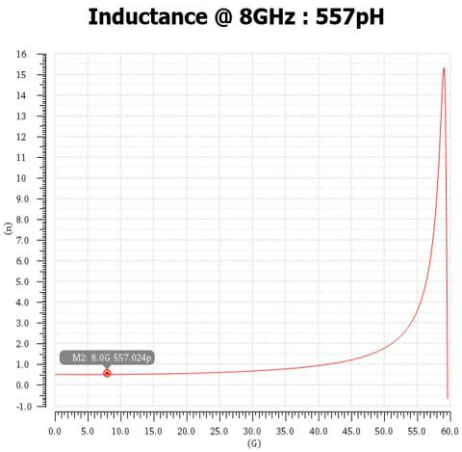


Fig. 2. Plot of inductance vs. frequency

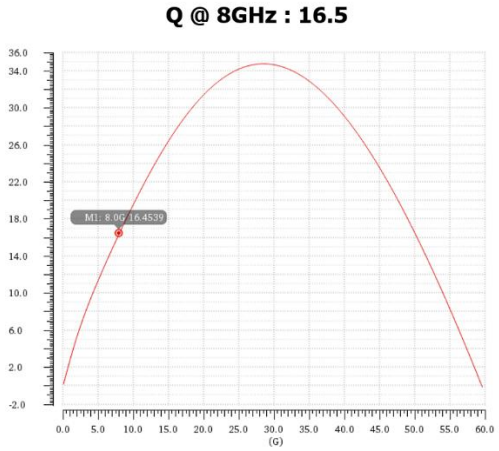


Fig. 3. Plot of Q-factor vs. frequency

B. Capacitor Bank & Varactor

Capacitor bank was designed based on the switched capacitor as shown in Fig. 4. Capacitor bank is binary weighted for the area-efficient design. Capacitance is doubled as the bit number increases. Resistance is inversely proportional to the capacitance to keep the high frequency-sweep linearity. Total 7-bit binary capacitor array is designed with 9 fF of unit capacitor. Varactor was designed to cover frequency range about 1.5 MHz as shown in Fig. 5.

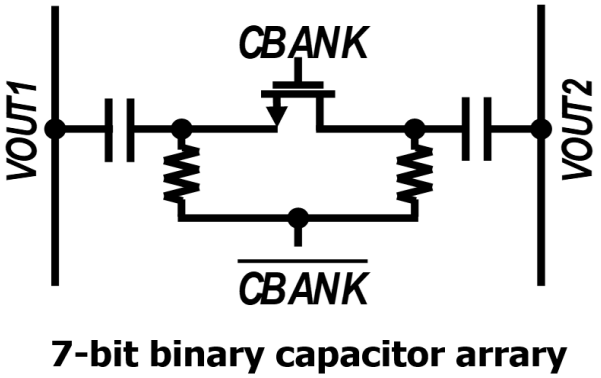


Fig. 4. Schematics of switched capacitor-based capacitor bank

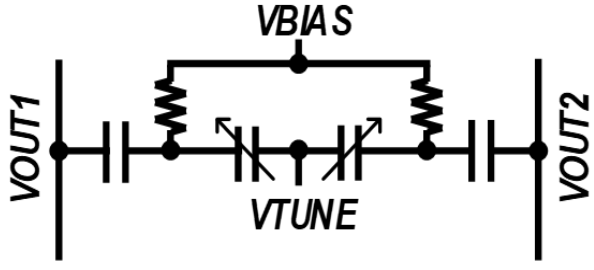


Fig. 5. Schematics of varactor.

C. Negative transconductance cell

Design of negative transconductance cell is crucial part of the VCO design. NMOS-type cell is adopted due to high transconductance, i.e., sufficient start-up margin.

$$g_m > \frac{2}{R_P} \quad (1)$$

Start-up condition of oscillator is expressed in equation (1) where g_m is the transconductance, and R_P is parallel resistance of the LC tank. The measured R_P of the LC tank this work was 155 ohm. For the 2.5 times of start-up margin, we set g_m to be 32 mS.

Fig. 6 shows that the oscillation starts within 3ns. So, start-up condition is well secured and margin is enough for the reliable operation.

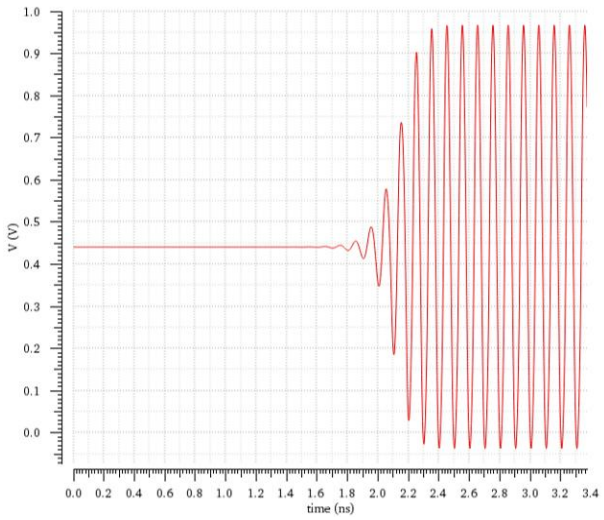


Fig. 6. Start-up transient simulation of the LC VCO.

D. Tail inductor

LC-VCO of this work includes noise filtering tail inductor as proposed in [6]. The principle of tail filtering is as follows. At first, only thermal noise in the current-source transistor around the second harmonic of the oscillation causes phase noise. Second, a high impedance at the tail is only required at the second harmonic to stop the differential- pair FETs in triode from loading the resonator.

The noise filtering tail inductor this work occupies only 61 μm x 63 μm due to high turns. In tail inductor, low quality factor can guarantee broad band filtering thereby can guarantee reliable operation.

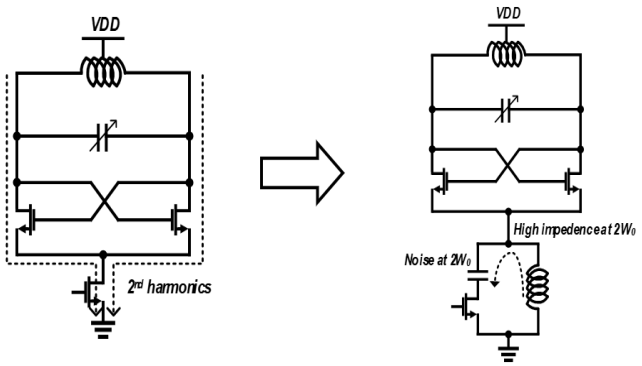


Fig. 7. Mechanism of noise filtering tail inductor

D. Overall schematics of LC-VCO

Fig. 8 shows the overall schematics of the LC-VCO. To secure reliable start-up, NMOS type negative transconductance cell is used. For the frequency tuning range, 7-bit of binary weighted capacitor bank is used. Two varactor sets are implemented for proportional-path and integral-path respectively. Also, tail inductor is used for the noise filtering with 5-bit of switched capacitor bank for wide band noise filtering. In this work, the bias of the VCO is set by the cross-coupled pair.

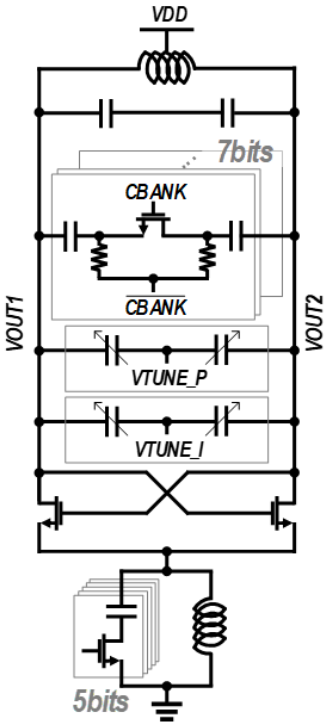


Fig. 8. Schematics of *LC*-VCO

III. RESULTS AND DISCUSSIONS

Fig. 9 shows post layout simulation of phase noise when frequency was 8 GHz. The phase noise is -116.6 dBc/Hz at 1MHz offset, and -137.5 dBc/Hz at 10MHz. The flicker noise corner was about only 10 to 20 kHz due to noise filtering tail inductor. Fig. 10 also shows the phase noise simulation when frequency was 7.2 GHz. The VCO also shows excellent phase noise performance and very small flicker noise corner about 8 kHz. Fig. 11 and Fig. 12 shows measured phase noise at 8 GHz and 7.2 GHz respectively. In thermal noise dominant region, i.e. frequency offset over 10MHz, the phase noise levels were close to the simulation results. However, measured flicker noise corner is approximately ten times larger than the simulated flicker noise corner. So that, the phase noises at 1 MHz offset are -111.7 dBc/Hz at 8 GHz and -113.8 dBc/Hz at 7.2 GHz. That is because of the parasitic. The parasitic capacitor or inductor inevitably change the harmonic tuning of the tail inductor. So, the noise filtering effect is diminished in the measured results. Fig. 13 shows the die micrograph of the LC-VCO.

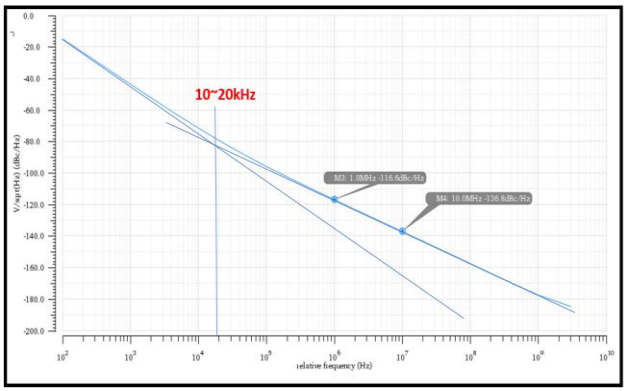


Fig. 9. Post layout phase noise simulation at 8GHz

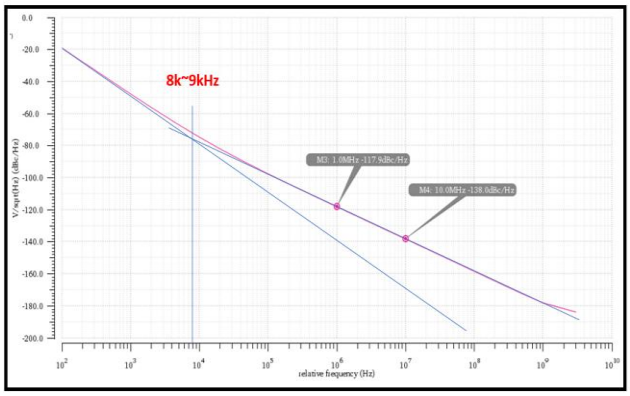


Fig. 10. Post layout phase noise simulation at 7.2GHz

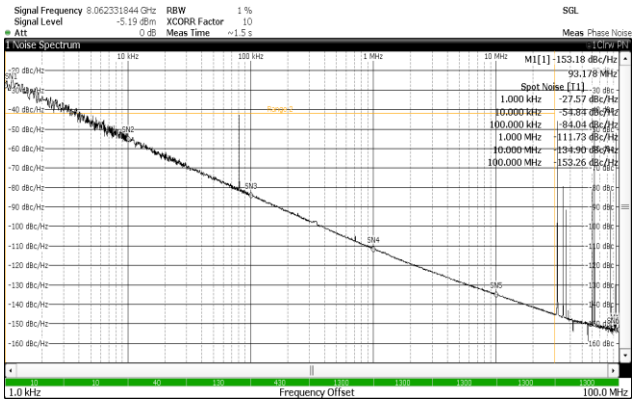


Fig. 11. Measured phase noise at 8GHz

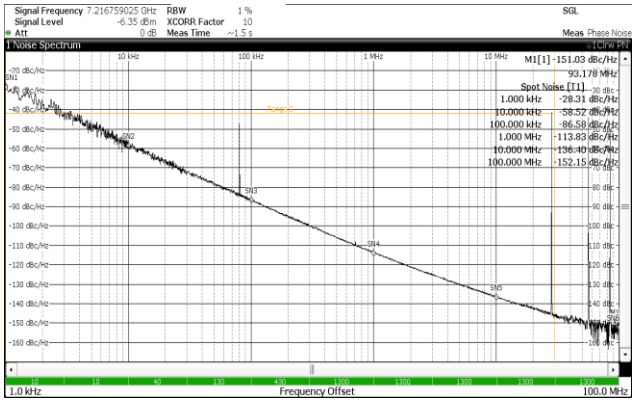


Fig. 12. Measured phase noise at 7.2GHz

IV. CONCLUSION

In this work, an area-efficient LC-VCO was designed. The main inductor was 3-truns spiral inductor which does not degrade the tank quality factor significantly with compact area dimension. The negative transconductance cell was implemented in NMOS type to secure reliable oscillation so that, the start-up was done in 3 ns in post layout transient simulation. For the frequency tuning, capacitor bank and varactor were used. Capacitor bank was based on binary-weighted switched capacitor. Total 7-bit was used for wide band tuning. To improve phase noise performance, especially to minimize the flicker noise up conversion, noise filtering tail inductor was also used. The measured phase noise at 8GHz was -111.7 dBc/Hz with 1 MHz offset and -134.9 dBc/Hz with 10 MHz offset. The power consumption was only 2.7 mW at 8 GHz. Also, the die area was less than 0.03 mm^2.

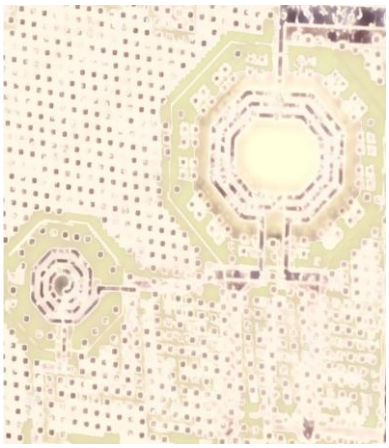


Fig. 13. Die micrograph.

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