Miniaturized Plasmon Detector using 0.25 μm CMOS Process for Large-Scale Sub-Terahertz Imaging

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Abstract **- A miniaturized complementary metal-oxide-semiconductor (CMOS) detector circuit is presented for large-scale 0.2 THz imaging. The proposed detector consists of an integrated differential antenna, common-source (CS) Plasmon detector cores, a buffer stage including pre-amplifiers, and off-chip main amplifiers. The folded dipole structure is used for reducing the unit size of the detector area and supplying the gate bias of the differential CS detector cores. The converted DC outputs at the detector are combined in the drain of the preamplifier as currents and transmitted to the output of the buffer. The off-chip main amplifier, implemented using discrete components, provides a high voltage gain for increasing responsivity and band-pass frequency response for optimizing the electrical modulation in the source. The proposed detector, except for the main amplifiers, is implemented in the area of 500 μm × 370 μm by using 0.25 μm CMOS technology. The responsivity and noise equivalent power of the proposed detector circuit, including the amplifiers, at 0.2 THz were measured to be 2.57 MV/W and 43.61 pW/√Hz, respectively.**

Keywords**—CMOS detector, Folded dipole antenna, Hybrid circuit, Sub-terahertz imaging**

I. INTRODUCTION

The large-scaled sub-terahertz imaging is promising in the non-destructive and real-time inspection in the applications to detect foreign bodies in food, non-metallic weapons for security, and voids in manufactured things [1–4]. The detectors based on conventional compound semiconductors have more high sensitivity and wide dynamic range compared to complementary metal-oxide-semiconductor (CMOS).

A plasmon detector has been presented as an attractive technology for large-scale sub-terahertz imaging. The plasmon detector provides the DC output signal from detecting sub-terahertz signals, which are at a higher frequency than the operating frequency of the device, with the fabricated detector using a low-cost CMOS technology [5−7]. However, the plasmon detector cannot be used in the industry due to its low voltage responsivity (R_V) and high noise-equivalent power (*NEP*). Recent research has shown that the CMOS plasmon detector can show the commercially available level of detection characteristics for non-destructive sub-terahertz imaging by using performance optimization with the circuit design, based on the device modeling including the operating principle [8,9]. In particular, the source modulation technique was presented to avoid the high 1/f noise characteristics included in the DC output by moving the DC output signal to the signal at the modulation frequency [10]. The technique is useful to increase the quality of the sub-terahertz imaging, and the main amplifier with a high quality-factor and a high voltage gain at the modulation frequency is necessary to improve the effectiveness of the usage of the technique. The size minimization of the detector unit is required for implementing large-scale imaging, and its size occupies most of the antenna size, which is determined by the operating frequency. A patch antenna has been conventionally used in the detector array for sub-terahertz imaging because of its straightforward design and high antenna gain [11,12]. However, the detector using the patch antenna has a limit to increasing the number of arrays owing to the large implementation area of the antenna. It is also difficult to realize the metal density of backend oxide layers per unit area required in the fabrication process for mass production. Therefore, the size reduction of the detector by changing the antenna structure as well as the improvement of the detecting performances by using the main amplifier should be simultaneously achieved for the implementation of large-scale sub-terahertz imaging.

In this paper, a CMOS plasmon detector module with an off-chip main amplifier is proposed for a large-scale sub-terahertz imaging system. The size of the detector integrated circuit (IC) is minimized by using the folded dipole antenna, which is also used for supplying the gate bias voltage of the detector cores by using the virtual ground node. The differential common-source detector cores with additional gate-drain capacitors and the buffer stage including the pre-amplifier are employed to improve the detection characteristics. The detector IC in the module for 0.2 THz imaging is fabricated by 0.25 μm CMOS process with 1-poly and 5-metal layers, which has a cut-off frequency of 10 GHz or less. The main amplifier implemented on an FR4 printed circuit board (PCB) is based on the multiple feedback structure providing high voltage gain and bandpass frequency response with the center of the modulation frequency. Section II presents design methodologies of the

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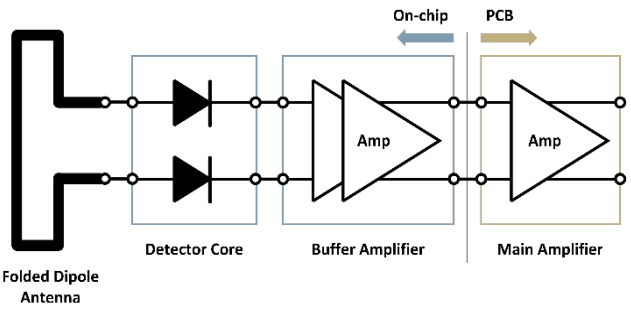

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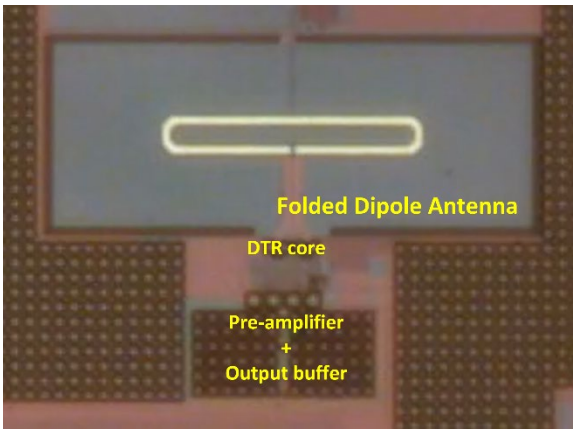


(b)

Fig. 1. Proposed plasmon detector IC; (a) Block diagram and (b) die photograph.

proposed detector IC and the off-chip main amplifier. Section III provides the experiment setup and discusses the measurement results for the detector IC, the main amplifier, and 0.2 THz imaging obtained by the detector module. The conclusion is presented in Section IV.

II. DESIGN METHODOLOGY

A. CMOS Plasmon Unit Detector IC

The mechanism of the plasmon effect in a field-effect transistor was first introduced by Dyakonov and Shur. The magnitude of high-frequency signals above the cut-off frequency of the transistor is obtained by the plasmon effect in a low-cost semiconductor process [5−7].

The proposed plasmon unit detector IC is designed at an operating frequency of 0.2 THz as shown in Fig. 1(a). The detector IC consists of a folded dipole antenna operating at 0.2 THz, detector core, pre-amplifier as transconductance stage, and voltage output buffer. The folded dipole antenna receives 0.2 THz signals, and the coupled signal is transmitted to the gate of the detector core which is designed with the smallest transistor size and the capacitor to optimize the plasmon effect. A DC voltage at the drain node of the detector core is generated by plasmon phenomena. The pre-amplifier is self-biased by the output voltage of the detector core and operates in the sub-threshold region. By tying the drain node of the pre-amplifier input transistors, each of the DC voltages is converted into current and combined. Additionally, the parasitic terahertz signals, coupled by the capacitor between the gate and drain node, are canceled due

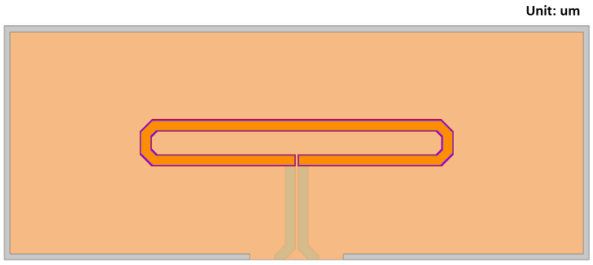
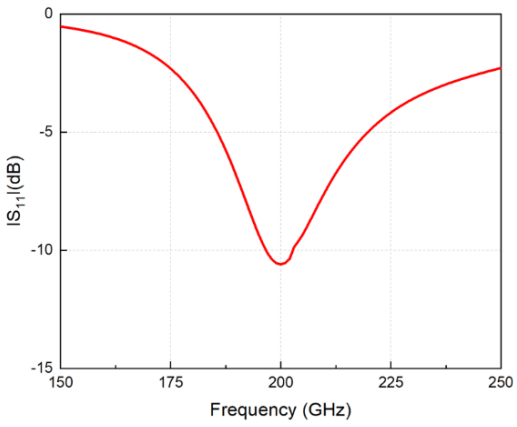


Fig. 2. Layout design of the folded dipole antenna.

to the phase of the signals at the drain node of the pre-amplifier inputs. The reference voltage is generated from the dummy cell biased to ground on the transconductance stage. The output and reference voltages of the pre-amplifier are transmitted to each of the PMOS input transistor of the voltage output buffer and amplified by the amplifier are transmitted to each of the PMOS input transistor of the voltage output buffer and amplified by the current mirror load. The source follower is designed with negative feedback for operation stability as the last stage of the voltage output buffer [13].

B. Folded Dipole Antenna

The differential antenna is a beneficial structure for reducing parasitic characteristics. The folded dipole antenna is advantageous in reducing the total size of the array and improving the characteristics of the detector by reducing the antenna area. The folded dipole antenna operating at 0.2 THz is designed by using an ANSYS HFSS 3D electromagnetic wave simulation as shown in Fig. 2. The radiated line of the antenna has a width of 10 μm of top metal which is the M5 layer with a thickness of 3 μm. The width of the feeding line is 8.8 μm implemented on the M4 layer for achieving the impedance matching at the input. The gate bias of the detector core is supplied by using the virtual ground node of the antenna for minimizing the performance degradation due to the parasitic components [14]. The antenna is shielded by stacking metal layers from M1 to M5 layers for decreasing the coupling effect of the neighboring antennas through the substrate. The total size of the antenna, including the guard ring, is 500 μm × 200 μm, and it can reduce the size of the detector by 80% or more as compared to the previous detector using the patch antenna [13]. The simulated antenna gain is to be – 2.79 dBi at 200 GHz shown in Figs. 3 and 4.



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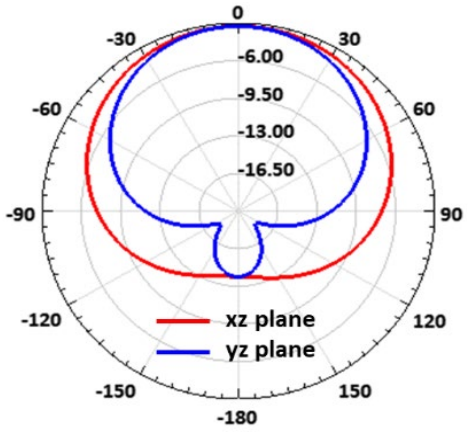

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Fig. 3. Simulation results of the folded dipole antenna; (a) $|S_{11}|$, and (b) directivity.

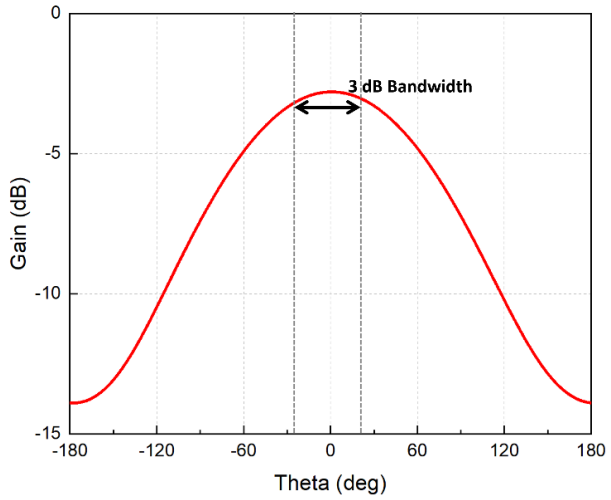


Fig. 4. Simulated antenna gains of the folded dipole antenna.

C. High-gain Amplifier

The output voltage of the detector is modulated to 200 Hz using a mechanical chopper to minimize the effect of flicker noise. A high gain amplifier for improving the characteristics of the detector is designed. The proposed amplifier uses a commercial high-speed FET-input operational amplifier (OPA4132) chip from Texas Instruments. The proposed amplifier is designed with multiple feedback band-pass filter to pass only the signal at a specified frequency. The schematic of the proposed main amplifier is as shown in Fig. 5. The center frequency (f_0) of the multiple feedback band-pass filter can be expressed as follows:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{C1 \cdot C2 \cdot R3}\left(\frac{1}{R1}+\frac{1}{R2}\right)}. \qquad (1)$$

The voltage gain (G) can be expressed as follows:
Using (1)–(2), the resistance and capacitance values of the amplifier satisfying the gain of 30 dB or more and the center

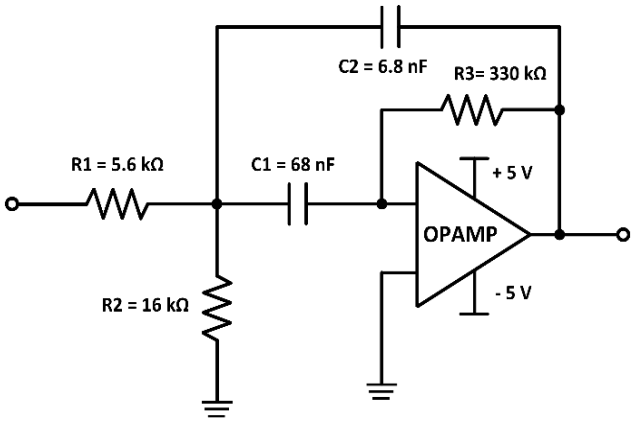
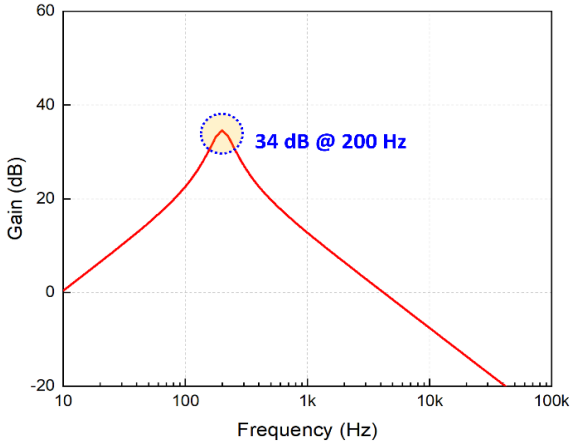


Fig. 5. Schematic of the main amplifier design using multiple feedbacks.



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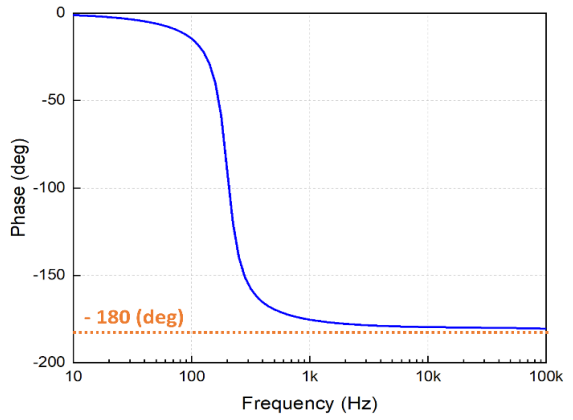

(b)

Fig. 6. Simulated AC response of the main amplifier; (a) Gain and (b) phase.

$$G = \frac{R3}{R1} \cdot \frac{-C2}{C1 + C2} \qquad (2)$$

frequency of 200 Hz was obtained. The simulation results in Fig. 6 depict the gain and phase of the main amplifier depending on the frequency. The maximum voltage gain and the phase margin of the amplifier were simulated to 34 dB at 200 Hz and 1.05° at the unity gain frequency of 4.16 kHz. The main amplifier is implemented on a PCB as shown in Fig. 7.

III. RESULTS AND DISCUSSIONS

A. Experiment *Setup for Unit Detector*

Fig. 8 shows the experiment setup for obtaining the R_V and *NEP* of the proposed detector. The signal generator (Keysight N5182B) is used for generating the 16.67 GHz signal. The generated signal is extended to 0.2 THz using a frequency multiplier (VDI WR5.1SGX). The 0.2 THz signal is radiated by a horn antenna with a gain of 25 dBi and electrically modulated to 200 Hz by a function generator (GW Instek AFG-2226). The incident power on the detector, which is required for the calculation of the voltage responsivity, is measured by a signal analyzer (Keysight N9030B) equipped with a frequency extension module (VDI WR5.1SAX). The power is obtained by calculating the data measured at the position where the detector is placed by compensating for the gain of the reference horn antenna. The output of the detector is analyzed by using an oscilloscope (Keysight DSO-9204H). The data acquisition board (DAQ)

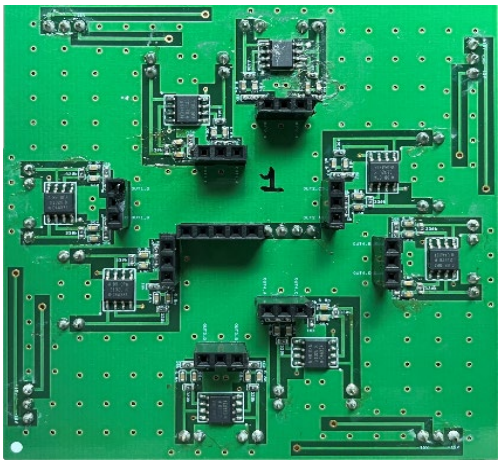

Fig. 7. Fabricated main amplifiers implemented on FR4 PCB.

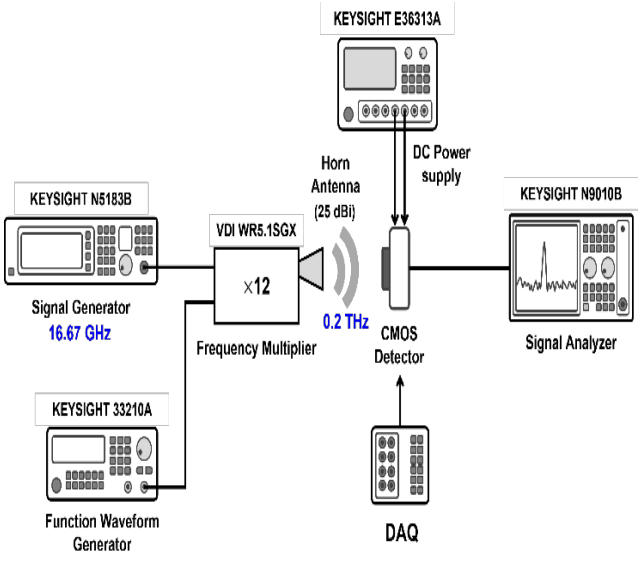

Fig. 8. Experiment setup for measuring the performances of the detector module.

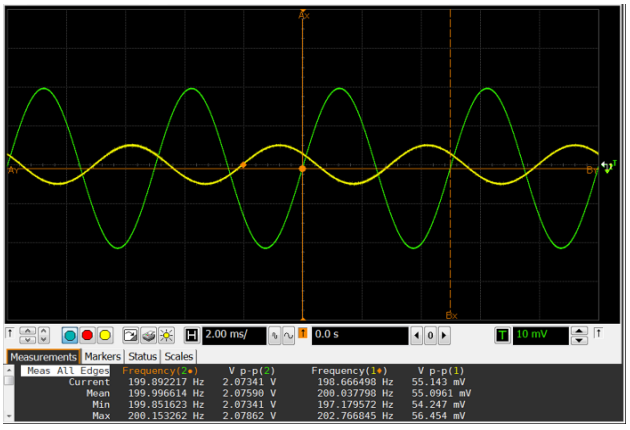

Fig. 9. Measured input and output waveforms when the signal of 200 Hz is inputted to the main amplifiers.

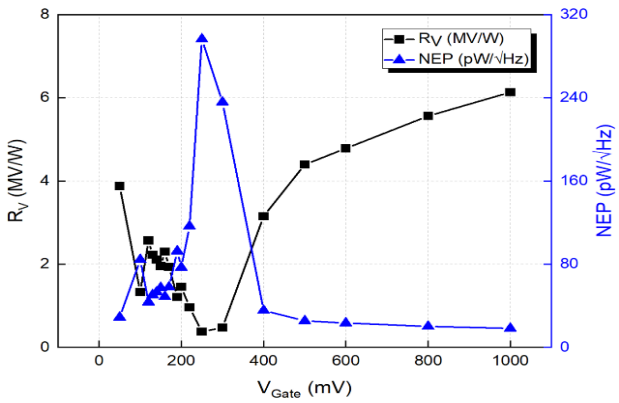

Fig. 10. Measured input and output waveforms at 200 Hz of the main amplifiers.

manufactured by National Instruments Inc. is used to adjust the bias voltage of the integrated low drop-out regulator. The signal analyzer is also used to obtain the noise spectral density for calculating the *NEP*.

B. Measurement Results of the proposed Unit Detector

Before measuring the detector module, the performance of the main amplifier was measured with the incident sine wave of 200 Hz frequency. Fig. 9 shows the measurement results of the implemented main amplifier only using the oscilloscope. The ratio of the input and output signal of the measurement results shows that the amplifier has a high gain of about 30 dB.

The R_V is obtained by calculating the ratio of the output voltage of the detector and the product of the incident power density and effective antenna area. The *NEP* is defined as dividing R_V by the square root of the noise spectral density. The effective antenna area is obtained to be 9.4×10^{-8} m^2 by using the integrated folded dipole antenna. Considering the transmitted power of the signal generator and gain of the horn antenna at the distance of 20 mm, the power density of the 0.2 THz incident signals on the folded dipole antenna is calculated to be 98.5 μW/m^2. The R_V and *NEP* of the proposed unit detector IC are shown in Fig. 10. The maximum value of R_V and *NEP* are measured to be 2.57 MV/W and 43.61 pW/√Hz at the gate bias of 0.12 V.

C. Measurement setup for 0.2 THz Imaging

The measurement setup for obtaining 0.2 THz imaging using the proposed unit detector IC is shown in Fig.11. The 0.2 THz signal is generated by the gyrotron and converted into a uniform line beam by off-axis parabolic (OAP) mirrors [15]. A mechanical chopper operating at 200 Hz is used to reduce the effects of DC noise and 1/f noise and positioned at 152 mm, which is the focal length of the OAP mirror [10]. The distance between the OPA and the sample is 440 mm, and the distance from the sample to the detector is 20 mm. The sample is moved at 1 mm intervals using 2D moving stage, and the obtaining time of data is set to 1 s. The output voltage for each position of the sample is acquired using the analog signal terminal of the NI-DAQ. The controlling of the X and Y axis motor stage and the output voltage of the detector for each position are obtained using the NI LabVIEW.

D. 0.2 THz Imaging Using the Detector IC

Fig. 12 shows the samples used for the 0.2 THz imaging measurements. The sample was implemented as an "M"-shaped copper tape of 60 μm thickness with different line widths. The image is obtained by raster scanning over a 70 × 70 mm^2 area which is marked in a yellow box shown in Fig.12. Measured 0.2 THz image is shown in Fig. 13. The

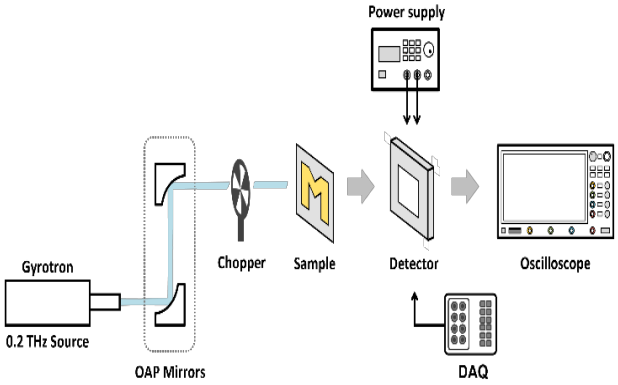

Fig. 11. Measurement setup for obtaining the 0.2 THz imaging using the proposed detector module.

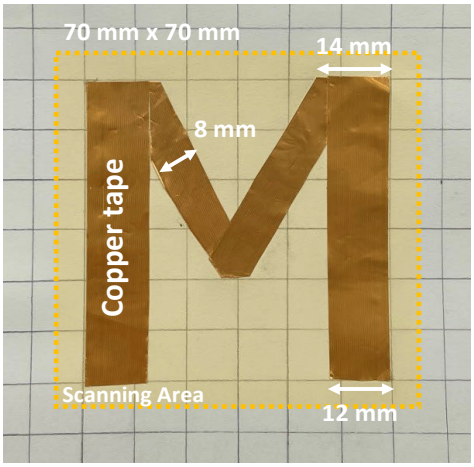

Fig. 12. Photograph of a sample for THz imaging.

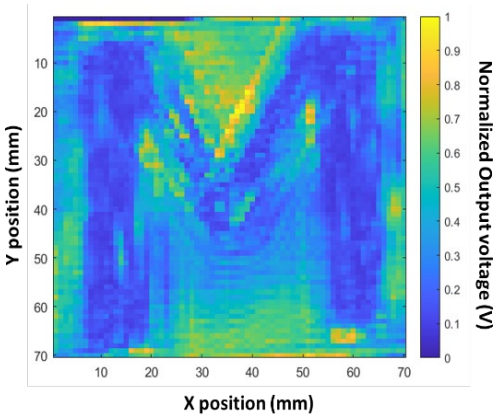

Fig. 13 Measured 0.2 THz image using the proposed detector module.

measured image SNR is to be 22.26 dB. The image shows that the proposed CMOS detector IC can distinguish a line width of 8 mm or less.

IV. CONCLUSION

A CMOS detector using 0.25 μm technology is proposed for sub-terahertz imaging. A detector module for imaging is implemented using the off-chip main amplifiers and the proposed CMOS IC, which includes the on-chip antenna, differential detector cores, and buffer stage with the sub-threshold preamplifier. The size of the proposed detector is miniaturized by using the on-chip antenna based on folded dipole structure. The differential CMOS detector uses a common-source topology with gate-drain capacitors to enhance the voltage responsivity. The off-chip main amplifiers with high gain and band-pass frequency response are used to increase the module's voltage responsivity and signal-to-noise ratio of the 0.2 THz images. The size of the detector unit implemented in the 0.25 μm CMOS process with a transition frequency of approximately 10 GHz is 500 μm × 370 μm. The measured R_V and *NEP* of the proposed detector show a high responsivity of 2.57 MV/W and a low value of 43.61 pW/√Hz at the incident signal of 0.2 THz, respectively. The 0.2 THz imaging measurement shows that the detector can distinguish a line width of 8 mm or less by using raster scanning with a step of 1 mm to an area of 70 mm × 70 mm.

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