An Evaluation and Comparison of State-of-the-Art Flip-Flops for Low-Power Applications

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***Abstract* – Flip-Flop (FF) is the basic block of sequential digital circuits, which has a significant impact on the speed, power, and stability of digital systems. Reducing the power consumption of FFs is an attractive solution for attaining good energy efficiency of digital systems. However, the conventional TGFF (Transmission-gate flip-flop) consumes excessive dynamic power at clock inverters even though the data transition does not occur. To eliminate redundant clock transitions, some techniques are applied. This paper analyzes and compares recently published low-power FFs in 65 nm CMOS.**

***Keywords*—Activity ratio, Flip-Flop(FF), Low power, Redundant transition free**

I. INTRODUCTION

For constrained battery life in IoT (Internet of Things) applications, minimizing the power consumption of digital circuits is becoming important [1]. A few million flip-flops (FFs) are used in the overall digital system, which may be one of the most dominant causes leading to dynamic power consumption [2]-[4].

Conventional transmission-gate flip-flop (TGFF) is widely used in most applications, but its always-toggling at clock inverters (Fig. 1) leads to excessive power consumption at a typical activity ratio (~10%) in modern digital systems.

On the other hand, many low-power applications exploit near-threshold voltage (NTV) computing for achieving maximum energy efficiency of digital systems [5]-[6]. This demands the reliable operation of FFs at low supply voltages, as sequential logic elements tend to be vulnerable to PVT variation [7]. Fully static and contention-free FFs are preferred in order to guarantee their reliable operation at NTV conditions.

For these reasons, many recently published low-power FFs [8]-[11] aim to minimize unnecessary clock transitions at the internal clocked node (*CKN*), while maintaining their static operation (*CKN* makes the slave latch in transparent mode conditionally at a rising *CK* edge). Usually, the static operation of a Flip-Flop (FF) helps not only its robustness but also energy conservation by eliminating unnecessary power losses due to contention. These new FFs generally show lower energy dissipation than a TGFF, but their different energy-saving mechanisms render some of them more suitable for a given operating condition. This paper evaluates recent low-power FFs in a wide range of operating conditions and compares their performance and power dissipation.

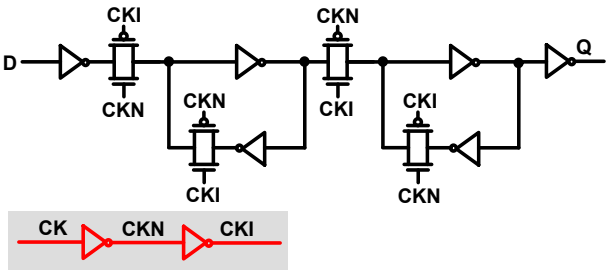

Fig. 1. Conventional TGFF

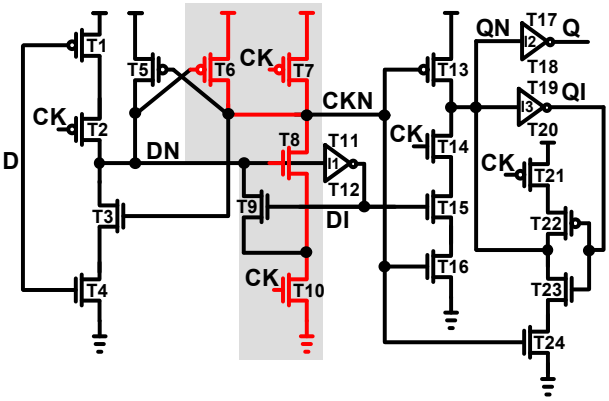

Fig. 2. Static single-phase contention-free flip-flop (S2CFF)

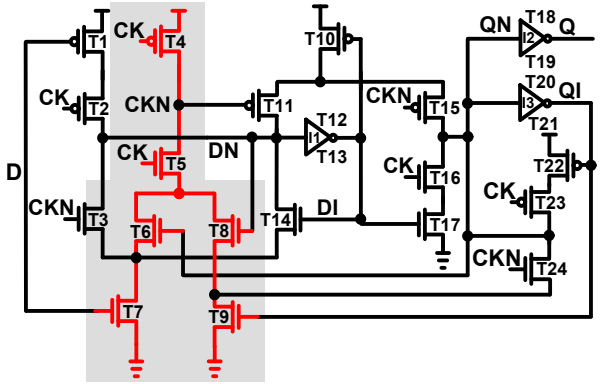

Fig. 3. Changing-sensing flip-flop (CSFF)

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II. REVIEW OF STATE-OF-THE-ART FFS

A. Static single-phase contention-free flip-flop(S2CFF)

S2CFF [8] shown in Fig. 2 is developed from dynamic TSPC FF [12] with additional transistors featuring glitch-prevention. It is static and contention-free like TGFF and operates reliably at near-threshold voltage (NTV) conditions. The highlighted transistors in Fig. 2 make a new internal clock node for eliminating redundant clock toggling at clock inverters shown in Fig. 1. However, the redundant clock transition remains when $D = 0$, $DN = 1$, and $QN = 1$, which leads to excessive power even though an input data (D) is same as a stored data (QI).

B. Changing-sensing flip-flop (CSFF)

CSFF [9] in Fig. 3 has a change-sensing circuit that detects the difference between the input data (D) and the stored data (QI) in the FF. When $CK = 0$, the output of the change-sensing circuit (CKN) is pre-charged. The master latch stores the new input data, while the slave latch keeps the previous data. When $CK = 1$, CKN is discharged only when the input data (D) and the stored data (QI) are different. ($D = 1$ & QN(an inverted output Q) $= 1$, DN(an inverted input D) $= 1$ & $QI = 1$). The discharged CKN enables the master latch to hold the new input data and transfer it to the slave latch. If the same input data (D) is transferred to the slave latch repeatedly at every clock cycle, CKN stays high even when a rising CK comes in. The change sensing circuit is activated only when the new data is different from the stored data (QI) and saves unnecessary power consumption of the following circuit. However, CSFF can run into a critical race condition when D changes 0 to 1 during $CK = 1$, $DN = 1$, and $QN = 1$. DN and CKN are discharged at the same time, so it is difficult to hold the original data in a slave latch. In addition, when $CK = 1$, $D = 1 \rightarrow 0$, $CKN \approx 0$, $DN = 0$, and $QN = 0$, no pull-up path for DN and QN is formed, which interrupts reliable operation at NTV.

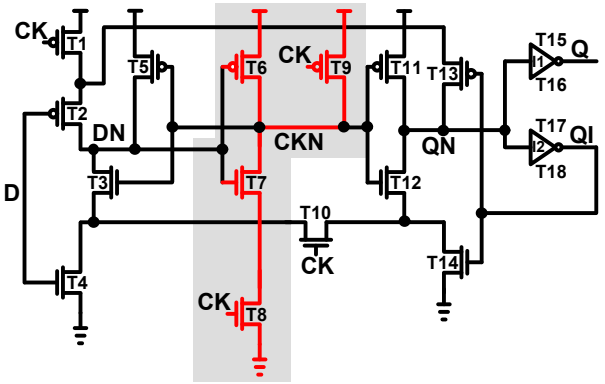

Fig. 4. 18-transistor single-phase clocked flip-flop (18TSPC)

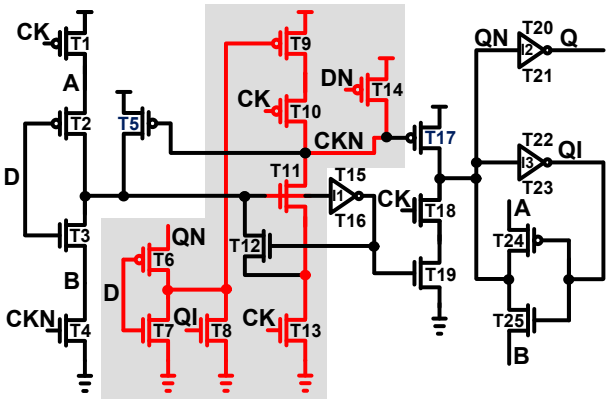

Fig. 5. Redundancy eliminated flip-flop (REFF)

C. 18-transistor single-phase clocked flip-flop (18TSPC)

18TSPC [10] shown in Fig. 4 is developed from MUX2_based FF. To eliminate redundant transistors, the logically equivalent nodes are merged. However, 18TSPC the has same internal clock buffering scheme like S2CFF, which still has redundant transitions. Besides, if CK goes to high when $D = 0$, $CKN = 1$, $DN = 1$, and $QN = 0$, a contention path is made, which may lead to failure at NTV.

D. Redundancy eliminated flip-flop (REFF)

REFF [11] in Fig. 5 eliminates all redundant clock transitions of internal clocked nodes and redundant transistors. With completely eliminated redundancy, REFF minimizes dynamic power consumption and guarantees reliable operation at low-voltage region.

Fig. 6 shows distinct FF's CKN waveform of low-power FFs including TGFF. Because of internal clock inverters, TGFF always reverses the clock phase regardless of the output state update. S2CFF and 18TSPC have the same internal clock buffering scheme (CKN), so they still have

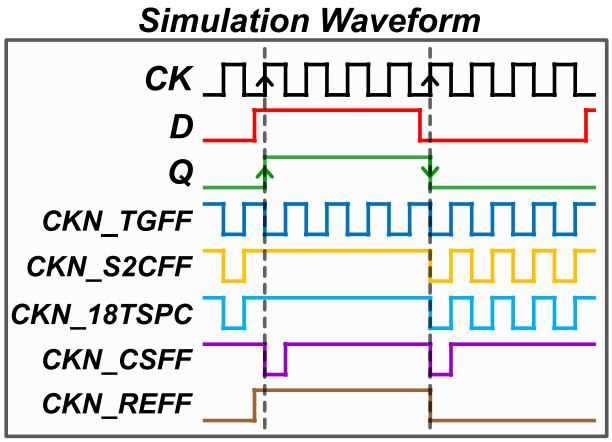

Fig. 6. Transitions of internal clocked node (CKN)

***Functionality Check PASS or FAIL (Yield)**

	TGFF	S2CFF	CSFF	18TSPC	REFF
1.2V	P(100%)	P(100%)	F(98.4%)	P(100%)	P(100%)
1.15V	P(100%)	P(100%)	F(97.6%)	P(100%)	P(100%)
1.1V	P(100%)	P(100%)	F(96.8%)	P(100%)	P(100%)
1.05V	P(100%)	P(100%)	F(96.2%)	P(100%)	P(100%)
1V	P(100%)	P(100%)	F(95.3%)	F(99.9%)	P(100%)
⋮	⋮	⋮	⋮	⋮	⋮
600mV	P(100%)	P(100%)	F(73.9%)	F(89.4%)	P(100%)
550mV	P(100%)	P(100%)	F(71.8%)	F(86.0%)	P(100%)
500mV	P(100%)	P(100%)	F(69.4%)	F(82.0%)	P(100%)
450mV	P(100%)	F(99.6%)	F(64.1%)	F(77.0%)	F(99.7%)
400mV	F(98.7%)	F(96.6%)	F(52.3%)	F(72.4%)	F(97.5%)
Min.VDD	0.45V	0.5V	X	1.05V	0.5V

- 1k Monte Carlo simulation each (global + local)
- Testing Clock Frequency = 1MHz

Fig. 7. Reliability of FFs

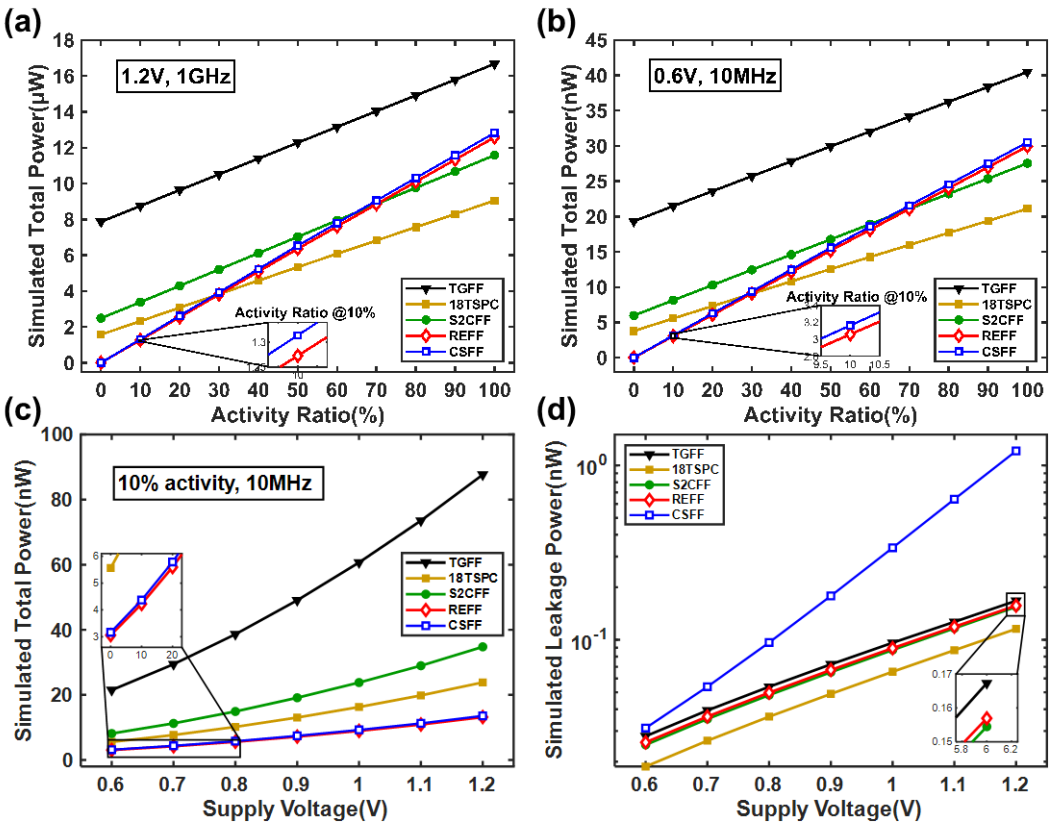

Fig. 8. Post layout simulation results of FFs. (a)Average power at 1V, (b) Average power at 0.6V, (c) Average power at 10% activity ratio by sweeping VDD, (d) Leakage power at different VDD

TABLE I. Performance Summary and Comparison

	TGFF	S2CFF [8]	CSFF [9]	18TSPC [10]	REFF [11]
	Conventional	ISSCC 2014	JSSC 2018	JSSC 2019	JSSC 2021
Static Operation	YES	YES	NO	YES	YES
Contention-Free	YES	YES	NO	NO	YES
Redundant Clock Transition	YES	YES	NO	YES	NO
Device Count	24	24	24	18	25
Power(μW) @1.2 V [a]	8.75	3.38	1.31	2.32	1.27
Power(nW) @0.6 V [b]	21.47	8.13	3.16	5.56	3.05
Leakage Power(nW) @1.2 V	0.16	0.15	1.20	0.11	0.15
Min. VDD	0.45	0.5	X	1.05	0.5
T_{CK-Q}(ps) @1.2 V	160.5	144.1	152.9	136.4	135.3
T_{setup}(ps) @1.2 V	22.9	97.9	106.9	57.2	134.2
T_{hold}(ps) @1.2 V	1.5	-18.7	-16.0	50.1	-22.2
PDP_{CK-Q}(fJ) [c]	1.409	0.487	0.200	0.317	0.172

[a] 10% activity ratio, f_{CK} = 1 GHz, [b] 10% activity ratio, f_{CK} = 10 MHz,
[c] PDP= Average Power(1.2 V, @10% activity ratio, f_{CK} = 1GHz)·T_{CK-Q}
*CK_Q Delay : Average of D = 0, D = 1 case *Setup / Hold Time : Average of D = 0, D = 1 case

redundant transitions when the input *D* is low. On the other hand, CSFF and REFF minimize transitions at *CKN*, which saves dynamic power than other FFs.

III. SIMULATION RESULT AND ANALYSIS

The aforementioned flip-flops are laid out and evaluated in various operation conditions. For comparison, traditional TGFF is also implemented and evaluated. The test was performed in a 65-nm CMOS process design kit. For fair a comparison, all FFs use the same process technology and transistor lengths/widths (minimum length for all transistors, and PMOSs use 2x width of NMOSs). Fig. 7 displays the minimum operating voltage of FFs in 1k Monte Carlo simulations (global+local) for a voltage range from 0.4V to 1.2V by 0.05V step. The result shows that fully static and contention-free FFs operate reliably at lower supply voltage than CSFF and 18TSPC with floating nodes and contention issues.

Fig. 8 shows the simulated power dissipation of FFs. By eliminating redundant transitions of clocked nodes and redundant transistors, REFF and CSFF show relatively low

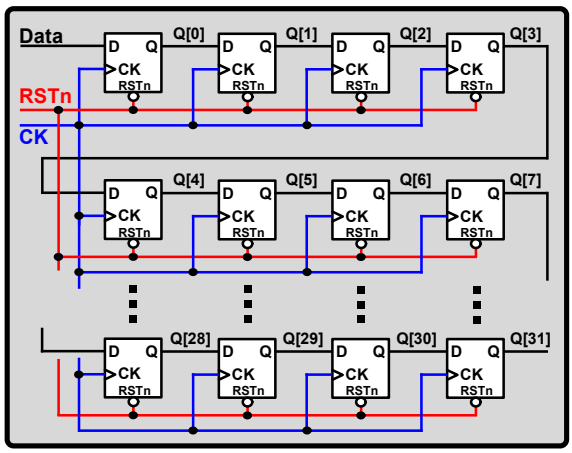

Fig. 9. Block diagram of 32-bit shift register

power consumption than other FFs when the data activity ratio is low (Fig. 8(a) and 8(b)). S2CFF and 18TSPC consume larger dynamic power than REFF and CSFF because they still have unnecessary clock transitions when $D = 0$, $CK = 0 \rightarrow 1$, $DN = 1$, and $QN = 1$. Fig. 8(d) shows the leakage power of FFs at operating voltages from 0.6 V to 1.2 V, averaged over all cases of internal node states (*D, CK, DN, QN*). CSFF [10] has a floating node at *DN* when $D = 1 \rightarrow 0$, $CK = 1$, $CKN \approx 0$, $DN = 0$, and $QN = 0$, which causes contention at *DN*, thus CSFF has larger leakage power than other FFs. Table 1 summarizes the results and compares other FFs. The Power-delay product (PDP = Average power × CK_Q delay @VDD = 1.2 V, @10% activity ratio), one of the circuit performance indicators shows REFF has the best performance. TABLE I shows the summary of simulation results and compares different FFs.

To validate the FF's actual performance, 32-bit shift registers with different FFs were designed as shown in Fig. 9. The 32-bit shift register based on CSFF and REFF consume less power than other FF-based shift registers (@f_{CK} = 10 MHz / 1 GHz), but they show lower speed than others. On the other hand, TGFF-based shift register consumes larger dynamic power than others and show the best speed among them.

Table II. Performance Summary and Comparison (32-Bit Shift-Reg)

		TGFF	S2CFF [8]	CSFF [9]	18TSPC [10]	REFF [11]
		Conventional	ISSCC 2014	JSSC 2018	JSSC 2019	JSSC 2021
10M Hz	Average Power (μW) @1.2V	2.88	1.74	0.61	1.24	0.49
1GHz		287.3	173.0	59.4	122.6	49.2
MAX Freq. (GHz)		3.71	2.89	2.55	3.50	2.60

IV. CONCLUSIONS

An energy-efficient flip-flop operation at NTV requires the following conditions: 1) fully static, 2) contention-free, 3) no redundant transition, and 4) no redundant transistor. TGFF is fully static and contention-free, but clock toggling at clock inverters always consumes dynamic power. S2CFF operates reliably down to 0.45V but still has partial redundant transitions at the internal clocked node. 18TSPC has the lowest transistor count, but it has contention and redundant transitions when input *D* is low. CSFF eliminates redundant clock transitions with the change sensing scheme. However, inevitable floating node *DN* causes contention, and sizing effort is needed to prevent failure at race condition (input *D* goes to high during $CK = 1$, $DN = 1$, $QN = 1$). REFF satisfies all requirements for energy-efficient operation at NVT.

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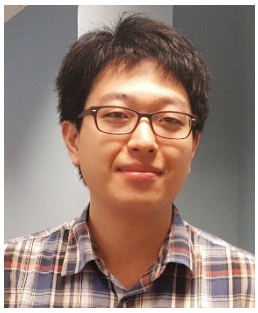

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