Design of InP HBT 230-GHz Frequency Multiplier Chain with a Multiplication Factor of 18

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***Abstract* - A x18 frequency multiplier chain has been designed in this work based on a 250-nm InP HBT technology. Three frequency multipliers are cascaded to form the integrated frequency multiplier chain: a 38-GHz frequency tripler, a 115-GHz frequency tripler, and a 230-GHz frequency doubler. The performances of the circuits are characterized based on simulation and presented in this paper, which will be verified with measurement when chip fabrication is completed. The 38-GHz cascode frequency tripler shows a saturated output power of 2.6 dBm at 38.3 GHz, while the 115-GHz single-balanced differential tripler exhibits an output power of 2.3 dBm at 115 GHz. With the 230-GHz frequency doubler, saturated output power of 3.2 dBm was obtained. The fully integrated multiplier chain shows a saturation output power of -3.4 dBm at 230 GHz, with a peak conversion gain obtained as -2.9 dB at an input power of -1.0 dBm. The 3-dB bandwidth is 27 GHz, covering a frequency range of 223 - 250 GHz.**

***Keywords*—250-nm InP HBT, Frequency multiplier**

I. INTRODUCTION

The frequency between 100 GHz to 10 THz, which is widely noted as the THz frequency band, is attracting increasing attention these days. The traditional application fields of the THz band included the spectroscopy and imaging, but its application has been expanding and now covers highly influential areas such as broadband communication and radars [1]. The two core components for the of THz systems are the signal sources and receivers. The realization of these components are increasingly difficult as frequency increases. In particular, to attain high-performance THz signal sources is very challenging as the available output power rapidly drops with increasing frequency, which requires extensive efforts for technical enhancement.

For semiconductor chip-based THz signal sources, two approaches are widely considered. One is the on-chip THz oscillator. The main advantage of this approach is the elimination of the needs for separate off-chip components for generating signals, while achieving high output power and low phase noise is challenging. Another approach is to employ a frequency multiplier, which is driven by an external signal source with a lower frequency. Although additional off-chip components are needed with this approach, more stable and potentially higher performance can be obtained when high-quality external signal sources are available. This work is based on the second approach.

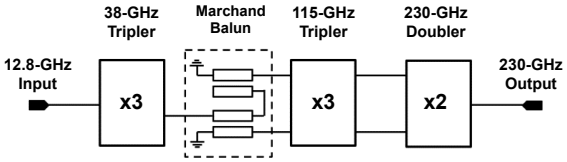

Fig. 1. Block diagram of the 230-GHz x18 frequency multiplier chain

Widely employed in the past for THz frequency multipliers were Schottky barrier diodes (SBDs) [2-5]. While they provide the nonlinearity suitable for frequency multiplication, the lack of the gain limits the performance such as the conversion gain. For this reason, transistors are often the device of choice for frequency multipliers, as they are intrinsically nonlinear device when proper bias conditions are applied and also can provide gain when needed. Despite the difference in the device structure, both bipolar junction transistors (BJTs) and field-effect transistors (FETs) offer nonlinearity and thus can be used for frequency multipliers. There have been growing number of transistor-based frequency multipliers based on FETs [6, 7] and BJTs [8, 9] operating at the THz frequency band.

In this work, 250-nm InP heterojunction bipolar transistors (HBTs) from Teledyne have been employed for the implementation of two frequency triplers and a frequency doubler with different operation frequency levels, each providing output frequency of 38 GHz, 115 GHz, and 230 GHz, respectively. Further, they were integrated in a single chip to realize a x18 frequency multiplier chain that converts a 12.8-GHz input signal to a 230-GHz output signal, which also includes a balun for single-ended-to-differential configuration conversion. The circuit can be considered as an advanced version of the previous work reported recently [10], with an increased multiplication factor and adjusted output frequency for the required application.

When transistors are employed for frequency multipliers, the multiplication is typically achieved based on either nonlinearity or mixing function that employs the input for two inputs. For frequency doublers and triplers, which are the most common choices as a unit multiplier stage for integrated

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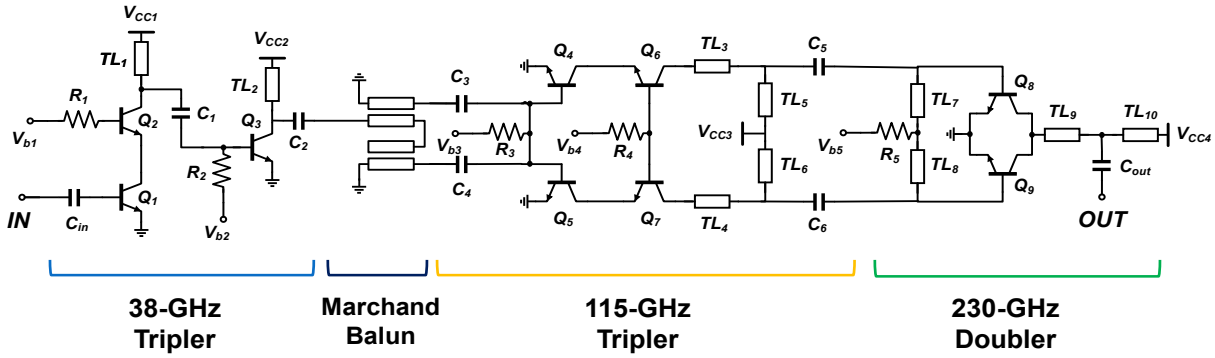


Fig. 2. Circuit schematic of the 230-GHz x18 frequency multiplier chain

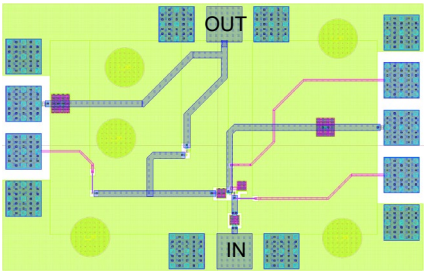


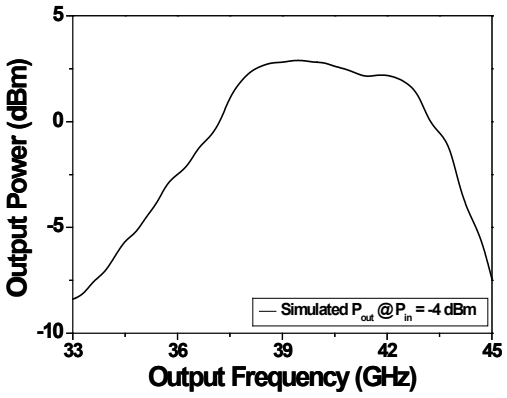
Fig. 3. Layout of the 38-GHz frequency tripler

frequency multiplier chains, the input and output may be configured single-ended or differential depending on the specific topology adopted. Hence, when choosing the unit multiplier stage topology, the match of the configuration (single-ended or differential) at the interface needs to be considered in addition to the required performance for each stage. Also, when a high-frequency test is considered, single-ended input and output configurations are preferred, with possible insertion of baluns as needed. In this work, the second tripler was designed with a differential configuration as the following frequency doubler has a differential input with the most preferred configuration as will be described in the design section. Hence, to accommodate the differential input of the second tripler, a balun is needed somewhere prior to the second stage to allow a single-ended test setup. One option is to place a balun at the front of the multiplier chain followed by a differentially configured first-stage tripler, while another option is to employ a single-ended tripler at the front with a balun attached at the output. In this work, the second approach was adopted, in favor of a small-sized balun owing to a short wavelength at the higher frequency. This configuration will also allow single-ended configuration for the first-stage tripler, which also contributes to reduced size of the entire multiplier chain. For both triplers, cascode stage was employed, which would provide higher gain leading to more efficient excitation of the desired third harmonic.

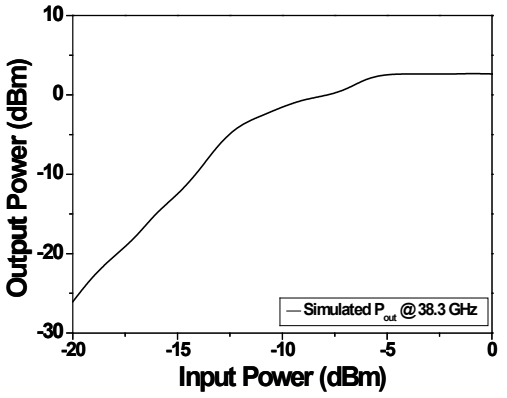
The block diagram of the integrated frequency multiplier chain is shown in Fig. 1. The schematic of the entire integrated frequency multiplier chain is provided in Fig. 2. To verify the performance of each circuit component, individual circuits were also built with for characterization purpose. The circuit is under fabrication at the moment and the performances predicted from simulation will be introduced in this paper. Each of the frequency multipliers are described in Section II – IV, which will be followed by Section V that will present the simulation result of the integrated frequency multiplier.

II. 38-GHZ FREQUENCY TRIPLER

As shown as the front-end circuit in Fig. 2, the 38-GHz frequency tripler converts the input signal around 12.8 GHz to 38.3 GHz output signal, both based on single-ended configuration. The layout of the tripler designed for



(a)



(b)

Fig. 4. Simulated output power of the 38-GHz frequency tripler plotted as a function of (a) output frequency and (b) input power

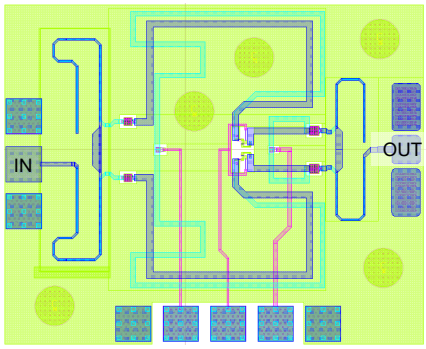


Fig. 5. Layout of the 115-GHz frequency tripler

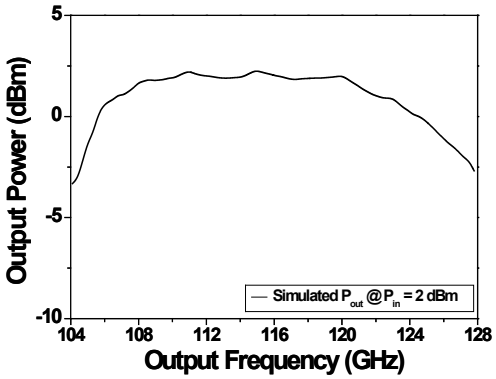
individual characterization is shown in Fig. 3. The chip size is 880 x 560 □ m^2 including DC and RF pads. The cascode first stage is basically an amplifier and will linearly amplify the input signal when the input power is low enough. The amplification will be further helped by the second-stage buffer, which is in common-emitter configuration. However, when the input power grows, the nonlinear characteristics of the entire circuit will gradually increase and eventually prevail. Hence, the output signal will be dominantly the 3rd harmonic of the input signal, a desired property for a frequency tripler. The tripler is never perfect and the output will certainly include the other frequency components, the most pronounced is still the fundamental component. The loads for both stages will serve this purpose. The cascode first stage employs a load composed of TL1, which serves as a short stub. It also forms an interstage matching together with C1, working as a filter that suppresses unwanted fundamental component. The second stage is followed by TL2 and C2, providing a similar function of suppression.

The simulated performance of the frequency tripler is shown in Fig. 4, for which full electromagnetic (EM) simulation was performed together with the schematic level circuit simulation based on the device models provided by the foundry. This procedure will be the same for all the circuits discussed in this paper. Fig. 4(a) shows the output power plotted as a function of the output frequency at a fixed input power of -4 dBm. The peak output power is 2.9 dBm at 39.6 GHz, with a 3-dB bandwidth of around 6 GHz. Shown in Fig. 4(b) is the output power vs input power, indicating the linearity performance of the circuit. At a fixed output frequency of 39.6 GHz, the output is saturated at 2.9 dBm. A peak conversion gain of 8.5 dB was obtained near an output power of -1.5 dBm at this frequency.

III. 115-GHZ FREQUENCY DOUBLER

The schematic of the 115-GHz frequency tripler appears right after the Marchand balun in Fig. 2. The layout of the individual version designed for characterization is shown in Fig. 5, indicating the chip size of 700 x 880 □ m^2 with DC and RF pads included. Note that baluns are placed at the input and output, which are purely for the characterization purpose. The core of the frequency tripler is a cascode differential pair with Q4 – Q7. It amplifies differential input signal when a low input power is maintained. At elevated injected power level, however, the harmonic components will develop, among which the 3rd harmonic component will be the largest. This leads to a frequency tripler operation. The signal coming out of the circuit core will, of course, include the fundamental component. The suppression of the fundamental component will be carried out by the load of the tripler, which is composed of TL3 – TL6, together with C5 and C6. This load, in fact, is designed as a high-pass filter that suppresses the fundamental frequency of 38 GHz.

Fig. 6 shows the results obtained with simulation based on a similar procedure described in the previous section. With an input power of 2 dBm that is delivered from the preceding 38-GHz frequency tripler, an output peak power of 2.3 dBm was obtained at 115 GHz output as shown in Fig. 6(a). The 3-dB bandwidth is 21 GHz, covering a range of



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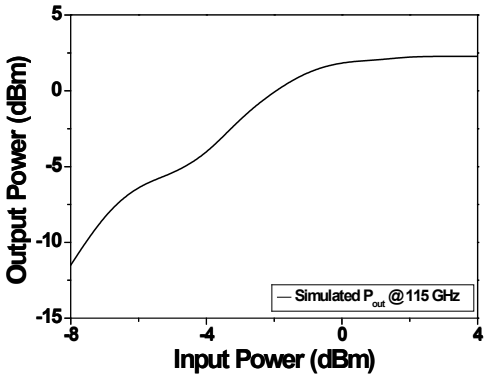

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Fig. 6. Simulated output power of the 115-GHz frequency tripler plotted as a function of (a) output frequency and (b) input power

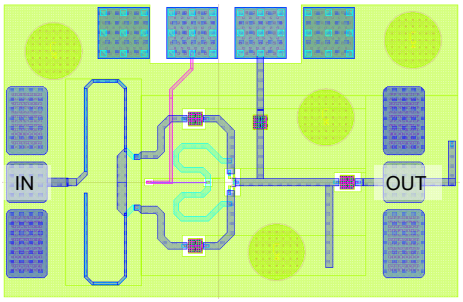
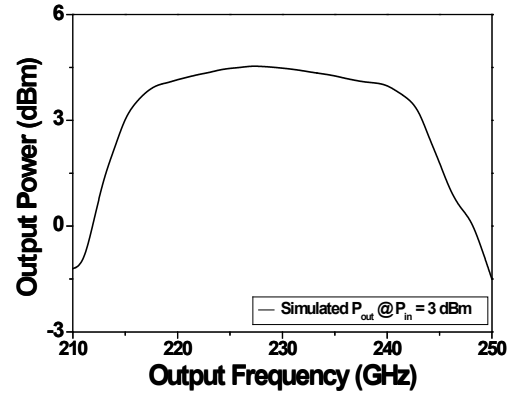
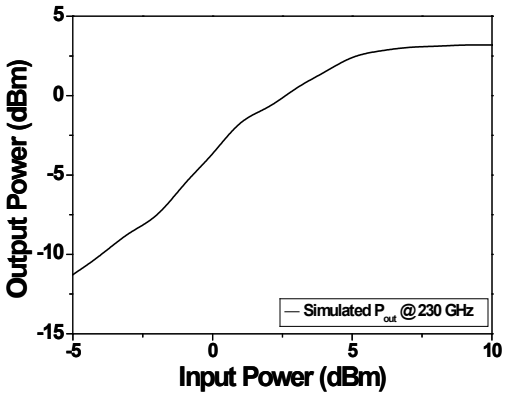


Fig. 7. Layout of the 230-GHz frequency tripler



(a)



(b)

Fig. 8. Simulated output power of the 230-GHz frequency tripler plotted as a function of (a) output frequency and (b) input power.

105 GHz – 126 GHz. When the input power is swept from -8 dBm to 4 dBm at a target output frequency of 115 GHz, the output power reached 2.3 dBm with saturation at an input power of 2.0 dBm, as shown in Fig. 6(b). At this input power level, the conversion gain is 0.3 dB, slightly above the unity. The peak conversion gain is 2.3 dB, obtained at an output power of 1.3 dBm at 115 GHz.

IV. 230-GHZ FREQUENCY DOUBLER

The 230-GHz frequency doubler appears as the last stage in Fig. 2. As the schematic shows, Q8 and Q9 constitute the core differential pair, while the input matching is composed of TL7 and TL8. At the common node of the differential pair where the collectors of Q8 and Q9 are tied together, the fundamental and odd harmonic signals are cancelled out due to the nature of the differential signal, while even harmonics are reinforced. As a result, the 2nd harmonic, which is the strongest among the even harmonics, will dominate, naturally leading to frequency doubler function. In reality, however, the fundamental and odd harmonic signal may survive at the common node due to unintended asymmetry of the circuit. The output matching network based on TL9 and TL10 along with C_{out} is designed to filter out any remaining fundamental signal component, while passing the 2nd harmonic signal developed at the common node. The layout of the individual test circuit is presented in Fig. 7,

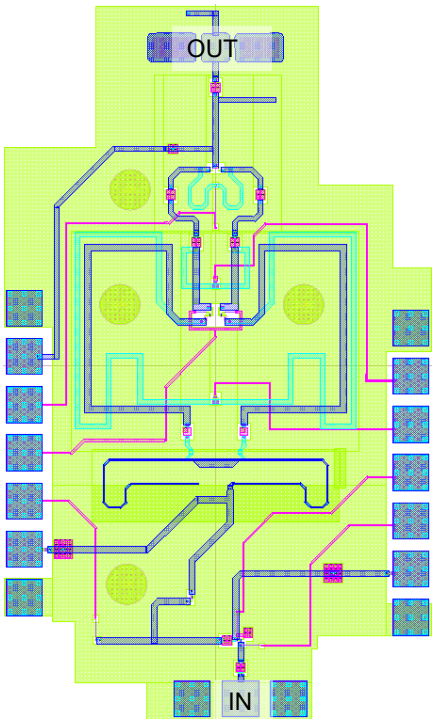


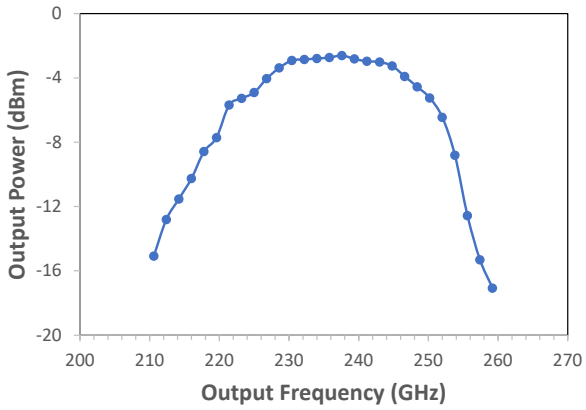
Fig. 9. Layout of the 230-GHz x18 integrated frequency multiplier.

occupying 430 x 660 μm^2 including the necessary probing pads. While symmetry is largely preserved in the layout, there exist some inevitable unbalanced parts in the layout. Nevertheless, the output matching circuit will filter out the fundamental signal, leading to the desired frequency doubler function.

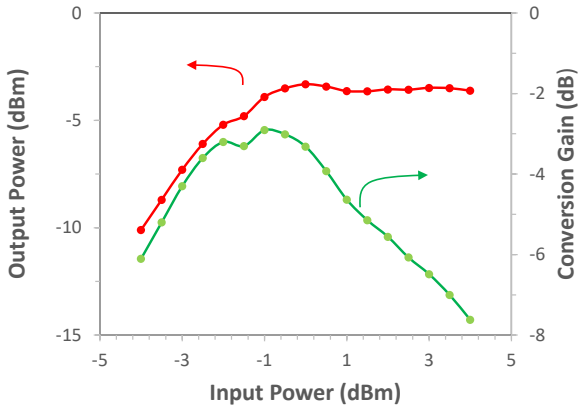
The simulation results of the circuit are shown in Fig. 8. For the output frequency swept from 210 GHz to 250 GHz, the output power is plotted in Fig. 7(a) with a fixed input power of -3 dBm. With this condition, the peak output power is 3.1 dBm, which occurred around 227 GHz. The 3-dB bandwidth is 31 GHz, ranging from 214 GHz to 245 GHz. At the target output frequency of 230 GHz, the saturation output power is 3.2 dBm, which is obtained at an input power of 9 dBm. The overall conversion gain is lower than the frequency multipliers of the lower frequency bands described earlier, a natural consequence of the lowered gain of the active devices employed in the circuit. A peak conversion gain of -2.5 dB is obtained at an output power of 0.5 dBm at 230 GHz.

V. 230-GHZ INTEGREATED FREQUENCY MULTIPLIER CHAIN

The three frequency multipliers described so far are integrated to implement a x18 frequency multiplier chain with an output center frequency around 230 GHz. As presented in Fig. 2, the three unit frequency multipliers are cascaded while a balun is inserted for single-ended-to-differential conversion at the input port of the 115-GHz frequency tripler. For this purpose, a Marchand balun is employed. As the 115-GHz frequency tripler provides the output in the differential manner and the last stage 230-GHz frequency doubler takes the input as a differential signal,



(a)



(b)

Fig. 10. Simulated performance of the 230-GHz integrated frequency multiplier (a) Output power vs output frequency (b) Output power and conversion gain vs input power.

there is no need for a balun between the second and the third frequency multiplier. The layout of the 230-GHz x18 integrated frequency multiplier chain is shown in Fig. 9. The circuit occupies a total area of 900 x 1480 μm^2. The interface between the circuits may require extra layout components that did not appear in the individual circuits, the effect of which needs to be minimized not to affect the matching between the circuit components.

The performance of the integrated frequency multiplier was characterized by simulation in a similar manner as was used for the individual circuits described above. The output power against the output frequency varied from 210 GHz to 260 GHz is plotted in Fig. 10(a). The peak output power reaches -2.6 dBm, which is obtained at 237 GHz, close to the target frequency of 230 GHz. The 3-dB bandwidth is 27 GHz, which covers the range from 223 GHz to 250 GHz. It is noted that a wide bandwidth is highly desired not only for communication applications intended for raised data rate but also for various other high-frequency applications including radar systems where a wider bandwidth results in a higher range resolution. Of course, high output power is also a heavily desired key parameter, especially for very high-frequency applications where system performance is often limited by the maximum output power available from the transmitter, resulting in a tight link budget. As Fig. 10(b) shows, the saturation output power is -3.4 dBm at an input power of 0.5 dBm at fixed output frequency of 230 GHz, as is plotted in Fig. 10(b). Also shown in Fig. 10(b) is the conversion gain of the integrated multiplier, the peak value being -2.9 dB obtained at input and output powers of -1.0 dBm and -3.9 dBm, respectively, with fixed output frequency of 230 GHz.

VI. CONCLUSION

A x18 frequency multiplier chain has been designed in a 250-nm InP HBT technology for operation around 230 GHz, which is composed of two frequency triplers followed by a doubler. Based on simulation, the integrated multiplier chain shows a saturation output power up to -3.4 dBm at 230 GHz with a peak conversion gain of -2.9 dB at an input power of -1.0 dBm. The circuit operates over a frequency range of 223 - 250 GHz leading to a 3-dB bandwidth of 27 GHz. The performance of individual frequency multipliers have also been characterized. The simulated performance will be verified with measurements when chip fabrication is completed. The multiplier chain may serve as a signal source for various high-frequency applications including broadband communication and radar systems operating beyond 200 GHz as a key component in transmitters and heterodyne receivers.

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REFERENCES

[1] J.-S. Rieh, *Introduction to Terahertz Electronics,* Springer, 2021.

[2] G. Chattopadhyay *et al.*, "An all-solid-state broad-band frequency multiplier chain at 1500 GHz," *IEEE Transactions on Microwave Theory Techniques,* vol. 52, no. 5, pp. 1538-1547, May 2004.

[3] A. Maestrini *et al.*, "Schottky diode-based terahertz frequency multipliers and mixers," *Comptes Rendus Physique,* vol. 11, no. 7-8, pp. 480-495, 2010.

[4] U. R. Pfeiffer, C. Mishra, R. M. Rassel, S. Pinkett, and S. K. Reynolds, "Schottky Barrier Diode Circuits in Silicon for Future Millimeter-Wave and Terahertz Applications," *IEEE Transactions on Microwave Theory Techniques,* vol. 56, no. 2, pp. 364-371, Feb. 2008.

[5] C. Mao, C. S. Nallani, S. Sankaran, E. Seok, and K. K. O, "125-GHz Diode Frequency Doubler in 0.13-μm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 44, no. 5, pp. 1531-1538, May 2009.

[6] A. Zamora *et al.*, "A high efficiency 670 GHz x36 InP HEMT multiplier chain," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, Honolulu, HI, USA, 2017, pp. 977-979.

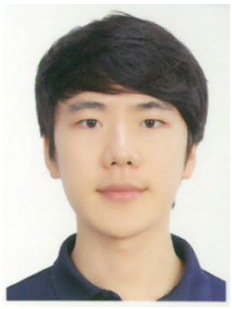
[7] Z. Ahmad, M. Lee, and K. K. O, "20.5 1.4 THz, −13dBm-EIRP frequency multiplier chain using symmetric- and asymmetric-CV varactors in 65nm CMOS," in *2016*

IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2016, pp. 350-351.

[8] M. Bao, Z. He, T. N. Do, and H. Zirath, "A 110-to-147 GHz frequency sixtupler in a 130 nm Sige Bicmos technology," in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, Madrid, Spain, 2018, pp. 105-108.

[9] M. Hossain, K. Nosaeva, N. Weimann, V. Krozer, and W. Heinrich, "A 330 GHz active frequency quadrupler in InP DHBT transferred-substrate technology," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, San Francisco, CA, USA, 2016, pp. 1-4.

[10] G. H. Lim, J. H. Yoo, H. K. Son, D. Y. Kim, and J.-S. Rieh, "A WR3.4 x12 Frequency Multiplier Chain Based on InP HBT Technology," *Journal of Integrated Circuits and Systems,* vol. 8, no. 2, Apr. 2022.



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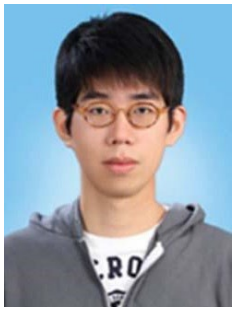

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