A Dynamic Wide-Bandwidth Compensation for Non-Inverting Buck-Boost Converter

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***Abstract*–A non-inverting buck-boost converter is a converter which produces a positive output voltage that is either larger or smaller than the input voltage. This type of converter finds use in various applications in general and mobile application in particular. However, there are some problems that limit the performance of the converter. First, the non-minimum phase characteristic in boost mode makes it hard to compensate the converter with high bandwidth. Therefore, the compensation network is usually designed with small bandwidth to ensure the stability of the system. Thus, the system response over a range of input, output voltage is unacceptable in some applications. In addition, the converter is commonly compensated and optimized for some specific values of input, output voltage. As a result, the stability of the converter is only guaranteed at this particular operating condition and the circuit probably become unstable when the operating condition such as input, output voltages and load current change. In this paper a dynamic compensation technique that optimizes the controller under various input, output voltage, load current conditions is presented which improve bandwidth and transient response of the converter. The theory and simulation show the effectiveness of the approach.**

***Keywords*—Compensation, DC-DC converter, Fast transient response**

I. INTRODUCTION

A non-inverting buck-boost converter is a converter which produces a positive output voltage that is either larger or smaller than the input voltage [1]. A conventional buck-boost converter is formed by cascading a buck and a boost converter. This structure gives rise to a right half plane zero in the converter control-to-output transfer function. This limits the bandwidth of the system and causes overshoot and undershoot in the response of the converter [2]. In addition, the control-to-output transfer function also depends on the input, output voltages and load current (load resistance) of the converter. Thus, normally the controller is designed for a specific operating condition of input, output voltage and load resistance. In addition, the controller's bandwidth is also limited in order to ensure the converter stable even the operating condition is changed. However, this makes the system response over a range of input, output voltage is unacceptable in some applications. This paper presented an optimization process and design for a high bandwidth compensation network.

Fig. 1 shows a buck-boost converter that uses peak current mode-controlled method. The converter is assumed to consist of one inductor L, one output capacitor C_{OUT}. All the components are considered ideal (no conduction loss) and L, C_F, C_{OUT} are assumed large enough so that ripple components of inductor current i_L, capacitor voltage v_{CF}, and output voltage v_{OUT} can be neglected. Thus, these quantities can be treated as constants and equal to their corresponding average values I_L, V_{CF}, V_{OUT} at the switching frequency. The converter operates in continuous conduction mode (CCM) with two phases, $\phi_1$and ϕ_2. The switches are turned on and off at a switching frequency of f_s or switching period T_s. The converter is compensated with type II compensator. Besides, the operation is divided into two separate buck mode and boost mode and controlled in accordance with this operation.

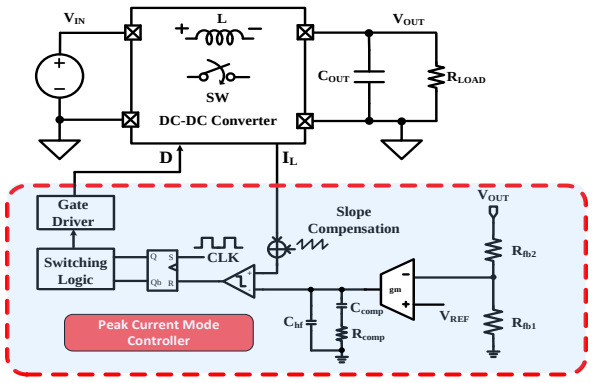

Fig. 1. Buck-boost converter and controller with peak current mode control method

II. COMPENSATION OPTIMIZATION APPROACH

A. Current mode stability analysis for buck converters

The objective is to design a dynamic controller which improve bandwidth and response for both buck and boost modes. Thus, the stability, compensation for each mode operation (buck mode and boost mode) is discussed first and from that the procedure to combine two modes and optimize compensation is demonstrated. Fig. 2 shows the compensation network for buck mode operation.

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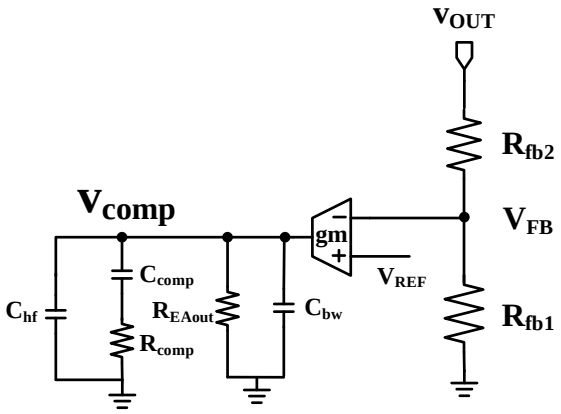

Fig. 2. Type II compensation network for buck mode

The following shows the calculation of compensation values which is mentioned in [3-4]. The compensator transfer function from output v_{OUT} to v_{comp} is given by

$$G_c(s) = \frac{v_{comp}(s)}{v_{out}(s)} = \frac{A_c}{s}\frac{1+\frac{s}{2\pi f_{zEA}}}{1+\frac{s}{2\pi f_{pEA}}} \quad (1)$$

where $A_c = \frac{g_m}{C_{comp}}\frac{R_{fb1}}{R_{fb2}}$, $f_{zEA} = \frac{1}{2\pi}\frac{1}{R_{comp}C_{comp}}$, and

$$f_{zEA} = \frac{1}{2\pi}\frac{1}{R_{comp}C_{hf}}.$$

The control-to-output small-signal transfer function of the buck converter is given in [4] by

$$G_v(s) = \frac{v_{out}(s)}{v_{comp}(s)} = \frac{A_{dc}(1+\frac{s}{2\pi f_{esr}})}{1+\frac{s}{2\pi f_p}}H(s) \quad (2)$$

where $A_{dc} = \frac{R_{out}}{R_i}\frac{1}{1+\frac{R_{out}}{f_s L_f}(m_c D'-0.5)}$, $f_{esr} = \frac{1}{2\pi}\frac{1}{R_{esr}C_{out}}$,

$$f_p = \frac{1}{2\pi}\left(\frac{1}{R_{out}C_{out}} + \frac{m_c D'-0.5}{f_s L_f C_{out}}\right),\ H(s) = \frac{1}{1+\frac{s}{Q_n\omega_n}+\frac{s^2}{\omega_n^2}}.$$

The overall loop gains around the loop including the buck converter and the controller are as written follows:

$$T(s) = G_c(s)G_v(s) = -\frac{A_c}{s}\frac{1+\frac{s}{\omega_{zEA}}}{1+\frac{s}{\omega_{pEA}}}\frac{A_{dc}(1+\frac{s}{\omega_{esr}})}{(1+\frac{s}{\omega_p})(1+\frac{s}{Q_n\omega_n}+\frac{s^2}{\omega_n^2})}. \quad (3)$$

From (3), if $\omega_{zEA} = \omega_p$ *and* $\omega_{pEA} = \omega_{esr}$ the loop gain equation can be reduced to

$$T(s) = -\frac{A_c A_{dc}}{s\left(1+\frac{s}{Q_n\omega_n}+\frac{s^2}{\omega_n^2}\right)}. \quad (4)$$

From this the required values of compensator component are calculated as follows:

$$R_{comp} = \frac{1}{g_m A_{fb} A_{dc}}\frac{f_c}{f_p} \quad (4)$$

$$C_{comp} = \frac{5}{2\pi f_c R_{comp}} \quad (5)$$

$$C_{hf} = \frac{1}{2\pi f_{esr} R_{comp}} - C_{bw} \quad (6)$$

$$R_{fb1} = R_{fb2}\left(\frac{V_{out}}{V_{ref}} - 1\right) \quad (7)$$

Based on this, the values of components are examined over different operating ranges. In all cases, the phase margin should be larger than 45 degree for proper operation. From Fig. 2 to Fig. 7 show the required values of compensation components over different operating conditions. Operating condition can be changed as input, output voltage or load current change. The input or output voltage can also be changed by varying duty cycle D.

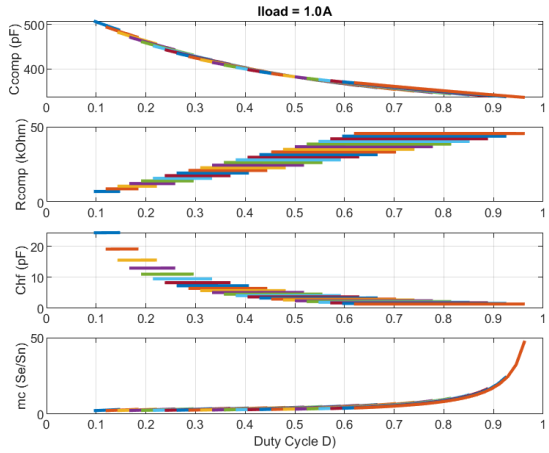

Fig. 3. The required values of compensation components as D is swept from 0 to 1 with step 0.1.

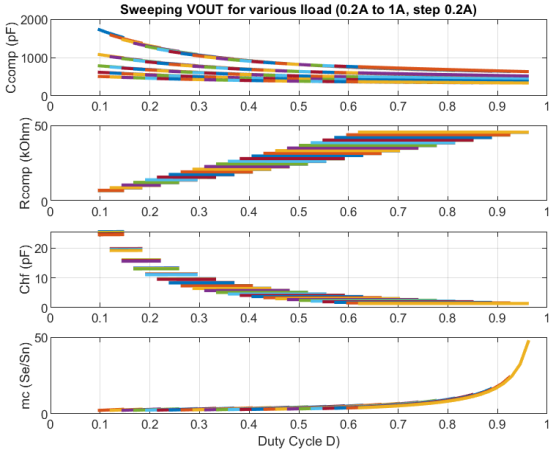

Fig. 4. The required values of compensation components as D is swept from 0 to 1 with step 0.1 and load current is swept from 0.2A to 1A with step 0.2A.

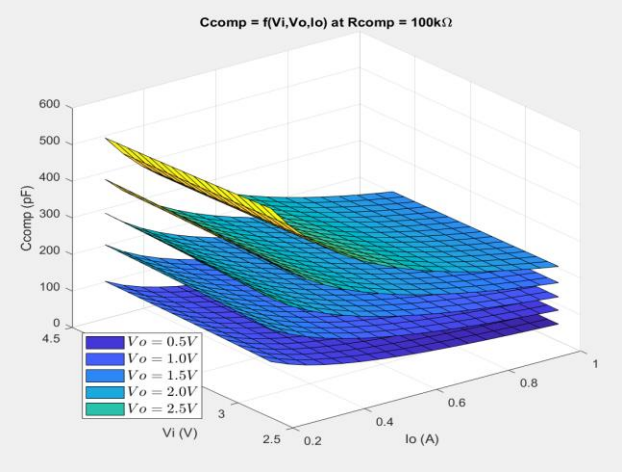

Fig. 5. The required compensation capacitor C_{comp} is plotted over different input, output voltages and load current.

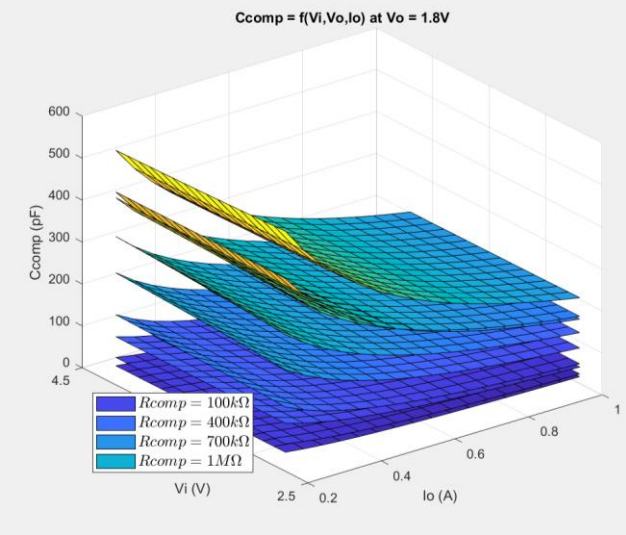

Fig. 6. The required compensation capacitor R_{comp} is plotted over different input, output voltages and load current.

The circuit should have a good phase margin over different operating condition.

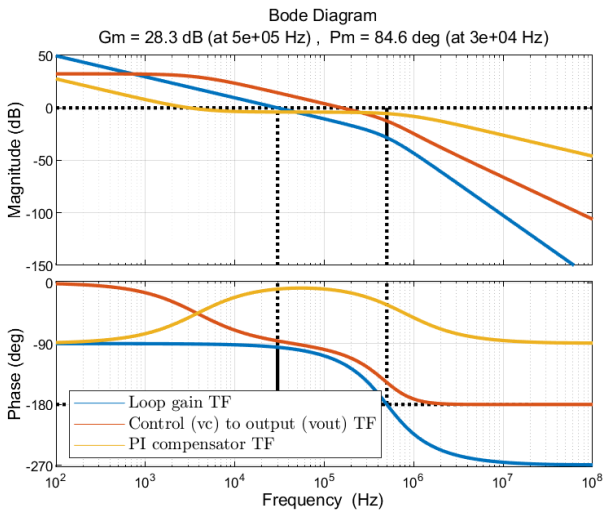

Fig. 7. Gain and phase margin of buck converter at one operating condition.

B. Current mode stability analysis for boost converters

As mentioned in [5], the small-signal model of power stage of a boost converter is expressed as follows:

$$G_c(s) = \frac{v_{comp}(s)}{v_{out}(s)} = \frac{R_{LOAD}(1-D)}{2\,R_{SENSE}}\,He(s) \tag{8}$$

where:

$$G_p(s) = \frac{(1+\frac{s}{2\pi f_{ESR}})(1-\frac{s}{2\pi f_{RHPZ}})}{1+\frac{s^2}{2\pi f_p}} \tag{9}$$

$$f_p = \frac{2}{2\pi\,R_{LOAD}} \tag{10}$$

$$f_{ESR} = 1 + \frac{2}{2\pi\,R_{LOAD}\,C_{OUT}} \tag{11}$$

$$f_{RHPZ} = \frac{R_{OUT}}{2\pi\,L}\,(\frac{V_{IN}}{V_{OUT}})^2 \tag{12}$$

and $He(s)$ is to model of inductor current sampling effect and slope compensation in this control method.

$$He(s) = \frac{1}{1+\frac{s[(1+\frac{S_e}{S_n})(1-D)-0.5]}{f_s}+\frac{s^2}{(\pi f_s)^2}} \tag{14}$$

$$\text{with } S_n = \frac{V_{IN}}{L}R_{SNS}.$$

The design procedure for the boost converter [5] is proceeded as follows:

Step 1: Choose crossover frequency

$$f_c = \min(\frac{1}{5}f_s, \frac{1}{3}f_{RHPZ}) \tag{13}$$

The crossover frequency should be small enough in order to ensure the stability when there exists a right half plane zero in the power stage. In addition, it should not be too low which limits the loop response.

Step 2: Size compensation resistor R_{comp} by solving the equation.

$$K_{COMP-dB}(f_c) = 20\log\left(g_m R_{comp}\frac{R_{fb1}}{R_{fb1}+R_{fb2}}\right) \tag{16}$$
$$= -K_{PW-dB}(f_c)$$

Step 3: Size the compensation capacitor C_{comp}

The compensation capacitor C_{comp} is sized to meet this condition $f_z = \frac{f_c}{10}$ and $f_p > 10f_c$.

Step 4: Size the compensation capacitor C_{hf}

This capacitor is to ensure the gain rolls off after the cross over frequency.

From Fig. 8 to Fig. 10 show the required values of compensation components over different operating conditions. In Fig. 8 the required of compensation capacitor C_{comp} is examined when R_{comp} is fixed and input, output voltages and output load current are swept. In this case, the output required value of the capacitor is checked at some discrete values of the output voltage from 4.2V to 5V.

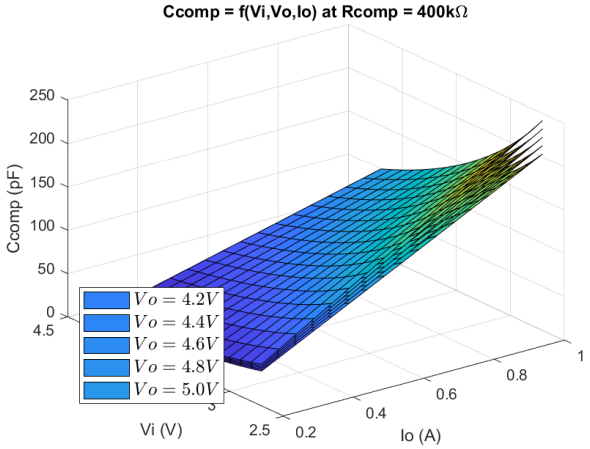

Fig. 8. The required compensation capacitor C_{comp} is plotted over different input, output voltages and load current.

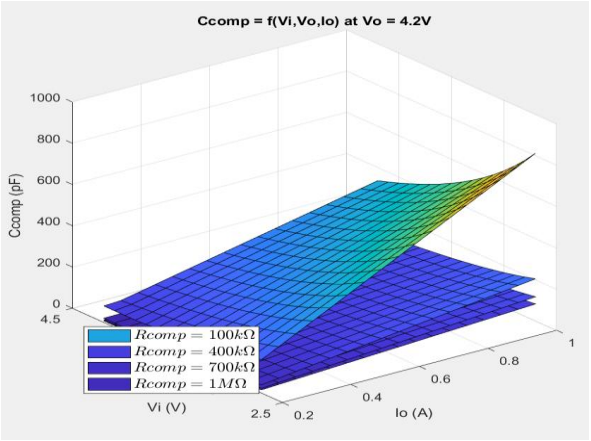

Fig. 9. The required compensation capacitor R_{comp} is plotted over different input, output voltages and load current.

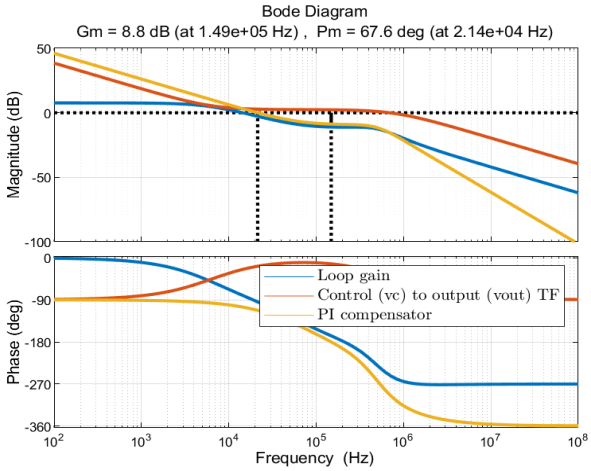

Fig. 10. Gain and phase margin the converter in boost mode at one operating condition.

C. Implementation of Compensation Network

The data obtained from the analysis above is recorded and it is used to design the compensation network which work for different operating conditions. The general block of the compensation network is shown in Fig. 12 and Fig. 13 where C_{comp} and R_{comp} are dynamically changed under during the operation of the circuit. R_{comp1}, R_{comp2}, C_{comp1}, C_{comp2} represented two terminals of the compensation resistor and capacitor, respectively.

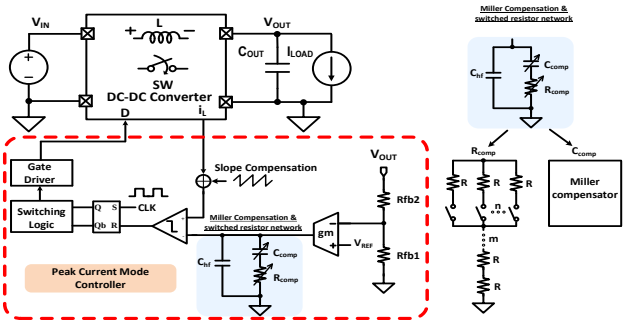

Fig. 11. Compensation network for the DC-DC converter

The compensation capacitor C_{comp} and R_{comp} are varied with the operating conditions such as input, output voltage and load current. This can be obtained by using a network of resistors which can be connected in series or in parallel by switching on/off switches. The same principle can be applied to C_{comp}. In Fig. 12, the value of compensation resistor can be changed from 10Ω to 1MΩ with the decade resistor network. Similarly, the compensation capacitance value varies from 1pF to 1nF. Moreover, the three branches can also be configured to be in parallel in order to increase the capacitance value if necessary. The capacitors are implemented by MOM with woven structure. Using metal layers from M1 to M4, the capacitance density of the structure is 4.34fF/μm^2 and thus, the overall chip area can be reduced. In addition, if the chip area can even be reduced by using Time-Mode Miller Compensation [6] to boost the effective value of C_{comp}.

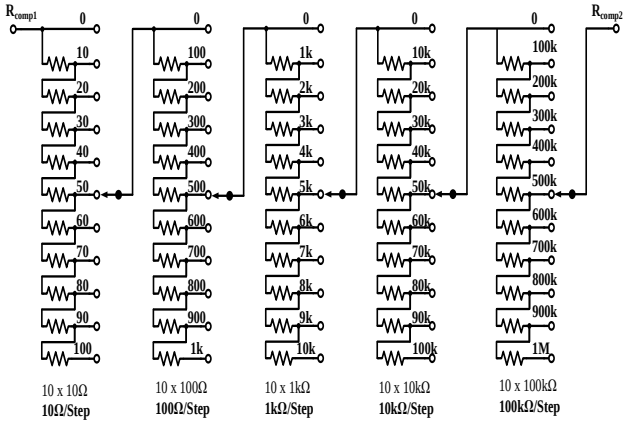

Fig. 12. Implementation of compensation resistor R_{comp}.

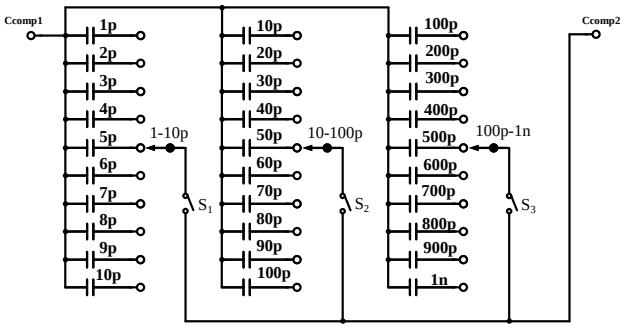

Fig. 13. Implementation of compensation capacitor C_{comp}.

One thing to notice here is that even though many switches are used, however their parasitic resistances and capacitances are much smaller than the values of their compensation components. Thus, the effect of the parasitic elements to the operation of controller network can be ignored. The R_{comp} and C_{comp} are in order of kΩ and pF while parasitic resistance and capacitance are about 1000 times lower.

III. RESULTS AND DISCUSSIONS

The circuit is first simulated for different load conditions. From the simulation, it can be seen that the circuit is stable under different loading conditions.

The chip layout is shown in Fig. 15 with a power stage of the buck-boost converter and the compensation resistor and capacitor.

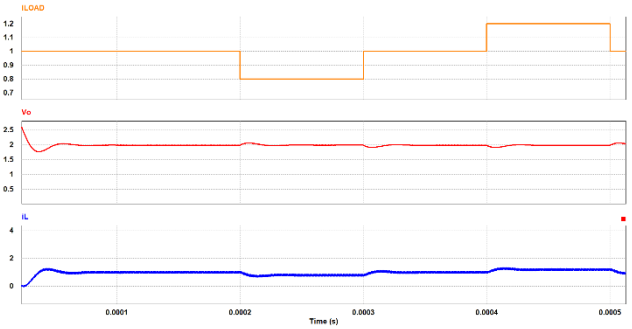

Fig. 134. The output voltage and inductor current under different load conditions.

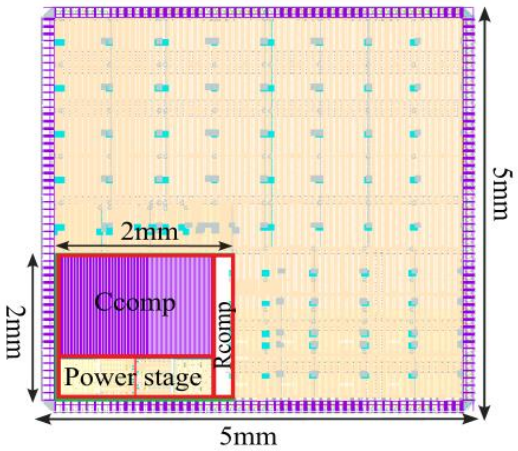

Fig. 15. Chip micrograph with the power stage and compensation network.

IV. CONCLUSION

The paper presented a dynamic compensation method by first analyzing the compensation components' values under different operating conditions such as input, output voltages or load current change. From data obtained from analysis is then used to build a compensation network where values of compensation components are controlled and dynamically changed according to their reference values. The network can be formed by using a network of resistors or capacitors which can be configured to be in series or in parallel depending on the operating condition. Thus, the values of these components are controlled and optimized for each particular operating condition.

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