Counter-Based Frequency Discriminator for Fine Dust Sensor

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***Abstract* – This work presents a counter-based frequency discriminator for a fine dust sensor. Detecting the frequency variations of MEMS resonator according to the fine dust concentration, the proposed frequency discriminator provides digital codes which represents the frequency variations. Since the proposed frequency discriminator is based on the CMOS process, it achieved extremely small area and low power of 0.3 mW, which facilitates the integration into portable devices. The proposed counter-based frequency discriminator covers the input frequency range of 1.6 to 2.4 GHz with a resolution of 50 kHz. Since it has a flexible divider, its resolution and detection speed can be flexibly changed.**

***Keywords*—Counter-based, Fine dust sensor, Frequency discriminator, Window**

I. INTRODUCTION

The increase in fine dust concentration is a cause of respiratory diseases and is emerging as a serious environmental problem these days. The problem becomes more serious as the industry develops. Fine dust is very small dust with a particle diameter of less than 10 μm. Then it cannot be filtered out by human organs. Therefore, people with respiratory diseases should refrain from going out when the concentration is high. An optical element is a widely used method for fine dust sensors to measure the concentration of fine dust. However, it is less accurate when detecting particles smaller than the wavelength of light [1], and can also be less accurate depending on the direction of refraction of the light.

To increase the reliability of the sensor, a system-on-chip (SoC) based smart integrated circuit (IC) can be an alternative. SoC-based smart ICs consist of detecting particles such as MEMS resonators [2] – [4], and the information from the particles is processed on the SoC board. Due to the high interactivity of SoCs, they are area- and cost-effective. In this study, only the SoC part was dealt with, and it was assumed that there is a MEMS resonator whose frequency changes according to the mass on the front side of the SoC. Fig. 1 shows the conceptual diagram of a MEMS resonator. As the number of dust increases, i.e. the concentration of dust increases, the weight of the MEMS resonator increases and the resonant frequency decreases.

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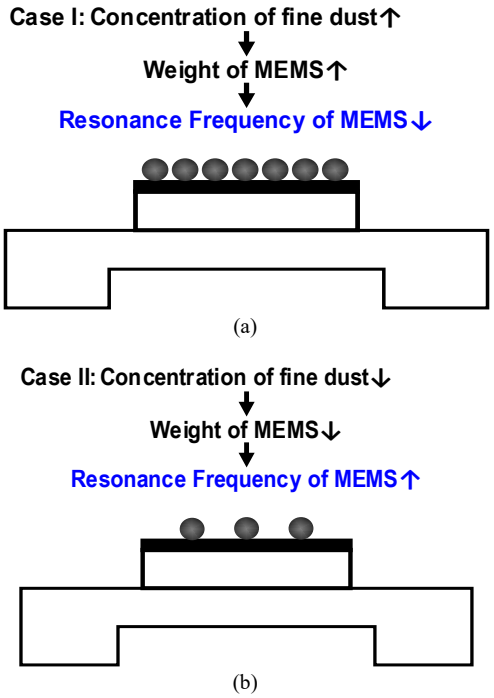


Fig. 1. Comparison of the frequency of the MEMS resonator between two cases; (a) Case I: high concentration of the fine dust (b) Case II: low concentration of the fine dust.

Similarly, as the number of dust decreases, the weight of the MEMS resonator decreases, and the resonant frequency increases. Then the next SoC part, which is the proposed delay-locked loop-based frequency discriminator, detects the frequency change of the resonator.

The rest of this paper is organized as follows. Section II presents the proposed SoC-based frequency discriminator. Section III shows the results and discussion. Section IV provides conclusions.

II. PROPOSED DLL-BASED FREQUENCY DISCRIMINATOR

The proposed frequency discriminator consists an oscillator with a shield, a sensing oscillator, a temperature compensated crystal oscillator (TCXO), a flexible divider, a power gating circuit, two divide-by-4 dividers with an enable, two 20-bit counters, and a subtractor. The oscillator with shield acts as a reference to compare with the sensing oscillator. The frequency of the sensing oscillator is changed according to the concentration of the fine dust. In contrast, the frequency of the oscillator with shield isn't changed since

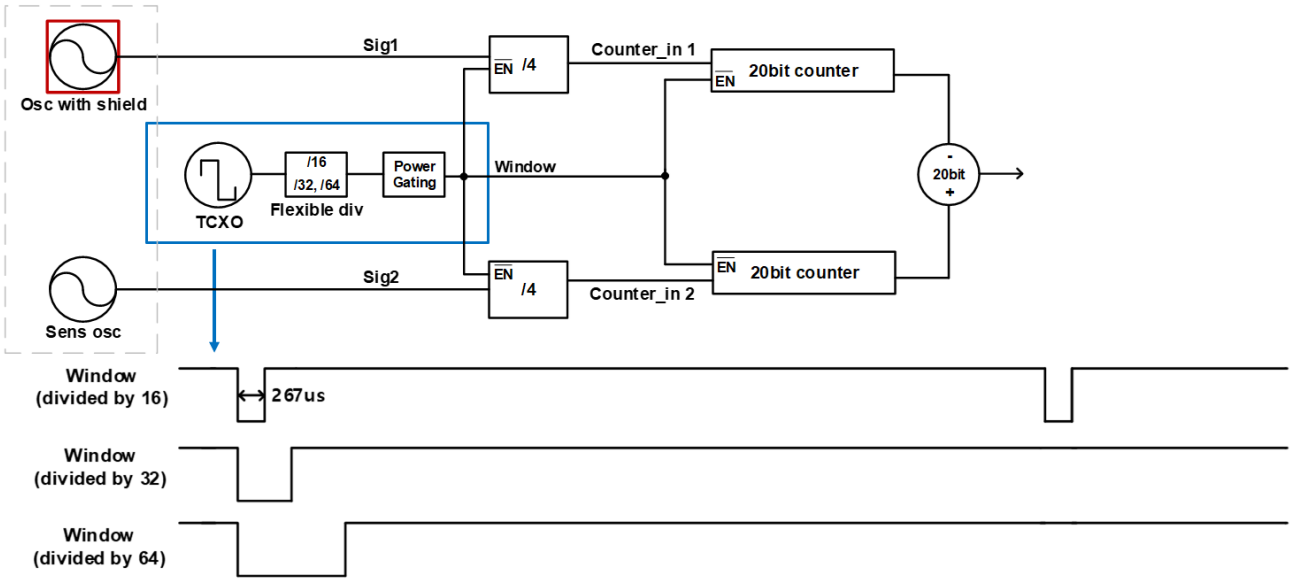


Fig. 2. Overall architecture of the proposed counter-based frequency discriminator.

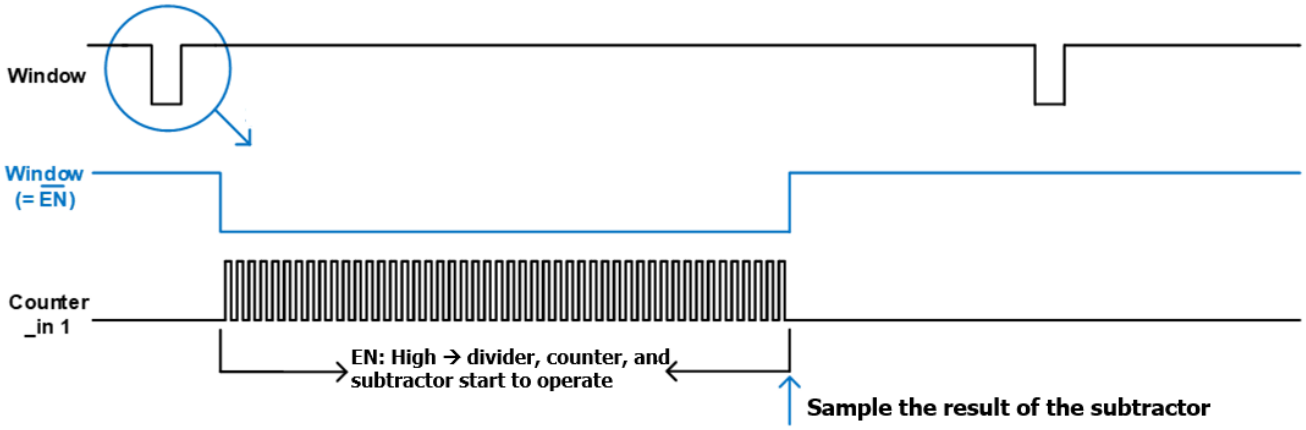


Fig. 3. Timing diagram of the proposed counter-based frequency discriminator.

TABLE I. Target specification of the proposed fine dust discriminator

Target center frequency for detecting	2 GHz
Target resolution for dust detection	50 kHz
Frequency deviation due to dust	3–5 MHz
Expected process variation of frequency	1.6–2.4 GHz

the shield of the oscillator prevents that the dust is attached to the surface of the MEMS oscillator. So, by comparing the frequency of the oscillator with a shield with the oscillator without a shield, which is sensing oscillator, we can obtain the concentration of the fine dust. To compare the frequency of two oscillators, with shield and without shield, two counters are used. By using counters, the frequency of the oscillator can be transformed into a digital code. Then, by subtracting two codes, which represent the frequencies of the oscillator with shied and without shield, respectively, we can detect the concentration of the fine dust. Sig1 is the output signal of the oscillator with shield and Sig2 is the output signal of the sensing oscillator. To decrease the power consumption of two counters and to increase the detection accuracy of the fine dust, two divide-by-4 dividers and window signals were used. A window signal comes from a TCXO, a flexible divider, and a power gating circuit. The TCXO is used to generate a window signal. The flexible divider divides the frequency of the TCXO by 16, 32, or 64. According to the division number, there exists a trade-off between the detection accuracy and the detection speed. If we use the division number of 16, the detection speed is fastest, while the detection accuracy is the worst. In other words, if we use the division number of 64, the detection speed is slowest, while the detection accuracy is the best. In the divide-by-4 divider has the enable port. So, the window signal decides the detection period, which means that the concentration of the fine dust only is detected during the enable signal is HIGH. Therefore, the enabled period is longer when we use more larger division number. Counter_in1 is the output of the divide-by-4 divider which has the input of Sig1 and Counter_in2 is the output of the divide-by-4 divider which has the input of Sig2. Two counters also have enabled node same as the divide-by-4

divider, and inputs the same window signal. The three-types of window signal were shown in the bottom of Fig. 3. The window is widest when the division number is 64 for the flexible divider. As shown in Fig. 2, since the divider and the counter are disabled for a long time, i.e., the disabled time is much longer than the enabled time, the power consumption of the proposed frequency discriminator is very small.

Fig. 3 shows the waveforms of Window and Counter in 1 to show the detail operation of the divde-by-4 divider in the proposed counter-based frequency discriminator to detect the concentration of the fine dust. When the window signal is LOW, the divide-by-4 divider and the 20-bit counter is enabled. Then, the counter counts the number of rising edges of the input signal, Counter_in1 and Counter_in2, which are

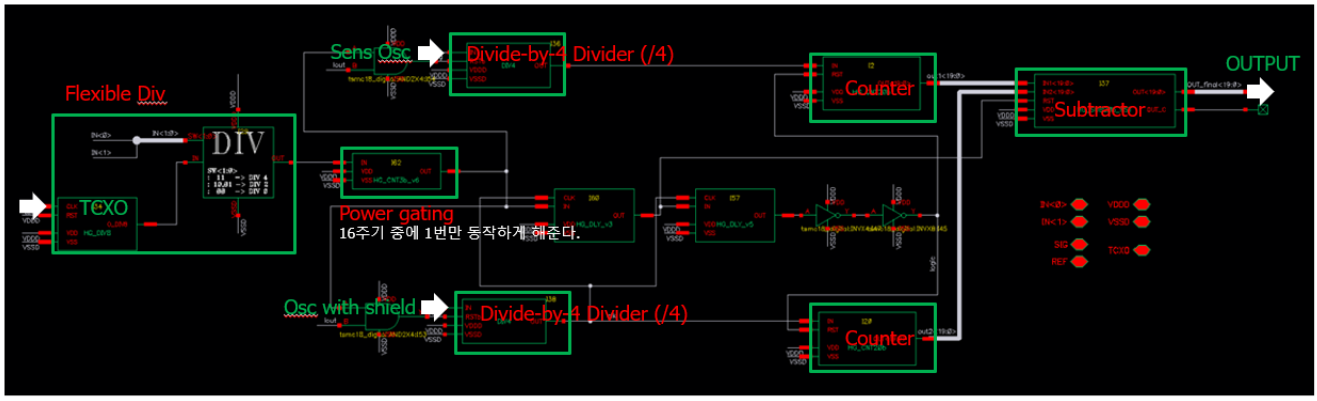


Fig. 4. Cadence schematic diagram of the proposed frequency discriminator

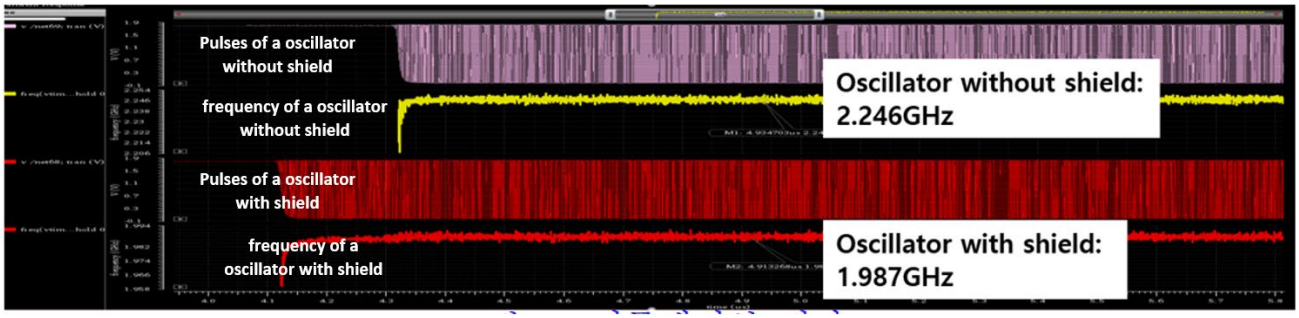


Fig. 5. Simulated waveform and frequencies of oscillators with shield and without shield

❖ Power consumption: 284.2uW

❖ Layout area with the pins' location

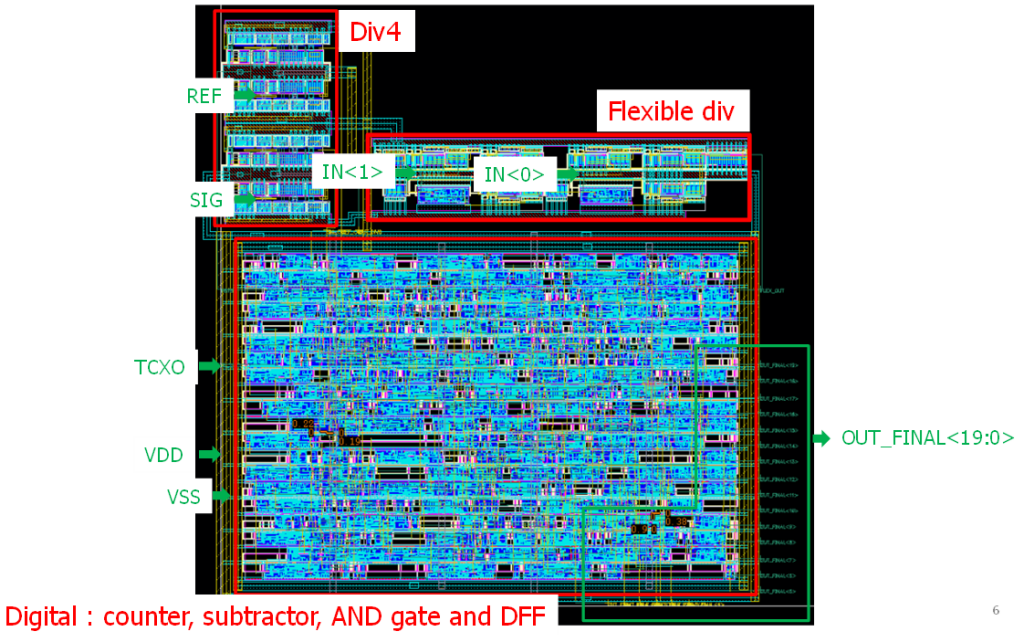
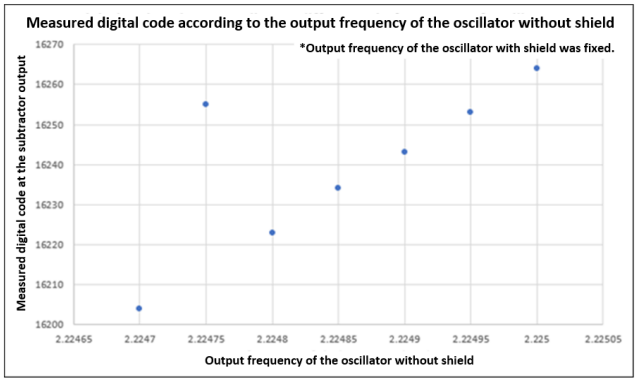


Fig. 6. Layout result of the proposed counter-based frequency discriminator

the outputs of divide-by-4 dividers. Then, if the output frequency of the oscillator increases, the number of rising edges of Counter_in1 or Counter_in2 increases, which results in an increase in the output code of the counter. The output code of the counter is sampled at the rising edge of the window signal. Then, by sample the result of the subtractor, we can find the concentration of the fine dust. Table I shows the target specification of the proposed fine dust discriminator. The target center frequency for detecting the fine dust is 2 GHz. The target resolution for dust detection is 50 kHz. The frequency deviation due to the fine dust is from 3 to 5 MHz. The expected process variation of the frequency is from 1.6 to 2.4 GHz. Fig. 4 shows the schematics of the proposed frequency discriminator in Cadence virtuoso. Between the power gating circuit and the counter, a few inverters were added to match the clock timings.

Fig. 5 shows the simulated waveform and frequencies of oscillators with a shield and without shield. The output frequency of the oscillator with a shield is 1.987 GHz. On the other hand, the output frequency of the oscillator without a shield is 2.246 GHz. It's because that since the concentration of the dust is very low, the frequency of the oscillator without shield is much higher compared to the output frequency of the oscillator with shield.



foffset	Digital Code Difference
50kHz (Measured)	10.18
4.9kHZ (Calculated from measured)	1

Fig. 7. Measured digital output code according to the input frequency

III. RESULTS AND DISCUSSION

Fig. 6 shows the layout result of the proposed counter-based frequency discriminator. The chip area is 0.06 mm^2. REF node is the input signal from the oscillator with shield and SIG node is the input signal from the oscillator without a shield. (Note that this layout doesn't contain two oscillators, and those MEMS oscillators were attached on PCB board.) IN<1:0> were digital code, which controls the division number of the flexible divider. Here, if IN<1:0> is 00_2, the division number is 16 and if IN<1:0> is 10_2, the division number 64. TXCO is the input node from the TCXO. The synthesized digital circuit consists of the counter, the subtractor, the AND gate and the DFF. The total power consumption of the divide-by-4 divider, the flexible divider, and the synthesized digital circuit was 284.2 μW.

Fig. 7 shows the measured output digital code according to the input frequency. The output code is from the output of the subtractor. When the frequency of the oscillator with shield was fixed and the frequency of the oscillator without shield was varied according to the concentration of the fine dust, the output digital code was changed. As shown in Fig. 7, the output digital code was proportional to the output frequency of the oscillator with shield. The below table in Fig. 7 shows the measured resolution according to the graph in the top of Fig. 7. When the frequency was changed by 50 kHz, the output digital code was changed by 10.18. As a result, the measured resolution was 4.9 kHz/bit, which means that when the output frequency was changed by 4.9 kHz by the variation of the concentration of the fine dust, the digital code would be changed by 1.

IV. CONCLUSION

The proposed frequency discriminator was implemented with a simple counter-based architecture. Except dividers (divide-by-4 dividers and flexible dividers), other blocks are all synthesized, thus, it achieved extremely small area. To increases the resolution of the frequency discriminator, we used the flexible dividers with a window signal having long period. The proposed frequency discriminator in 180-nm CMOS process consumes only 0.3 mW of power in total. Thanks to the high interactivity and low-power architecture, which can reduce the battery size of the sensor, the proposed frequency discriminator is a good candidate for the fine dust sensor market.

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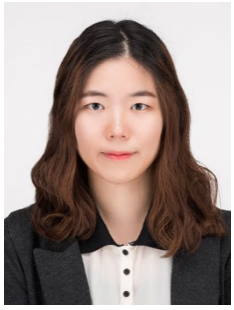

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