A 17.5 GHz VCO with 1/4 Frequency Divider Chain Based on 65-nm CMOS Technology

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Abstract **- In this work, a 17.5-GHz voltage-controlled oscillator (VCO) integrated with a frequency divider chain of 1/4 division ratio has been designed based on a 65-nm CMOS technology. The VCO is implemented as a LC cross-coupled structure, which includes a 2-bit capacitor bank and switches for coarse frequency tuning and varactors for continuous tuning. The frequency divider chain is composed of a current-mode logic (CML) /4 frequency divider, CML-to-CMOS converter, and 50-Ω driver. The VCO exhibits a frequency tuning range from 16.3 GHz to 20.8 GHz, with -11.3-dBm output power at the center frequency of 17.5 GHz. The frequency divider chain converts the VCO oscillation frequency down to 4.4 GHz with an output power around 0 dBm. The total DC power consumption is 23.8 mW, and the circuit size including the pads is 600 × 700 mm².**

Keywords**—65-nm CMOS, Capacitor bank, Current-mode logic, Frequency divider, VCO**

I. INTRODUCTION

The frequency range over 100 GHz has been attracting lots of interests in various applications due to the wider frequency bandwidth that can be provided [1]. High data-rate communication systems [2] and high-resolution radar systems for short range imaging and gesture scanning have been developed in this frequency range [3], [4]. The key component of these systems is a signal source that can be modulated. However, for frequency ranges over 100 GHz, it is challenging to generate a modulated signal because of the issues related to phase mismatch and/or low Q-factor of passive components. Especially, the low Q-factor is a main cause of the phase noise degradation. For these reasons, high-frequency radar systems conventionally employ a frequency synthesizer operating in a relatively low frequency band, typically around 15 GHz, which is subsequently upconverted to the desired high frequency range using a frequency multiplier [5], [6]. This configuration benefits from the phase noise performance available, while providing a wide frequency bandwidth owing to the low intrinsic phase noise

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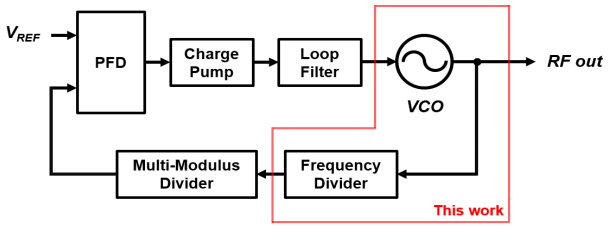


Fig. 1. Conceptual block diagram of the conventional frequency synthesizer.

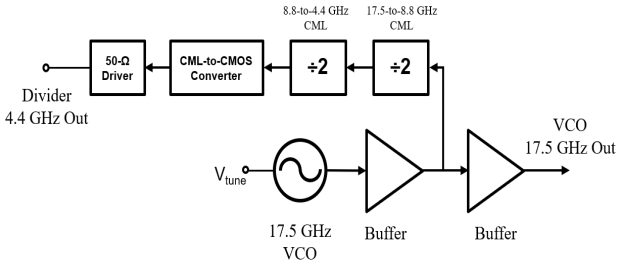


Fig. 2. Block diagram of the 17.5-GHz VCO integrated with frequency divider.

of the frequency multipliers [7]. Hence, developing frequency synthesizer around K- or Ku-band frequency band is essential to generate the high-quality signals for systems operating over 100 GHz.

A conceptual diagram of the conventional frequency synthesizer which provides frequency modulation is depicted in Fig. 1. The signal generated by the voltage-controlled oscillator (VCO) is injected to the frequency divider, and the divided signal passes through the multi-modulus divider that provides additional frequency division as well as frequency modulation. For the remaining part of the frequency synthesizer, standard components needed for charge pump phase-locked loops (PLLs) are included such as phase-frequency detector (PFD), charge pump, and loop filter. This work is focused on the implementation of a VCO integrated with a frequency divider chain, which serves as a core element of a complete frequency synthesizer operating at 17.5 GHz. The circuit is composed of a VCO, two frequency dividers, and a CML-to-CMOS converter with a 50-ohm driver, as shown in Fig. 2. The simulation results of each circuit component and the integrated circuit are presented in this work.

The remaining part of this paper is composed of following sections. Section II describes the circuit design of the 17.5-GHz VCO while the main results with the frequency divider

and CML-to-CMOS converter are described in Section III and IV, respectively. The main results with the full integrated circuit is presented in Section V. Lastly, the conclusion is given in Section VI.

II. 17.5-GHz VCO

The designed VCO is composed of two parts: an oscillator core and a cascaded buffer. The buffer is included to improve the isolation between the oscillator core and the subsequent circuit as well as to ensure the intended oscillation frequency. As shown in Fig. 2, the output of the VCO is branched into two paths, one leading to the frequency divider and the other taken as the output of the entire circuit. The path to the frequency divider is connected to the output of the first buffer for isolation from the oscillator core, while the circuit output is taken after the second buffer to enhance the isolation between the frequency divider and the output. The isolation provided by the buffer in terms of S_{21} is -24.4 dB at 17.5 GHz by simulation, although a large-signal isolation will be more relevant in practice.

A. Oscillator with 2-bit capacitor bank

Fig. 3 depicts the 17.5-GHz VCO core design. It is implemented based on the conventional LC cross-coupled structure, with a tail transistor, M_3, to provide a stable current bias of the oscillator. A pair of varactors are included for frequency tuning of the VCO. Its capacitance is varied from 36.5fF to 177fF by adjusting V_{tune}, leading to the change in the core capacitance as well as the oscillation frequency of the circuit. To achieve a wide frequency tuning range, the size of varactors was determined large enough, although its Q factor was limited below 10 with the selected size. Also included for additional frequency tuning is the 2-bit binary weighted capacitor bank: C_3, C_4 with 28.8fF, and C_5, C_6 with 57.1fF. The 2-bit capacitors are linked by switches that can be on and off depending on the tuning requirement. Each switch is implemented by the same structure, which is presented in Fig. 4. For enhanced switching operation, the size of M_5 was determined large enough (10 μm) to reduce the on-resistance. Those of M_6 and M_7 were selected small (200 nm) to set the bias at the nodes X and Y through the high on-resistance (about 1.5 kΩ) when switch is turned on [8]. The 2-bit binary weighted capacitors can provide four different states of coarse tuning of the oscillation frequency, each state being further tuned by V_{tune}, to compensate for any frequency shift caused by process, voltage, temperature (PVT) variation or other parasitic components [9]. In this way, the varactor and the capacitor bank collaboratively work to provide a wide tuning range with preferred performance. A pair of inductors, L_1, L_2, are implemented with a spiral structure as shown in Fig. 5(a). Their peak Q factor was above 15, as confirmed by electromagnetic (EM) simulation shown in Fig. 5(b) along with the inductance value, for which ADS momentum was used.

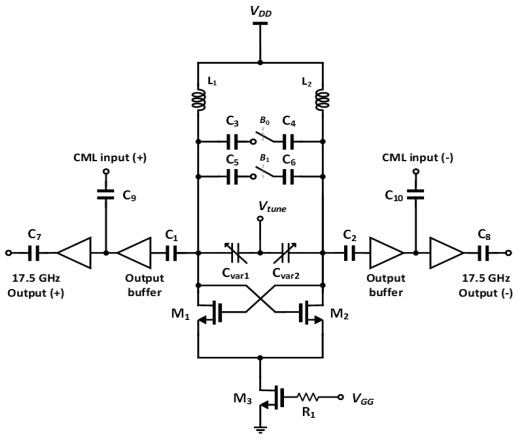


Fig. 3. Schematic of the 17.5-GHz VCO.

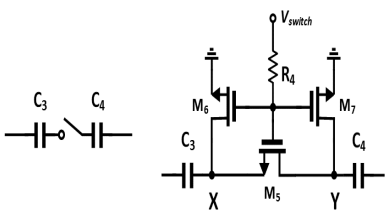
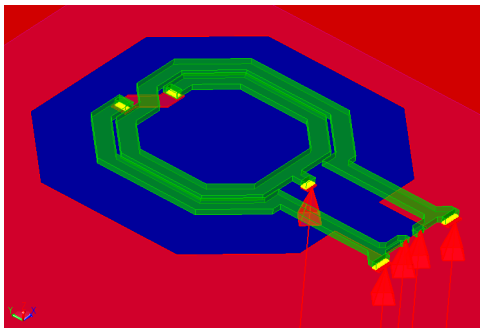
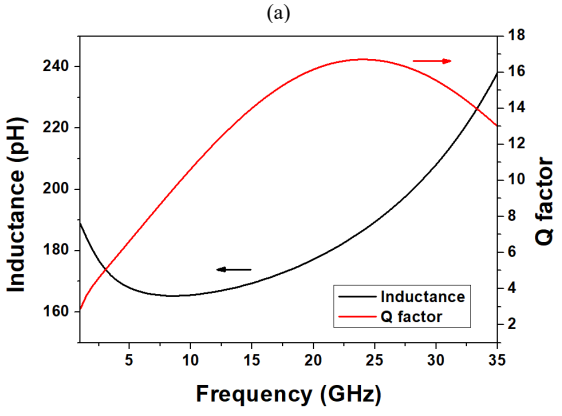


Fig. 4. Schematic of the capacitor bank switch.

Fig. 6 depicts the simulation result of the designed VCO. The tuning range of the oscillation frequency is from 16.3 GHz to 20.8 GHz. For each capacitor bank control bit, B_0 and B_1, a frequency tuning of 2.5 GHz - 3 GHz is obtained as V_{tune} is varied from 0 V to 1.5 V. For a fixed V_{tune}, the step frequency shift with the control bit changes is 0.6 GHz. FoM (Figure of Merit) and FoMT (FoM with Tuning range) of the VCO was -175.2 dBc/Hz and FoMT = -182.9 dBc/Hz, respectively, by simulation.



(a)



(b)

Fig. 5. (a) Structure of the spiral inductor (b) Simulated performance of the inductor.

B. Resistive Load Buffer

As mentioned previously, the output buffer enhances the isolation between the oscillator core and the output or other circuits. The conventional output buffer is typically implemented by common-source stage with an inductive load to drive a 50-Ω output port with sufficient output power. However, designing inductive load around 17.5 GHz needs a large chip area. For this reason, in this work, a resistive load was applied to the output buffer for small area at the cost of gain or output power, which also involves a simpler design compared to the inductive load.

To improve the isolation between the oscillator core and the output node as well as the CML divider input, a 2-stage buffer was employed as mentioned earlier. Both stages employ the same structure as shown in Fig. 7, which is a simple common-source stage with a resistive load. As presented in Fig. 8, the simulated output power of the VCO is from -12 dBm to -11 dBm when V_{tune} varies with different capacitor bank control bits. As explained before, the output power is degraded due to the resistive load buffer, but the low output power can be compensated by subsequent circuits such as an amplifier or input buffer. The output power decreases with the low control bit numbers, as the gain of the output buffer is decreased as the oscillation frequency increases.

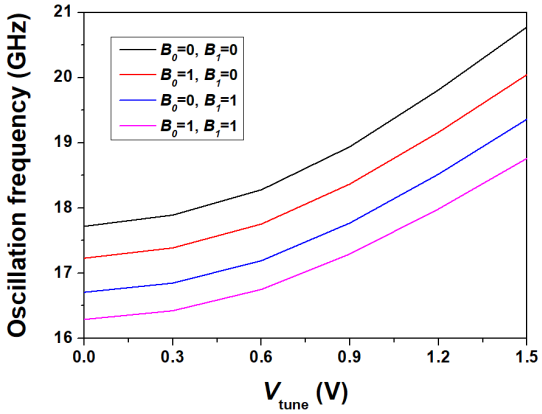


Fig. 6. Simulated oscillation frequency of the VCO

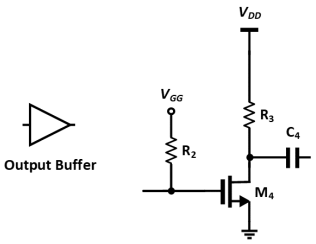


Fig. 7. Schematic of the resistive load buffer

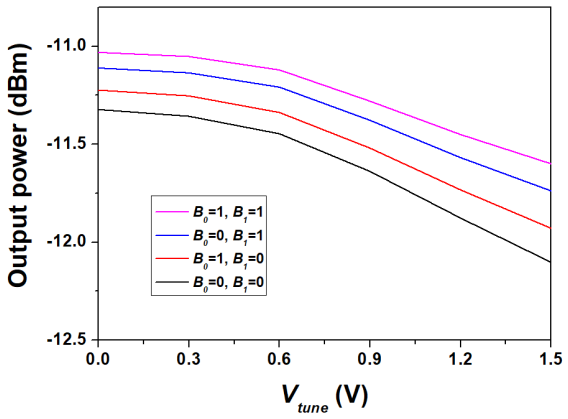


Fig. 8. Simulated output power of the VCO

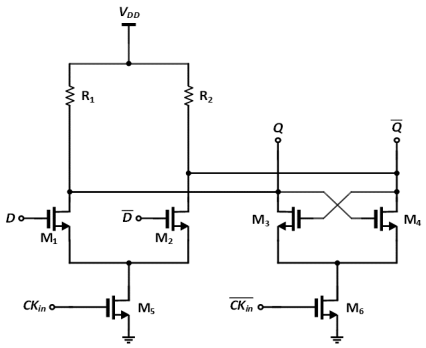


Fig. 9. Schematic of the CML D-latch

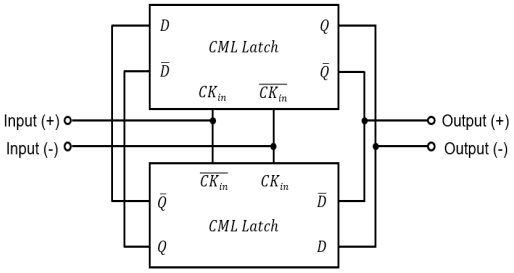


Fig. 10. Block diagram of the CML frequency divider

III. FREQUENCY DIVIDER

For high-speed frequency dividers, a current-mode logic (CML) structure is conventionally utilized because of its advantages such as fast switching and wide input frequency range [10]. In this work, two identical CML latches are cascaded in a master-slave configuration to form a /2 frequency divider. The circuit schematic of the latch is shown in Fig. 9. The block diagram of the frequency divider composed of the two latches is given in Fig. 10. Furthermore, a CML divider benefits from large voltage swings available with the positive feedback of the latch, which was also utilized in the designed frequency divider. Two frequency dividers, 17.5-to-8.8 GHz divider and 8.8-to-4.4 GHz divider, are cascaded in the design, which were implemented with the same topology, only difference being the size of the transistors and resistors included in the circuits.

Typically, CML dividers are driven by the input rail-to-rail differential swing. However, the output swing of the VCO buffer in this work that drives the CML divider is not large enough. Therefore, to ensure a stable switching operation of the first divider (17.5-to-8.8 GHz divider), a DC block capacitor was inserted, and an external gate bias was applied to the CML divider input (gate of M_5 and M_6) so that the CML divider operates in the class-AB biasing [11]. The bias level of the input transistors, M_5 and M_6, of the second divider (8.8-to-4.4 GHz divider) was determined by the output voltage level of the preceding divider. Hence, for the

second divider, the chip area can be saved because the DC block capacitor can be omitted. On the other hand, if the bias is not applied to the second divider properly, it is possible that the entire divider chain does not operate. Therefore, for proper operation, the transistor size and the resistor values must be chosen with enough margins for the bias levels. As for the cross-coupled pairs in the latch shown in Fig. 9, M_3 and M_4 are smaller than M_1 and M_2, thus contributing relatively small capacitance at the output node [12].

The layout of the CML divider chain, which consists of 17.5-to-8.8 GHz divider and 8.8-to-4.4 GHz divider, is presented in Fig. 11. Special care was taken to maintain the symmetry in the layout. Fig. 12 shows the simulated sensitivity curve of the CML divider chain, for which post-layout simulation was performed for accurate RC extraction. The input voltage swing of the CML divider was about 330 mV_{pp} (-5.6 dBm, single-ended), which would allow a locking range wide enough to match the frequency tuning range of the designed VCO that drives the frequency divider.

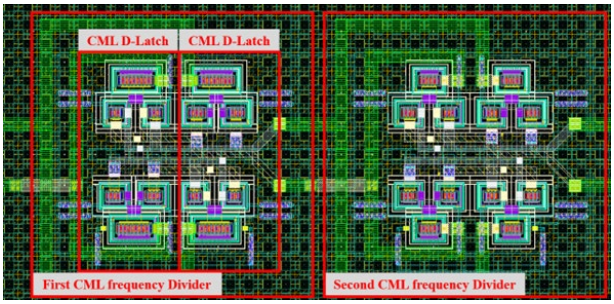


Fig. 11. Layout of the CML divider chain

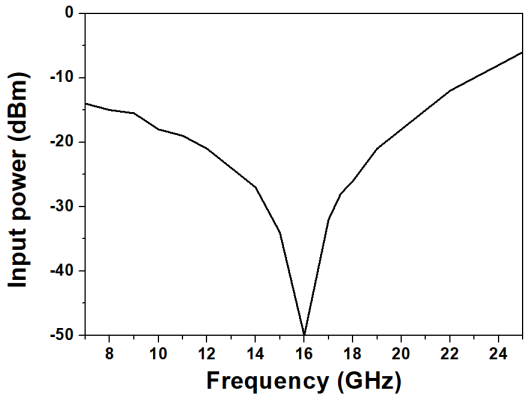


Fig. 12. Simulated sensitivity curve of the CML divider chain

IV. CML-TO-CMOS CONVERTER WITH A 50-Ω DRIVER

Typically, a CML-to-CMOS converter is employed to convert the current-mode circuit to static CMOS circuit which is driven by a voltage level. Thus, a CML-to-CMOS converter follows the CML divider chain to drive the 50-Ω driver that is implemented as a pair of inverters cascaded as shown in Fig. 2. The CML-to-CMOS converter in this work mainly serves to boost the voltage swing and set the required common-mode voltage level, so that the 50-Ω driver can easily drive the signal.

Fig. 13 shows the schematic of the CML-to-CMOS converter, which is basically a push-pull OP-Amp structure with a differential output. Also shown in Fig. 14 is the schematic of the 50-Ω driver, which is a 2-stage inverter chain with resistive feedback. A large value (10 kΩ) was selected for the resistors to sufficiently isolate the input and output signals while enforcing the same common-mode levels for the input and output. For the 50-Ω driver, tapered size was employed where a larger size was employed for M_3 and M_4 than M_1 and M_2, an effort to drive the signal efficiently [13].

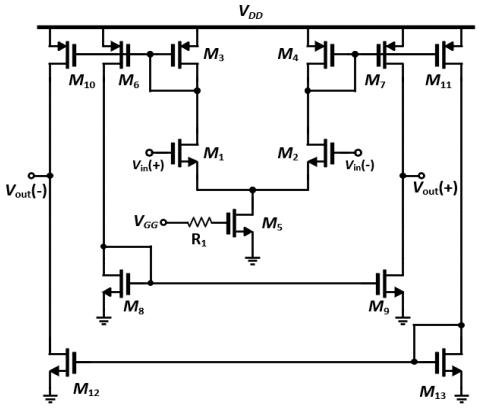


Fig. 13. Schematic of the CML-to-CMOS converter.

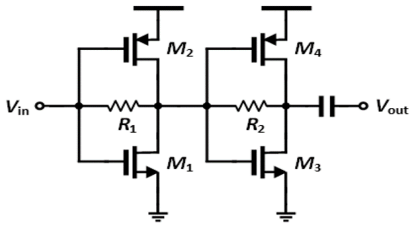


Fig. 14. Schematic of the 50-Ω driver.

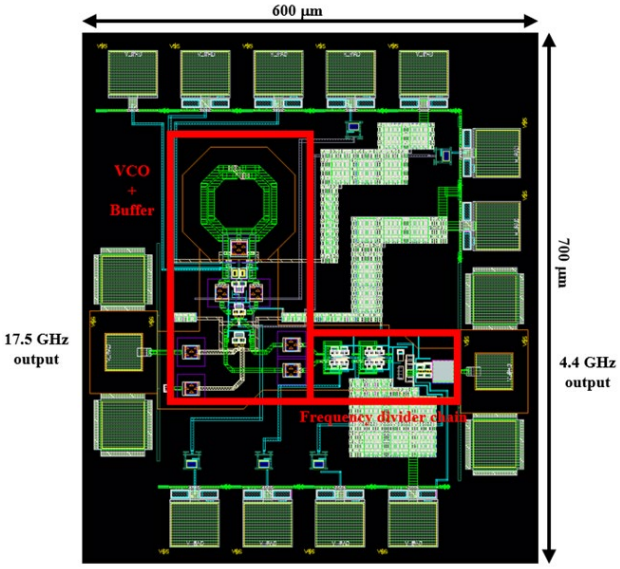
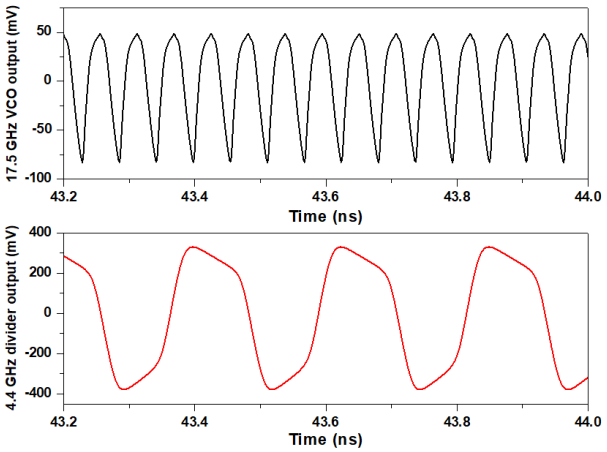


Fig. 15. Layout of the VCO integrated with the frequency divider chain

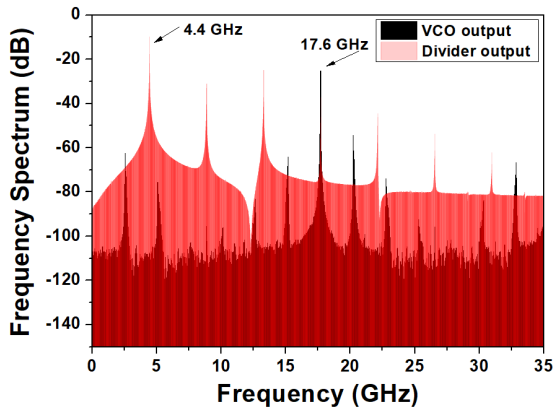
V. INTEGRATED VCO-FREQUENCY DIVIDER CHAIN

The circuit components described in the previous sections, namely the VCO with a 2-stage buffer, CML frequency divider, CML-to-CMOS converter, and 50-ohm driver, have been integrated to form an integrated VCO-frequency divider chain. Fig. 15 shows the layout of the entire circuit integrated, which also includes the pads and bypass capacitors. The total area is 600 μm × 700 μm.

Transient simulation was performed for the waveform at the output of the VCO and the frequency divider, for which V_{tune} and capacitor bank control bit were fixed. The results shown in Fig. 16(a) confirm that the divider chain divides the VCO output signal by 4 as intended, and its output power is estimated to be over 0 dBm. The frequency domain spectrum profile of the output obtained from the Fast Fourier Transform (FFT) of the transient simulation result is presented in Fig. 16(b). It clearly shows the two peaks at 17.6 GHz (VCO output) and 4.4 GHz (frequency divider output) with sufficient suppression of adjacent harmonics. The total power consumption of the entire circuit is 23.8 mW, which is divided into 14.3 mW and 9.5 mW for the VCO and the divider chain, respectively.



(a)



(b)

Fig. 16. Simulation result of the VCO and the frequency divider: (a) Time-domain transient simulation (b) Frequency-domain spectrum converted from the transient simulation by FFT

VI. CONCLUSIONS

A 17.5 GHz VCO integrated with a frequency divider chain of 1/4 division ratio, which consists of two CML divider, CML-to-CMOS converter, and 50-Ω driver, has been designed in this work based on a 65-nm CMOS technology. The VCO exhibits a tuning range from 16.3 GHz to 20.8 GHz, which was realized with a capacitor bank and a varactor tuning. The frequency divider converts the oscillator frequency of the VCO down to around 4.4 GHz. Total power consumption of the entire integrated circuit is 23.8 mW. The circuit can be applied to a K- or Ku-band PLL and frequency synthesizer, which will serve as a modulated signal source for various high-frequency systems including broadband communication and radar systems.

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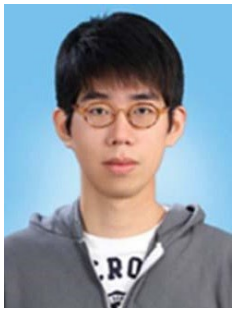

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His current research interests include high-speed wireless transceivers for communication applications and ultra-wideband transceivers for user-defined radio system application.

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Prof. Rieh was a recipient of IBM Faculty Award (2004) and a co-recipient of IEEE EDS George E. Smith Awards (2002 and 2006) and IEEE Microwave and Wireless Component Letters Tatsuo Itoh Best Paper Award (2013). He has served as an Associate Editor of the IEEE Microwave and Wireless Components Letters (2006-2009) and the IEEE Transactions on Microwave Theory and Techniques (2010-2013). He is the author of the book, "Introduction to Terahertz Electronics (Springer, 2021)".