An Output Capacitor-less LDO with a Fast Transient Response using Two Positive Feedback Loops

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***Abstract* – This paper proposes an output capacitor-less low-dropout regulator (LDO) with a fast-transient response. The proposed LDO can have fast transient response by using positive feedback loops which are implemented by the simple change from a conventional structure. In addition, the proposed LDO designs negative feedback loops with RC high pass filters which rapidly reflect output voltage variation to achieve the fast-transient response. The total compensation capacitance is 7.8 pF. The maximum load current supplied by the LDO is 100 mA and it consumes static current of 9 µA. The proposed LDO has been implemented in 0.18 µm CMOS technology and the active chip area is 0.0146 mm^2.**

***Keywords*—Capacitor, Fast transient response, Low-dropout regulator (LDO)**

I. INTRODUCTION

As the functions required for mobile devices have recently increased, power management integrated circuit (PMIC) is becoming more important. PMIC converts a battery voltage into a various voltage required by each module. Since the battery voltage decreases over time, PMIC which should constantly supply the voltage required for each module, is required.

There are various types of circuits in PMIC, such as low-dropout regulator (LDO), DC-DC converter, and charge pump. They each have their own strengths and weaknesses. Among them, LDO has its great advantage of simplicity of structure. However, power efficiency of the LDO is lower than other types of PMICs because its power efficiency is directly determined by input and output voltages ratio, while input and output voltages ratio almost does not affect to the power efficiency in other types of PMIC. Nevertheless, LDO has been widely used owing to the simple structure, regardless of the low efficiency.

As many functions are added in mobile devices, the size of ICs has recently been reduced compared to the previous one due to the trend that more devices should be embedded into the limited area. If external components such as capacitors and inductors are used, they are wasted in terms of area, which is directly related to cost waste. Accordingly, research on PMIC from which external devices have been removed is being conducted, and this trend is also shown in LDO studies [1] – [8]. Research is being conducted on capacitor-less LDO in which output capacitors are removed from existing LDO, which has the advantage of reducing a significant area. However, referring to the papers published so far, it is true that the performance is insufficient compared to LDO of which capacitors exist externally. This paper proposes capacitor-less LDO to compensate for these shortcomings. The chapter II explains the design of the proposed LDO. The simulation results are explained in chapter III and conclusion is discussed in chapter IV.

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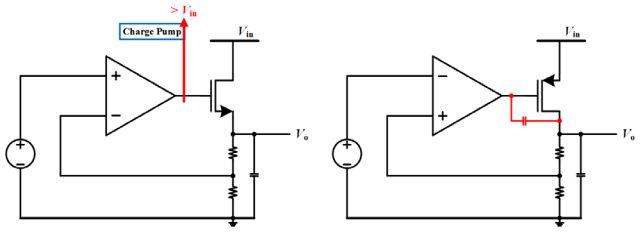
II. AN OUTPUT CAPACITOR-LESS LDO WITH A FAST TRANSIENT RESPONSE

A. Conventional LDO

Fig. 1. shows the basic LDO structure. The LDO structure consists of error amplifier and main transistor, and the main transistor can be configured as NMOS or PMOS. The main transistor is an important in efficiency and circuit design.

Looking at the NMOS structure in Fig. 1. (a), the output impedance of the NMOS is small ($1/g_m$), and the dominant pole is present at the gate of the main transistor. Therefore, it is easy to secure stability. However, since a gate voltage of the main transistor (NMOS) must be higher than output voltage (V_o) as much as a threshold voltage (V_{th}), the gate voltage of the main transistor (NMOS) must be higher than input voltage (V_{in}) to make the dropout voltage small, so an additional charge pump is required.

At PMOS structure shown in Fig. 1. (b), it becomes a 2-pole system on V_o and gate nodes, because of the capacitance of the main transistor (PMOS). There is a risk of oscillation depending on the load conditions, so it is important to pay attention to the compensation. However, since the gate voltage should be lower than that of the NMOS shown in Fig. 1. (a), it is easier to be implemented. In this paper, according to this advantage, the proposed LDO is designed by using PMOS structure shown in Fig. 1. (b).



(a) (b)

Fig. 1. Basic schematic of a LDO regulator (a) NMOS (b) PMOS

Fig. 2. shows the presence or absence of output capacitor in the basic LDO structure. Since LDO is a circuit mainly composed of negative feedback, stability is very important. In addition, without an external output capacitor, it is difficult to minimize a peak or drop of V_o because the feedback loop only deals with the peak or drop at the transient response. Although, it has the demerits if the output capacitor is not used, the chip size becomes smaller and costs are also reduced. Therefore, considering these advantages, the proposed LDO is designed as capacitor-less shown in Fig. 2 (b).

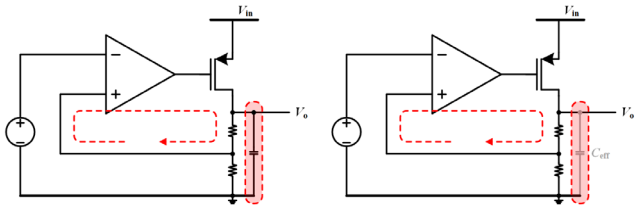


Fig. 2. Basic schematic of an LDO regulator (a) capacitor (b) capacitor-less

B. Proposed LDO

Fig. 3. shows the schematic of the basic LDO. It consists of an error amplifier and a main transistor, PMOS. Because of the PMOS main transistor, the circuit has a 2-pole at a lower frequency than its unity-gain frequency (UGF), so miller compensation is applied by C_3 and R_3.

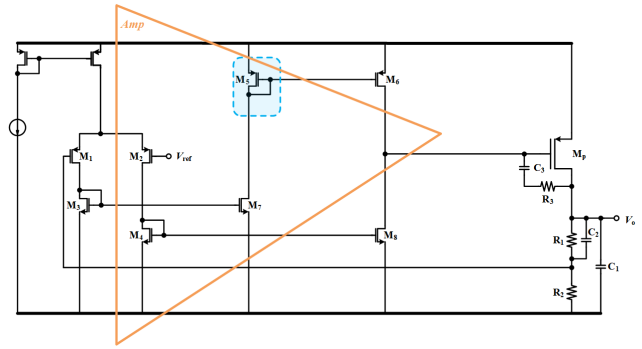


Fig. 3. Original schematic of a capacitor-less LDO regulator

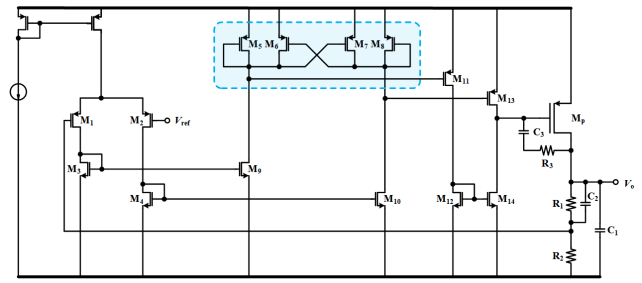


Fig. 4. Previous schematic of a capacitor-less LDO regulator

Fig. 4. is a structure in which transistors are added to increase the impedance of M_5, $1/g_{m5}$, shown in Fig. 3. The gain increases since the impedance increases from $1/g_{m5}$ to $1/g_{m5}$-g_{m6}. The simulation of the circuit in Fig. 4 is shown in Fig. 5.

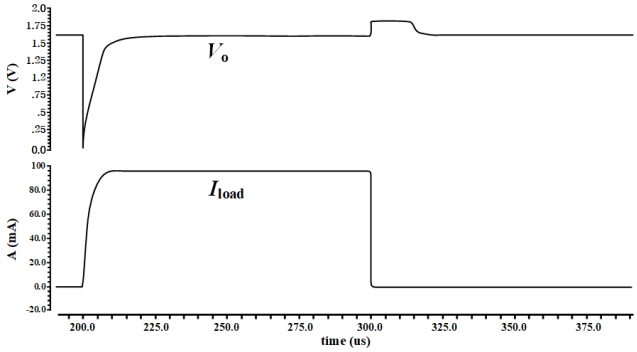


Fig. 5. Simulation of a previous schematic LDO regulator

Although the gain of LDO increases owing to the impedance increment, it barely improves the transient response. Since the capacitor-less LDO has no external capacitor at its output, the fast transient response is one of the most important characteristics of the LDO. The main reason of the slow transient response of circuit shown in Fig. 4 is charging and discharging currents for the gate node of main PMOS transistor is limited by a tail current. Therefore, to improve transient performance, charging and discharging the parasitic capacitor of the gate node of the PMOS main transistor should be improved. To achieve this, there are two ways, reducing the capacitor size or increasing the current. However, since the capacitor size is fixed, a method of increasing current is selected. Adding high impedance node or positive feedback can be method for this. Adding high impedance node increases the overall gain of the LDO, while making it difficult to compensate. So, in this paper, adding positive feedback that does not implement the addition of gate stage is selected.

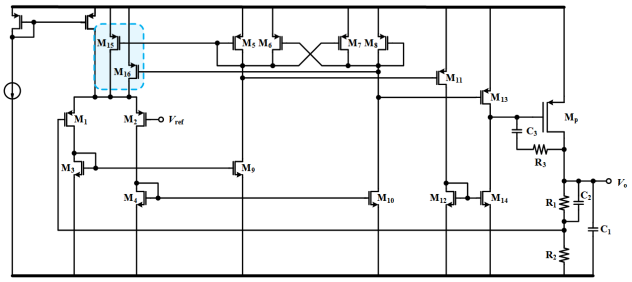
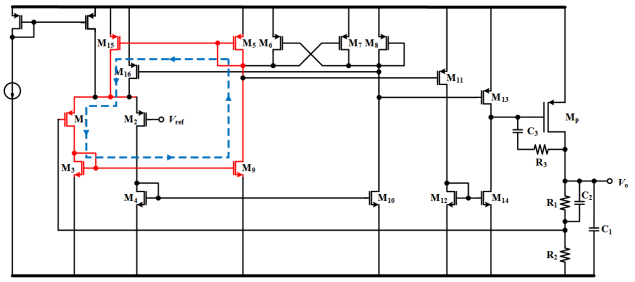


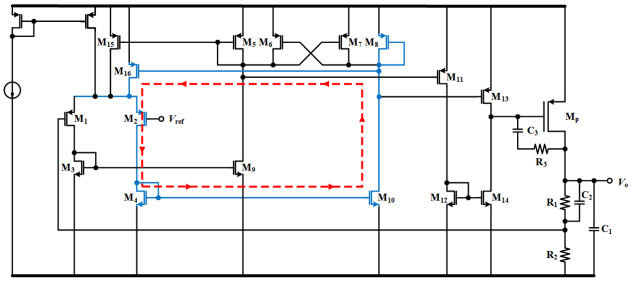
Fig. 6. Modified schematic of an LDO regulator

Fig. 6. is a circuit that constitutes positive feedbacks by simply adding two transistors, M_{15} and M_{16}, to the circuit of Fig. 4. When two transistors are added and configured like tail currents, two positive feedback loops are created, which allow the current to be dynamically pushed and pulled to the gate node of main PMOS transistor, resulting in a faster

Positive feedback loops which are composed by M_{15} and M_{16} are shown in Fig. 7. The positive feedback loop composed by M_{15} is shown in Fig. 7 (a) and it dynamically increases discharging current to the gate node of the main PMOS transistor through M_{14}. Likewise, the positive feedback loop composed of M_{16} is shown in Fig. 7 (b), and it dynamically increases charging current to the gate node of the main PMOS transistor through M_{13}.



(a)



(b)

Fig. 7. Two positive feedback loops in the circuit of Fig. 6.

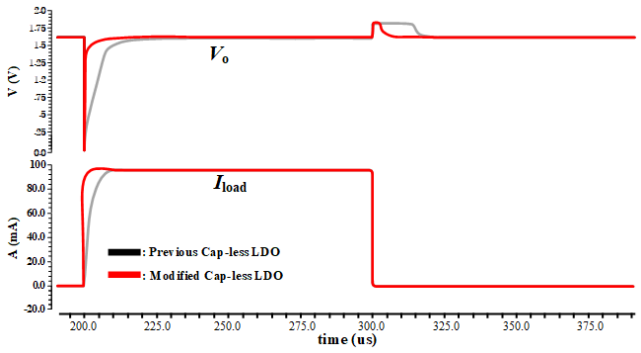


Fig. 8. Modified LDO regulator simulation

Fig. 8. is the simulation waveform of the circuit of Fig. 7. Owing to the positive feedback loops, the tail current could be greatly increased in transition. Therefore, LDO achieves a shorter settling time as red waveforms in Fig. 8. However, there is still problem especially when load current changes from light to heavy. In general, V_o of LDO is close to V_{in} for a high efficiency. So, V_o peak is not a huge problem when load current changes from heavy to light because the V_o peak is limited to V_{in}. On the other hand, when load current changes from light to heavy, V_o drops to considerably low level which could cause a mal-function of the load. Therefore, it is important to reduce not only the settling time but also the V_o drop in this situation.

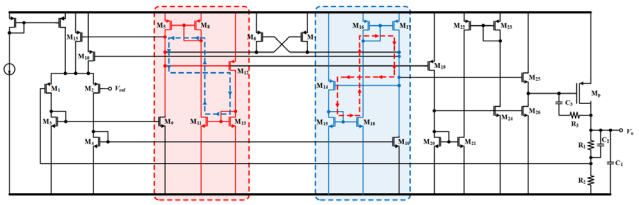


Fig. 9. Modified schematic of an LDO regulator

To reduce the V_o drop, the circuit shown in Fig. 7 is modified to the circuit shown in Fig. 9. This circuit transforms the diode-connected transistors of M_5 and M_8 of Fig. 7 into negative feedback structures. At the frequency range of which gain of these negative feedback structures are maintained, these feedback structures operate as diode connected transistors. On the other hand, at the frequency range higher than a UGF of the feedback structures, these feedback loops cannot be considered as diode connected transistors but as high impedance nodes. By using this dynamic high impedance nodes, the LDO could further increase charging and discharging current to the gate node of main PMOS transistor in transition.

With these negative feedback structures, the proposed LDO additionally uses RC high pass filters, which are composed of R_4+1/g_{m29} with C_4 and R_5+1/g_{m30} with C_5, to reduce the V_o drop further as shown in Fig. 10. This technique has been widely used because of its effectiveness. Since RC high pass filter has a considerably short time delay for the high frequency signal, it could transfer V_o drop and peak information to the LDO without almost zero delay. Owing to this technique, the proposed LDO generates significantly huge charging and discharging current to the gate node of main PMOS transistors. As a result, the LDO could reduce V_o drop and peak more. The simulation results are shown in Fig. 11. It can be identified that the settling time and V_o peak/drop reduce thanks to the aforementioned techniques.

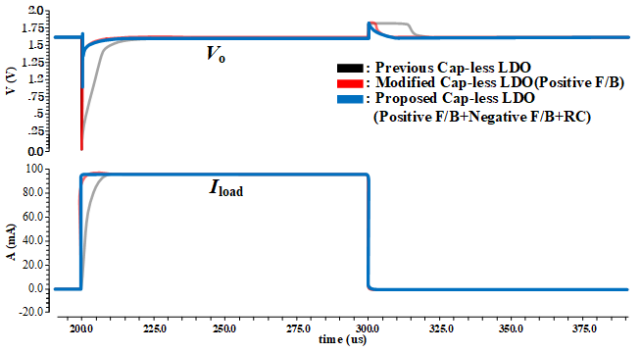


Fig. 11. Simulation of a proposed LDO regulator

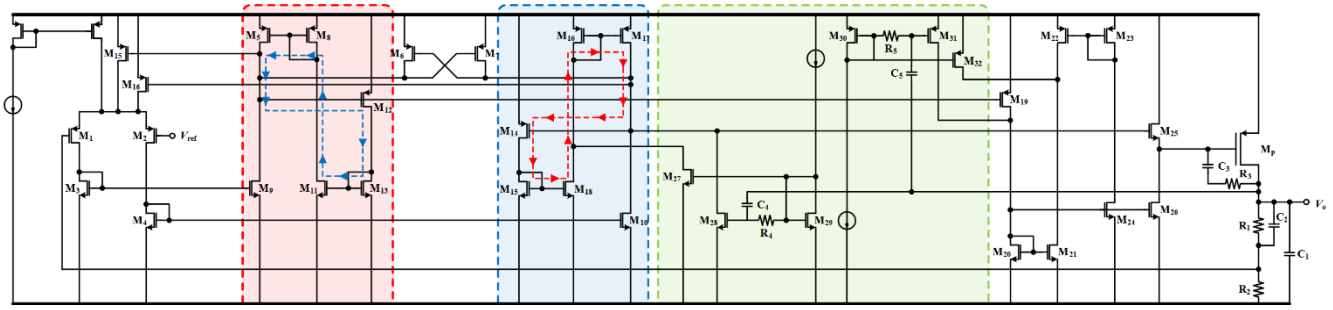


Fig. 10. Proposed schematic of an LDO regulator

III. RESULTS AND DISCUSSIONS

A. Frequency Response

Fig. 12 shows frequency response of the proposed LDO. Also, Table I summarizes the frequency responses. When the load current is 1mA, the DC gain is 81.77 dB and the phase margin is 159.415 deg. At 100mA, the DC gain is 31.887 dB and the phase margin is 99.37 deg.

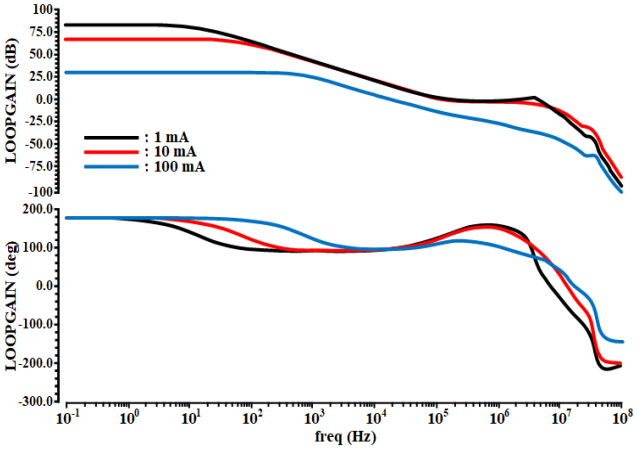


Fig. 12. Proposed LDO regulator stability response

B. PSRR

Fig. 13. shows PSRR characteristics of the proposed LDO. The values in the plot above are -111.1dB at 1Hz, -106.166Hz at 10Hz, -88.37dB at 1kHz, -33.625dB at 100kHz, and -32.75dB at 1MHZ.

At a lower frequency, the LDO achieves a sufficient PSRR while it has a deficient PRSS at a higher frequency. The reason is that when disturbance comes in, it is suppressed by feedback loop of LDO. If the loop gain of the negative feedback is large enough, it can be sufficiently suppressed by the feedback loop, however, if the gain is small, the disturbance appears even after going through the feedback loop.

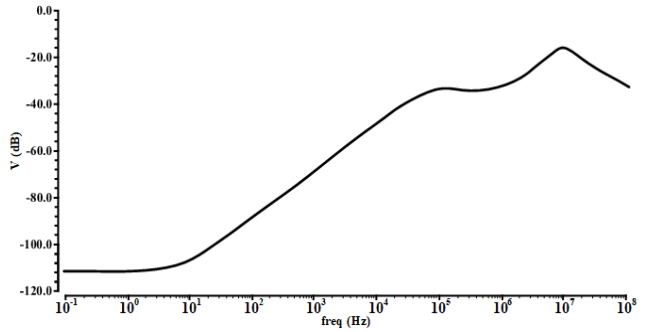


Fig. 13. Proposed LDO PSRR

C. Load and Line Regulation

Fig. 14. (a) shows the load regulation of the proposed LDO. The load regulation represents a change in the output voltage according to the change in the load current. When the load current changes from 1 mA to 300 mA, the output voltage constantly regulated. The output voltage when the load current is 1 mA is 1.599 V, when it is 100 mA is 1.594 V, and when it is 300 mA it is 1.556 V.

Fig. 14. (b) is the line regulation. The line regulation represents a change in the output voltage according to a change in the input voltage. When the input voltage is changed from 1.6 V to 1.8 V, the output voltage is constantly regulated to 1.394 V at 1.6 V, 1.393 V at 1.7 V, and 1.393 V at 1.8 V.

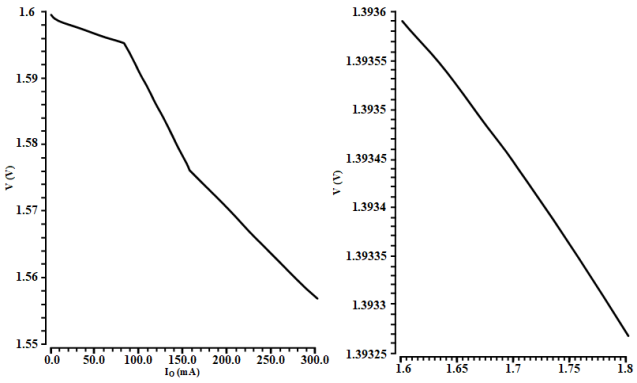


Fig. 14. (a) Load regulation and (b) line regulation of the proposed LDO

Fig. 15 is the simulation result of the line transition. As shown in Fig. 14 (b), it is stably regulated even when the input voltage is in transient situation.

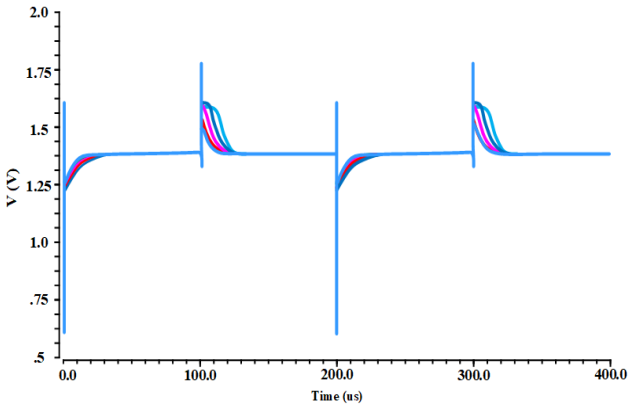


Fig. 15. Proposed LDO line transient

TABLE I. Proposed LDO regulator stability response

Parameter (load current)	1mA	10mA	100mA
DC gain	81.77 dB	67.115 dB	31.887 dB
Unity gain frequency	263.027 kHz	216.77 kHz	29.512 kHz
Phase margin	159.415 deg	124.318 deg	99.37 deg

D. Layout

Fig. 16 is the completed layout photo except for pads. The size is 557 μm × 227 μm, and the yellow part is a model of the output load as a 100 pF capacitance. Except for the load capacitor, the PMOS main transistor occupies the largest area.

TABLE II. LDO comparison table

	UNIT	[1]	[2]	[3]	[4]	This Work
Tech	μm	0.35	0.09	0.35	0.18	0.18
Active Area	mm^2	0.15522	0.019	0.053	0.04394	0.014575
Input Voltage	V	0.95 – 1.4	0.75 – 1.2	1.05 – 3.5	1.4	1.8
Output Voltage	V	0.7 – 1.2	0.5 – 1	0.9	1.2	1.594
Maximum Load	mA	100	100	50	100	100
Compensation Capacitor	pF	6	7	No	No	7.8
Current consumption (I_{bias})	μA	43	8	4.04 to 164	40	9
PSRR 1 kHz	dB	-	-44	>50 (0 Hz to 1 MHz)	51.5	-38.8
PSRR 10 kHz	dB	-	-	>50 (0 Hz to 1 MHz)	-	-19.4
PSRR 100 kHz	dB	-	-	>50 (0 Hz to 1 MHz)	36	-9.1
PSRR 1 MHz	dB	-	-	>50 (0 Hz to 1 MHz)	17	-10.96
Line Regulation	mV/V	-	3.78	1.061	-	37.136
Load Regulation	mV/mA	~0.4	0.1	0.0614	-	0.006
FOM	ns*mV	18.24242	0.940206	2.20898	12.12121	7.318182

*FOM = $T_{edge} * I_{bias} * \Delta V_O/\Delta I_{load}$

IV. CONCLUSION

Table II compares the existing papers with the proposed capacitor-less LDO. The proposed LDO is produced in the 018 CMOS process. The current consumption is on the good side, and power is like or less than the state-of-arts. The proposed LDO satisfies similar performance while having a much smaller active area than other references.

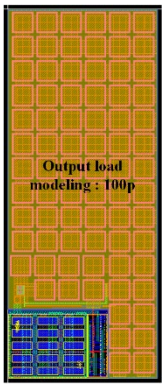


Fig. 16. Proposed layout of an LDO regulator

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