Analysis of Millimeter-Wave Power Amplifier Using Cascode Structure

Deok Young Kim
Department of Electrical & Electronic Engineering, Yonsei University
E-mail: star570@yonsei.ac.kr

***Abstract* - This paper illustrates a power amplifier design methodology used in the millimeter-wave and analyzes design issues at millimeter-wave band. The designed millimeter-wave band power amplifier is implemented in 3 stages cascade. The power amplifier consists of a drive stage using cascode and power stage to which neutralization technique is applied. we analyze how to verify the parasitic effects in the millimeter-wave band on the cascode structure of the drive stage through pre-layout and post layout simulation. The power amplifier of the millimeter-wave band was designed using the Samsung 28nm process. The simulation result of the designed power amplifier shows the saturation output power is 7 dBm and the PAE is 6.5%. In the simulation, S21 is 16.8 dB. Designed with 1 V supply, the power amplifier consumes 62 mW of DC power.**

***Keywords*—Cascode, Millimeter-wave, Parasitic, Power Amplifier (PA)**

I. INTRODUCTION

Radar systems are being used in various fields such as medical devices and radar for precise distance measurement. In particular, various types of sensors are integrated into smart sensors under complementary relationships to play the role of precise distance recognition and object recognition. The 76-77 GHz frequency band has the advantage of being a high allowable isotropic radiated power (EIRP) [1]. In addition, short-range radar is also being actively studied targeting the 77-81 GHz band, so the 77 GHz band is evaluated as a frequency band that can play many roles. Since a wide bandwidth is available, it has the advantage of being very superior to other RF radars in terms of speed resolution and precision, and since the sensor size can be much reduced, it is easy to apply to many applications. Indeed, the need for 77 GHz (1 GHz BW) for LRR and 79 GHz (4 GHz BW) for SRR is growing compared to 24 GHz (200 MHz BW) due to radar systems and output power limitations that determine precision depending on bandwidth of frequency. The existing radar was mainly composed of Frequency Modulated Continuous Wave (FMCW) radar [2]. This method is useful for obtaining physical information of speed and location degree because data are obtained based on signal processing through frequency change. However, there is considerable bottleneck to make wideband PLL, VCO, etc. In addition, it takes a long time to obtain Doppler Shift information, and it is difficult to obtain precise speed and location information [3]. Therefore, research is underway to use Impulse radar of 4GHz BW using W-band of 77 to 81GHz. Using this, autonomous driving technology among radar systems has become the most important topic in the automobile industry, and research on vehicle radar sensors necessary for it is becoming active. The vehicle radar sensor includes an SRR that detects a short distance and an LRR that detects a long distance [4]. The need for radar sensors for vehicles that utilize W-bands of 77 to 81 GHz has increased due to limitations in radar systems and output power, which determine precision depending on the bandwidth of frequencies. Therefore, the implementation of the transceiver has become very important. Fig. 1 (a), (b) shows the radar system of the proposed transceiver. The power amplifier in the mm wave band is limited in voltage swing and output due to the low supply voltage source 1V. Therefore, the proposed cascode & neutralization technique of the power amplifier maximizes output power, high gain, and stability. In the mm-wave band, the parasitic component

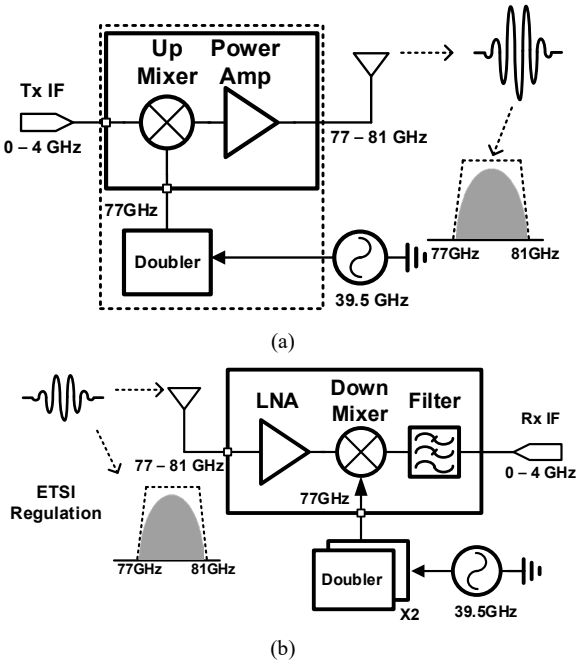


Fig. 1. Impulse radar system (a) receiver (b) transmitter

Manuscript Received Apr. 30, 2022, Revised Sep. 28, 2022, Accepted Sep. 29, 2022

of layout plays a major role in limiting the performance of the circuit, and the post layout simulation of the cascode stage adopted as the drive stage of the designed PA was analyzed to optimize the circuit performance.

II. DESIGN METHODOLOGY

A. PA circuit design

The proposed PA is shown in Fig. 2. M1 to M8 of the drive stage applied in two stages were applied as a cascode structure [5]. M9 through M12 of the power stage applied a neutralization technique [6]. It is difficult to obtain a common source structure at high frequencies and is not stable due to feedback by Miller capacitance between gate and drain [7]. To overcome the shortcomings of CS's gain and stability, the drive stage applied a cascode structure. However, it allows smaller output swings than CS structures. Therefore, it is not suitable for a power stage requiring high power and efficiency. Finally, neutralization technique was applied to the CS structure for the power stage. Neutralization is designed using a source floating transistor, such as from M11 to M12. Input/inter-stage/output

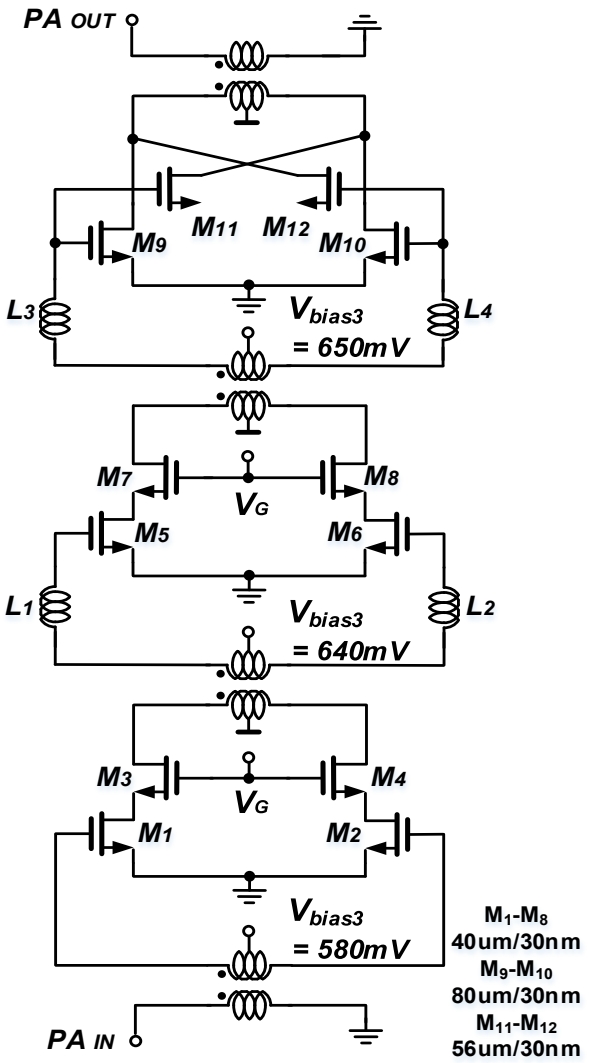


Fig. 2. 3-stage diff. cascode & CS(neutralization) transformer matched PA

impedance matching proceeds with a transformer made using sonnet, an EM simulator.

B. EM simulation and parasitic extraction

In the mm-wave band circuit design, analysis of adjacent metal effects and parasitic components of a circuit designed differently from the design at a low frequency is a method of improving the accuracy of circuit design. Fig. 3 is a layout of the proposed mm-wave PA. For accurate circuit analysis, EM simulation is performed for all areas except the transistor model. Parasitic extraction is performed because the part connected to the transistor element of the PDK model is difficult to express through EM simulation. Circuit analysis was conducted through EM simulation to confirm the effect of transformer and surrounding metal.

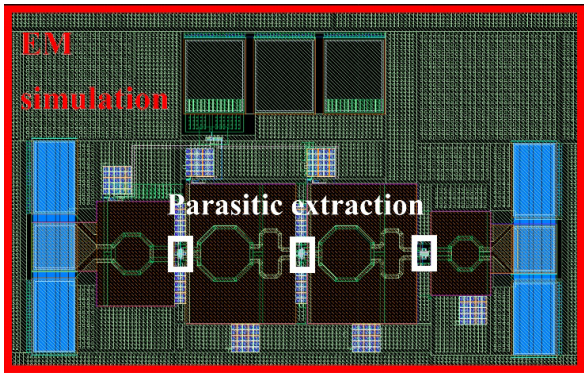


Fig. 3.Mm-wave PA layout

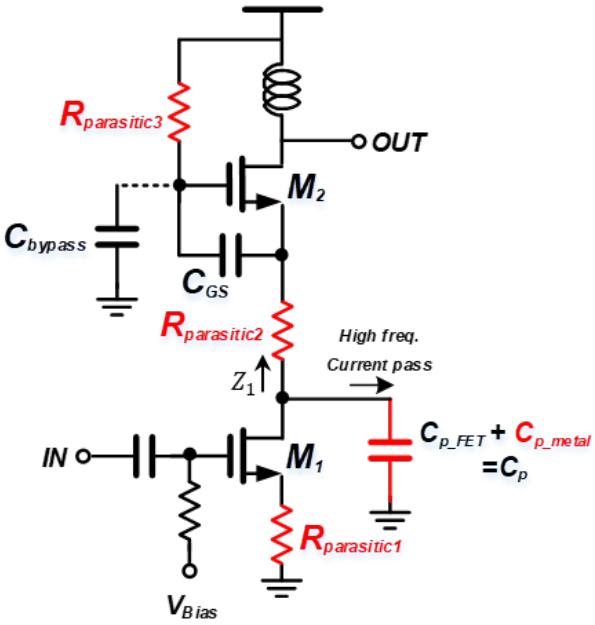


Fig. 4. Cascode parasitic elements

C. Cascode parasitic elements

Fig. 4 shows the resistance and capacitance among the most dominant parasitic elements in the cascode structure. Rparasitic1 reduces the gain by $1+g_{M1}R_{parasitic1}$ due to the source degeneration. Therefore, the source parasitic resistance is an important issue in design because it affects the gain in low and high frequency. Cp and Rparasitic3 are

important parasitic components in circuit analysis in the high frequency because they show an effect as the frequency increases. In low frequency, since the impedance of the current pass that falls into Cp is still large as shown in equation (1), the effect on the leakage current is not large, and the decrease in gain is not large. However, at high frequencies, the current pass to the ground is caused by Cp between M1 and M2, which affects the reduction of the circuit gain. The impedance for the ground path between the M1 and M2 nodes is Equation (3). As the frequency increases, $R_{parasitic3} \cdot sC_{GS}$ increases, and $1/sC_P$ decreases. As a result, current leakage through the Cp results in a decrease in gain. If the parasitic resistances 2, 3 and capacitor increase due to the wrong layout, this gain reduction becomes more serious. The influence of the cascode gate on the parasitic resistance may be removed through the bypass capacitor. In conclusion, it should be analyzed through parasitic extraction because the influence on parasitic elements from metal components adjacent to the PDK transistor model, which is difficult to analyze with EM simulation, affects the gain of the circuit.

$$\frac{1}{g_{M2}} + R_{parasitics2} \tag{1}$$

$$\frac{1}{g_{M2}} + R_{parasitics2} + \frac{R_{parasitic3}}{\beta_{CMOS}} \tag{2}$$

$$\left(\beta_{CMOS} = g_{M2} \cdot \frac{1}{sC_{GS}}\right)$$

$$Z_1 = \left(\frac{1}{g_{M2}} + R_{parasitics2} + \frac{R_{parasitic3} \cdot sC_{GS}}{g_{M2}}\right) // \frac{1}{sC_p} \tag{3}$$

D. mm-wave PA drive stage pre-&post simulation

Fig. 5 shows the differential cascode structure applied to the drive stage of the mm-wave PA in Fig. 2. Similarly, dominant parasitic components generated through the layout of the cascode structure of Fig. 6 (a) were expressed. Fig. (b) shows the layout structure of the cascode gate and the parasitic resistance $R_{p5,6,7}$. R_{p7} is not significantly affected by the virtual ground of the cascode gate, but $R_{p5,6}$ remains influenced by the parasitic resistance of the cascode gate, as shown in the previous analysis of Fig. 4. To analyze the effects of cascode gate parasitic components (R_{p5} and R_{p6}), parasitic components are identified using parasitic extraction through Fig. 7 (a), (b). In Fig. 7 (a), metal is used as a single layer and thin layout is performed to generate a large parasitic resistance. R_{p5} and R_{p6} each have a parasitic resistance of 11.5 ohm. In Fig. 7 (b), four layers are stacked to reduce parasitic resistance components. Metal is thickened to reduce the resistance component to 0.8 ohm. The Fig. 8 is a gain graph obtained by extracting the parasitic resistance value of the cascode gate metal and comparing it according to the stack and thickness change. Post simulation1 is a metal layout with a thin width of 1 stack, showing a 11.5ohm parasitic resistance and causing a gain reduction of 1 dB or more. Therefore, the metal was increased in width and applied in 4 stacks to minimize the decrease in gain by lowering the resistance. Fig. 9 confirms the parasitic resistance through the layout of the drain to source of M1, 2 and M3, 4 of cascode. Fig. 10 is the result of comparison according to parasitic resistance of metal. As shown in the previous equation (2), (3) as the parasitic resistances R_{p3} and R_{p4} between the drain and the source increase, the gain decreases. The decrease in gain is greater than the cascode gate parasitic resistance. Since it overlaps with the cascode gate, it is difficult to stack in many layers, so there is a limit to lowering parasitic resistance, and the overlapping area grows C_{p_metal}, so the layout should be

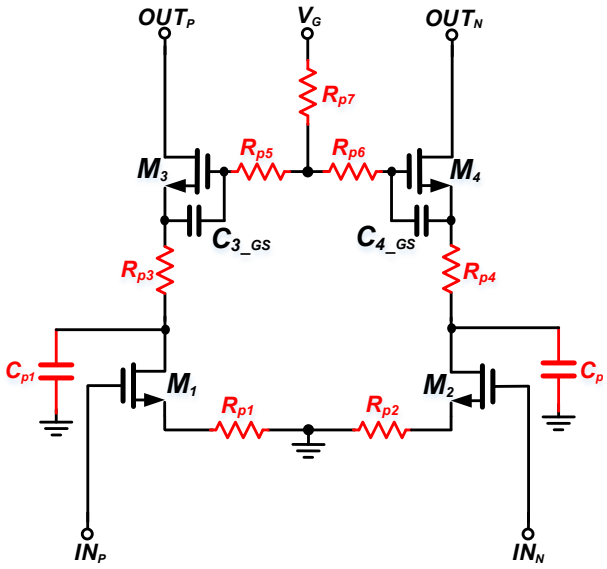
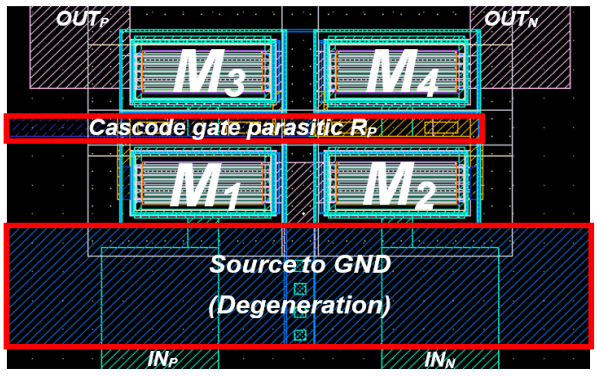
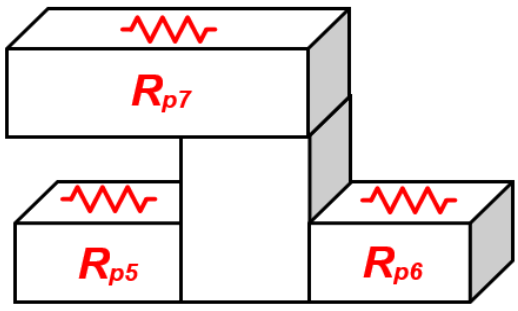


Fig. 5. Parasitic elements in drive stage of PA



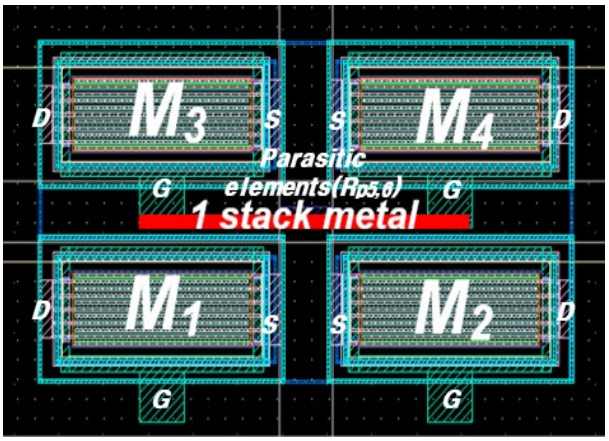
(a)



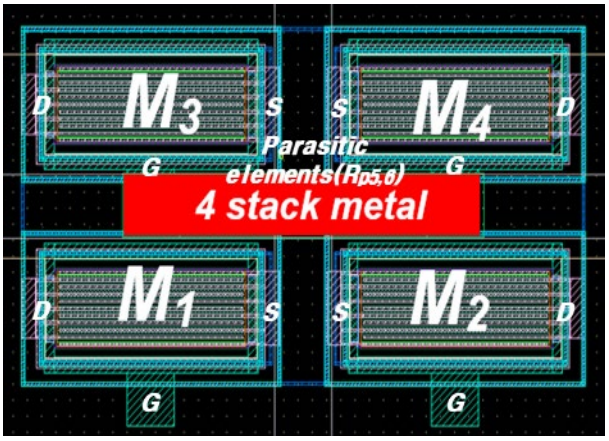
(b)

Fig. 6. Drive stage (a) layout, (b) cascode gate layout structure

designed appropriately. Fig. 11 is designed to reduce the influence of source degenerate parasitic resistance as much as possible by stacking metal in several layers and designing it thickly. As a result, the Fig. 6 (a) layout was designed by analyzing the previous post simulation and reducing the parasitic. When all parasitic are reflected, the result is shown in Fig. 12, which reduces the gain to about 1 dB or less and can be designed to be 16.8 dB.



(a)



(b)

Fig. 7. Cascode gate layout (a) 1 stack(11.5 ohm) (b) 4 stack(0.8 ohm)

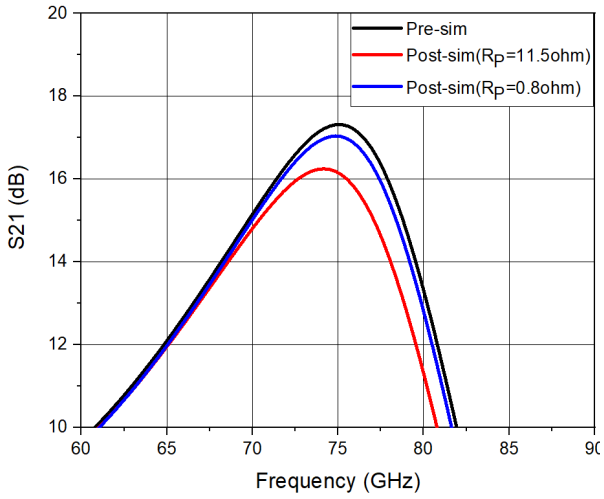


Fig. 8. Cascode gate parasitic resistance pre&post simulation

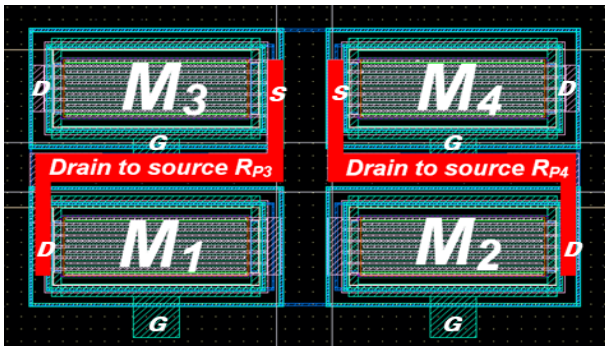


Fig. 9. Drain to source layout

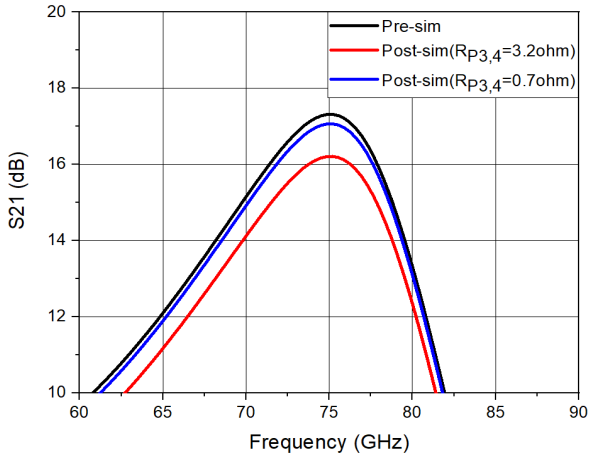


Fig. 10. Drain to source parasitic resistance pre&post simulation

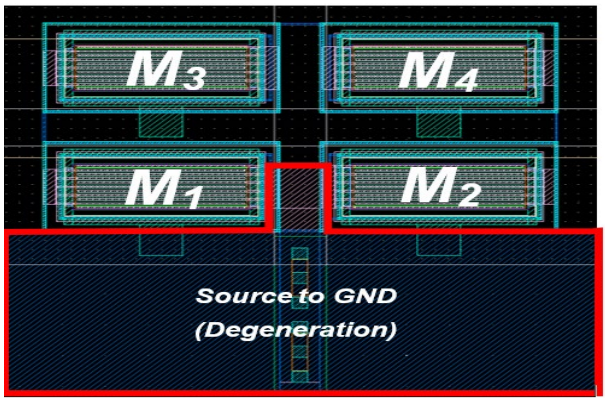


Fig. 11. Source to ground layout

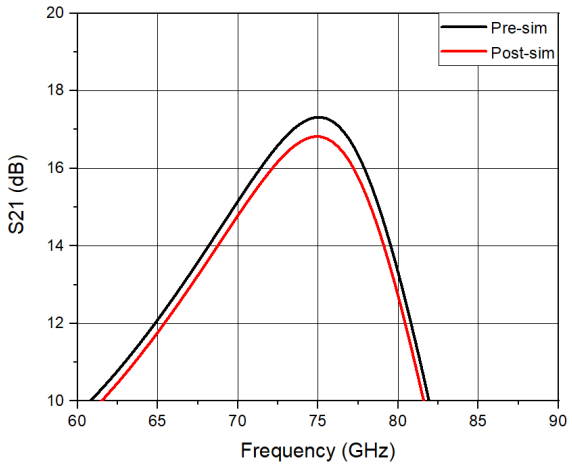


Fig. 12. Mm-wave PA pre&post simulation

TABLE I. Performance comparison with other millimeter-wave power amplifiers

Reference	Technology	Freq. (GHz)	VDD (V)	Max. S21 (dB)	P_{Sat} (dBm)	Max. PAE (%)	P_{DC} (mW)	Architecture
This work*	28nm CMOS	73-78	1	16.8	7	6.5	62	3-stage Cascode & CS Diff. w/ baluns
[5]	65nm CMOS	77	2	14.3	12.83	8.06	236	2-stage Cascode Diff. w/ baluns
[6]	65nm CMOS	58-65	1	16	11.5	15.2	50	3-stage CS Diff. w/ baluns
[7]	65nm CMOS	45-56	1.2	12.6	13	11.7	-	3-stage CS Diff. w/ baluns
[8]	90nm CMOS	77	1.2	9.9	13.2	10.4	140.4	3-stage pseudo-differential CS
[9]	90nm CMOS	77	1.2	8.5	6.3	-	142.2	

*Simulation results

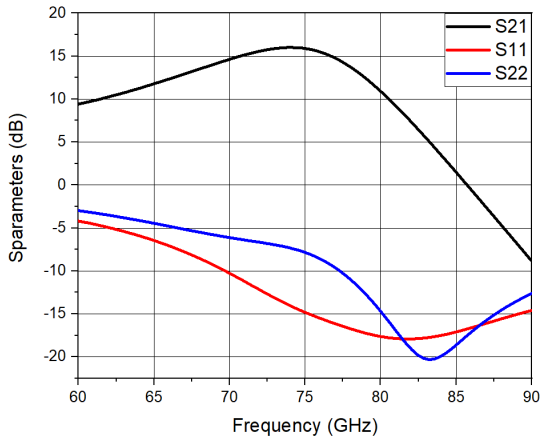


Fig. 13. S-parameters

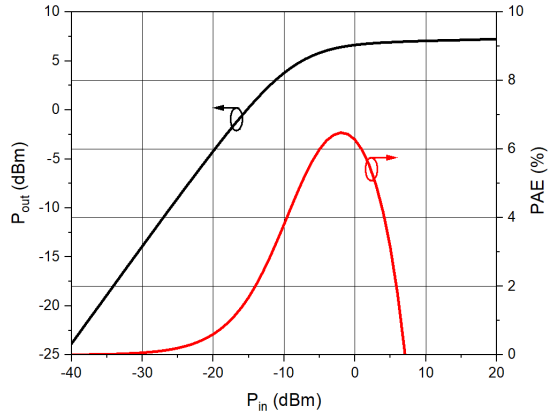


Fig. 14. Output power & PAE

III. SIMULATION RESULTS

The chip layout of the PA designed using the 28nm CMOS process is shown in Fig. 3. The chip area is 907 µm x 572 µm, including PAD. PA consumes 62 mW DC power from 1 V supply. Fig. 13 shows the simulated S-parameters result of PA. Through the simulation results, it was confirmed that the peak small signal gain of 16.8 dB was obtained. Fig. 14 confirms the output power and PAE compared to the input power at 77 GHz by simulation. The maximum output power is 7 dBm and the PAE is 6.5%.

IV. CONCLUSION

For optimal gain, the mm wave power amplifier designed by analyzing the effect of parasitic components in the cascode structure was designed using the 28nm CMOS process. We present insights into circuit design by analyzing the gain effects of parasitic extraction from gate and drain nodes of cascode. As a result of the simulation, the saturation output power was 7 dBm and the PAE was 6.5%. Using 1 V supply voltage, S21 of 16.8 dB is obtained and DC power of 62 mW is consumed. In Table 1, the simulation results of this paper are smaller in power and efficiency than other results. This is because trade-off is performed where the gain is higher than power matching at the output terminal.

ACKNOWLEDGMENT

This work was supported by Samsung Electronics Co. Ltd. and IDEC.

REFERENCES

[1] S. Lawton, C. Andrews, and D. Topham, "Test Implications for Approval of 76–77 GHz Radar Systems in Vehicles," *The Journal of Navigation,* vol. 53, no.1, pp. 48-53, Jan. 2000

[2] J. Lee, Y. -A. Li, M. -H. Hung, and S. -J. Huang, "A Fully-Integrated 77-GHz FMCW Radar Transceiver in 65-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2746-2756, Dec. 2010

[3] Ken B. Cooper et al., "Using FMCW Doppler Radar to Detect Targets up to the Maximum Unambiguous Range," *IEEE Geoscience and Remote Sensing Letters,* vol. 14 no.3, pp. 339-343, Mar. 2017.

[4] J. Wenger, "Automotive radar - status and perspectives," *IEEE Compound Semiconductor Integrated Circuit Symposium (CSIC)*, Palm Springs, CA, USA, 2005, pp. 21-24.

[5] J. Oh, B. Ku, and S. Hong, "A 77GHz CMOS medium power amplifier with transmission line transformers for multi-mode automotive radar system," *IEEE Asia-Pacific Microwave Conference Proceedings (APMC)*, Seoul, South Korea, 2013, pp. 769-771

[6] Wei L. Chan, and John R. Long, "A 58–65 GHz

Neutralized CMOS Power Amplifier with PAE above 10% at 1-V Supply," *IEEE Journal of Solid-State Circuits*, vol. 45 no. 3 pp. 554-564, Mar. 2010

[7] S. Park, and S. Jeon, "A Transformer-Matched Millimeter-Wave CMOS Power Amplifier," *Journal of Semiconductor Technology and Science*, vol. 16 no. 5 pp. 687-694, Oct. 2016

[8] Tao-Yao Chang, Chao-Shiun Wang, and Chorng-Kuang Wang, "A 77 GHz Power Amplifier Using Transformer Based Power Combiner in 90 nm CMOS," *IEEE Custom Integrated Circuits Conference 2010,* San Jose, CA, USA, 2010, pp. 1-4

[9] T. Suzuki et al., "60 and 77GHz Power Amplifiers in Standard 90nm CMOS," *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2008, pp. 562-636, doi: 10.1109/ISSCC.2008.4523307.

Deok Young Kim received the B.S. degrees in electrical and electronics engineering from Kangwon National University, Chuncheon, Korea, in 2019, where he is currently working toward the M.S. degree in electrical and electronics engineering from Yonsei University, Seoul, Korea. His research interest includes mm-wave PA and GaN amplifier.