A 101.6-dB-SNDR Fully Dynamic Zoom ADC using a Closed-Loop Miller Compensated Floating Inverter Amplifier

Yohan Choi[1] and Chul Woo Kim[a]
Department of Semiconductor engineering, Department of Electrical Engineering, Korea University
E-mail : [1]cyh@kilby.korea.ac.kr

***Abstract* - A floating inverter amplifier (FIA) is an alternative amplifier for switched-capacitor circuits. FIA-based switched-capacitor circuits have both negative feedback and dynamic operation advantages. However, the self-cutoff operation creates time-varying operating points while acting as an amplifier. Therefore, a small-signal analysis cannot anticipate the system's response. This paper presents a circuit-design-oriented intuition to tame the step response of such circuits. Also, the simulation method using RF simulators is explained to verify the gain and noise performance. Finally, a Miller-compensated 2-stage FIA is designed based on described design procedure, then applied to a fully dynamic zoom ADC design. The prototype ADC achieves 101.6 dB signal-to-noise and distortion ratio (SNDR) with an SNDR-based Schreier figure of merit (FoM) of 174.2 dB at 2.56-MHz fs having linearly scalable bandwidth and power consumption as fs varies, as well as easy power duty-cycling.**

***Keywords*—Delta-sigma modulator, Dynamic amplifier, Floating inverter amplifier, Frequency compensation, Zoom ADC**

I. INTRODUCTION

The operational transconductance amplifier (OTA) is essential for designing delta-sigma ADCs because integrators and residue amplifiers are OTA-based building blocks, offset with low noise in sub kHz bandwidth. However, such analog circuits get penalties for scaling the CMOS process because of shrunk voltage headroom and low intrinsic gain. Moreover, bandwidth control of an OTA is not straightforward because extra circuits and dedicating logic are needed.

Recently, an FIA were introduced as an alternate circuit for the OTA in a switched-capacitor circuit. [1]-[3]. Two characteristics are important factors for above. First, an FIA's self-quenching behavior makes system operate dynamically. Therefore, controlling sampling speed and on-demand operation are available easily. Second, it is simple to embed the FIA to closed-loop system because of inherent common-mode feedback (CMFB), which is a tricky issue in dynamic amplifier or ring amplifier.

Fig. 1 shows a schematic of the FIA and its operation. As shown in Fig. 1(b), a varying common-source voltage of NMOS and PMOS over time results in time-varying operating points. This time variance makes it impossible that analyze the small-signal model in the frequency or Laplace domain. A basic linear system theory is brought to help better understand. General input/output description of the initially relaxed linear system is expressed as

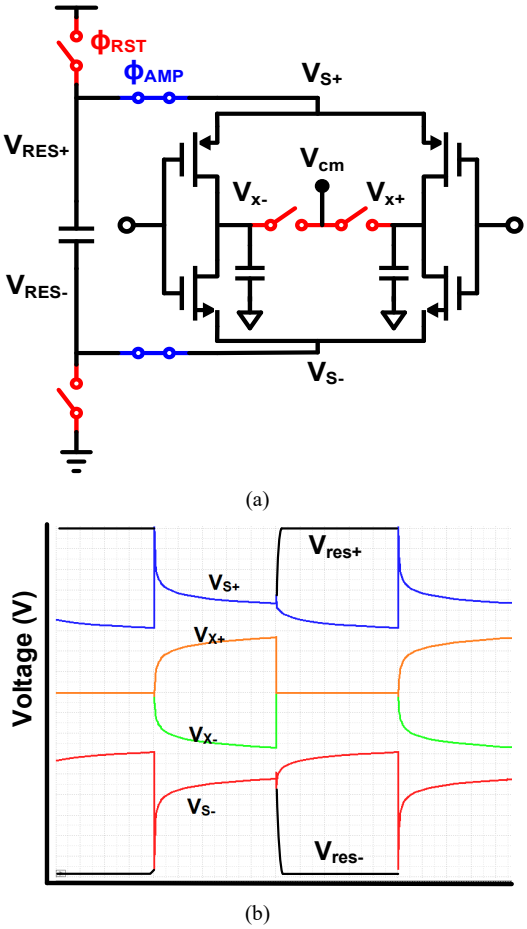


Fig. 1 (a) schematic and (b) operation across the time

$$y(t) = \int_0^{\infty} h(t,\tau) \cdot x(\tau) d\tau. \quad (1)$$

h(t, τ) represents the impulse response observed at time t to the applied impulse before *τ* time. With the time-invariance, *h(t, τ)* reduces to *h(t - τ)* thus Fourier transform of (1) becomes

a. Corresponding author; ckim@korea.ac.kr

Manuscript Received Apr. 12, 2022, Revised Dec. 17, 2022, Accepted Dec. 20, 2022

$$Y(j\omega) = \int_0^\infty \left[\int_0^\infty x(\tau)\cdot h(t-\tau)d\tau\right]e^{-j\omega t}dt$$
$$= \int_0^\infty x(\tau)e^{-j\omega t}\left[\int_0^\infty h(t-\tau)e^{-j\omega(t-\tau)}dt\right]d\tau$$
$$= H(j\omega)\cdot X(j\omega). \quad (2)$$

However, this is not valid in the time-variant system because an impulse response is time-dependent and therefore is no longer a time-shifted version of the original one, as expressed below

$$x(t) \rightarrow h(t)\cdot x(t). \quad (3)$$

$$x(t-t_d) \rightarrow h(t)\cdot x(t-t_d) \neq h(t-t_d)\cdot x(t-t_d). \quad (4)$$

An FIA's open-loop gain is already discussed by time-domain analysis in [4]. However, using those to different topologies is debatable since both instant input and the response of the corresponding system differ from the open-loop case (e.g., multi-stage cascading or embedding in a feedback system).

Also, quantitative analysis of the LTV system is much more intricate than the LTI system. As shown in Fig.2, the amplification phase of the SC-integrator is configured as a capacitive feedback amplifier, but deriving the transfer function is difficult because the linear time-variant state equation should be solved. Therefore, circuit designers count more on intuition than analysis to interpret the circuit's response.

This paper is organized as follows. Verification method of a proposed FIA in the SC-circuit is discussed in terms of gain, noise and stabilization in Section II. In Section III, a designed fully dynamic zoom ADC is briefly described. Section IV presents measurement results, then conclude this article.

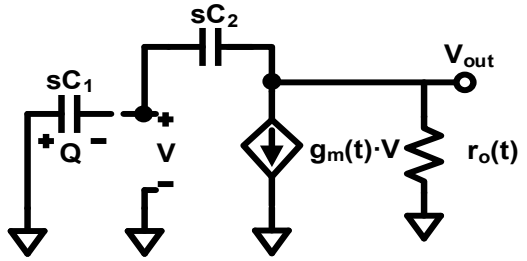


Fig. 2. Small-signal model of FIA based SC-circuit at amplification phase.

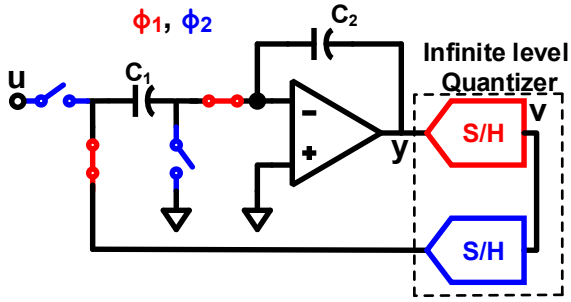
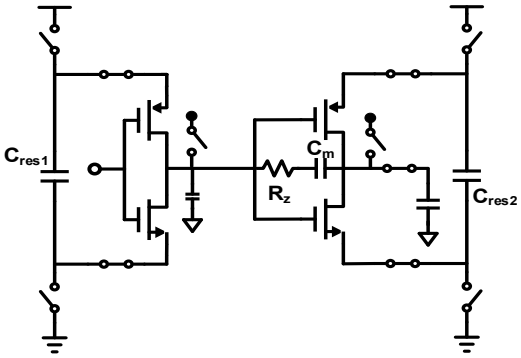
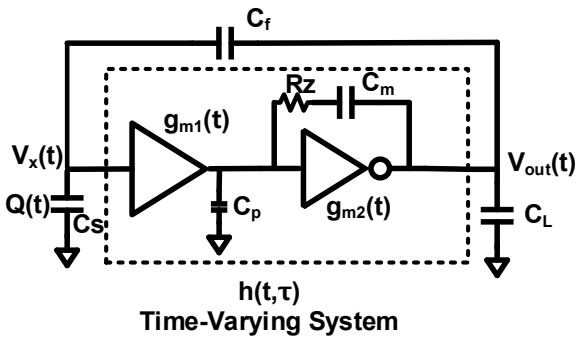


Fig. 3. Block diagram of simulation testbench.



(a)



(b)

Fig. 4. (a) Proposed FIA (single-ended equivalent) and (b) SC circuit configuration.

II. DESIGN VERIFICATION OF THE FIA IN SC-CIRCUITS

A. Gain

A simulation test-bench is shown in Fig. 3. Input, output, and the corresponding response of FIA are precisely those of the FIA inside the SC-integrator under this configuration. An ideal S/H plays the role of ADC and DAC with an infinite resolution. Therefore, a MOD1 without quantization error operates periodically rather than chaotic, so running PSS analysis is available. A transfer function of an SC-integrator is

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2}\cdot\frac{pz^{-1}}{1-pz^{-1}} \quad (5)$$

where p ≈ A/1+A.

An NTF of the first order delta-sigma modulator is $1\text{-}pz^{-1}$. A gain of an FIA within the SC-integrator can be extracted from the magnitude of the NTF at DC. Using this method, the gain of an FIA in the first integrator is about 60 dB.

B. Noise

Assuming the amplifier is a static OTA, the total noise power on C_1 of the SC-integrator in Fig. 3 is

$$\overline{v_{n,C_1}}^2 = \frac{kT}{C_1}\cdot\left(\frac{7/3+2x}{1+x}\right) \quad (6)$$

where $x = 2g_m r_{on}$ [5].

A formula can be changed according to the OTA's topology, but it is apparent that the sampling capacitor, g_m, and switches' R_{on} affect noise power. However, with an FIA rather than the OTA, parameters are highly coupled through feedback, and varies along with time. Consequently, acquiring an equation such as (6) demands a lot of mathematical efforts.

Fortunately, CAD tools those are widely used for circuit design can compute noise power of the time-variant system. A simulation testbench is same to that of in fig. 3. In terms of noise simulation, this is a traditional method to calculate device noise of delta-sigma modulator [6]. Fig. 5 shows that pnoise and transient-noise simulation are well matched.

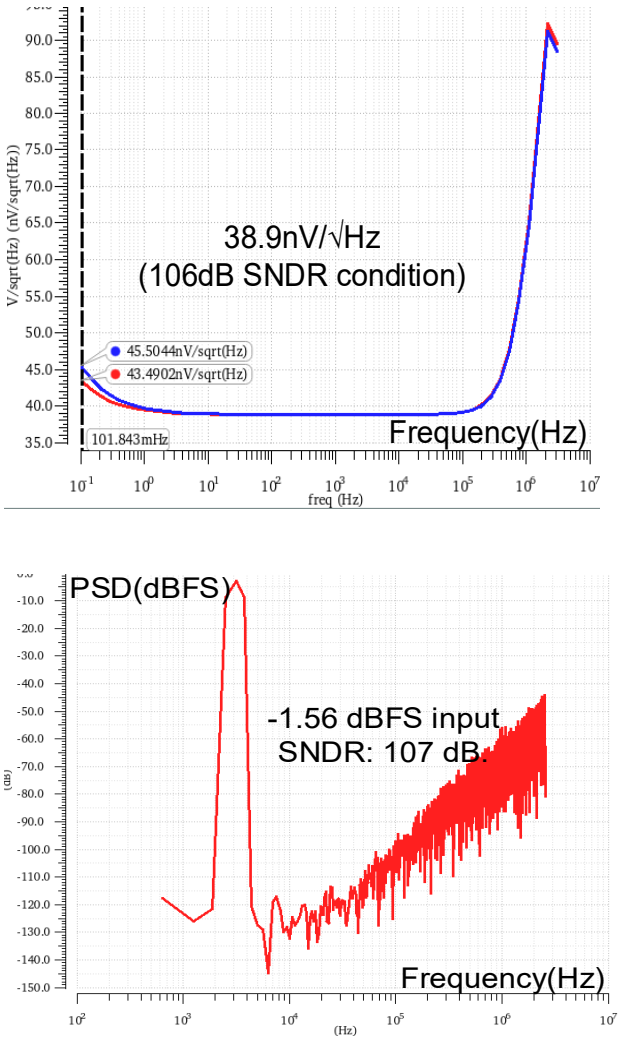


Fig. 5. PNOISE result of the first integrator and SNDR of the designed ADC which only loop-filter's noise is activated.

C. Stabilization

In case of the nominal 2-stage amplifier using a Miller-compensation with zero-nulling resistor, key parameters for stabilization is below

$$\omega_{ug} = g_{m1}/C_m. \tag{7}$$

$$|z| \approx \frac{\left|R_z - \frac{1}{g_{m2}}\right|}{C_m}. \tag{8}$$

$$|p_2| \approx \frac{|g_{m2}|}{C_m}. \tag{9}$$

A difference from the conventional case is that g_m changes over time in case of the FIA based SC-circuit. The necessary condition of the stable condition is $\|\omega_{ug}\|<\|p_2\|$. Since C_{res} affects FIA's gm more than transistor's size, the stable condition implies $C_{res1}<C_{res2}$. R_z acts on a damping of the step response. This means that R_z contributes not only stability but also settling accuracy.

For initial design procedure, designers should first tame a step response by manipulating C_{res1}, C_{res2}, C_m, and R_z including transistor sizing, and then check the gain, noise by performing simulations as described in Section II A and B.

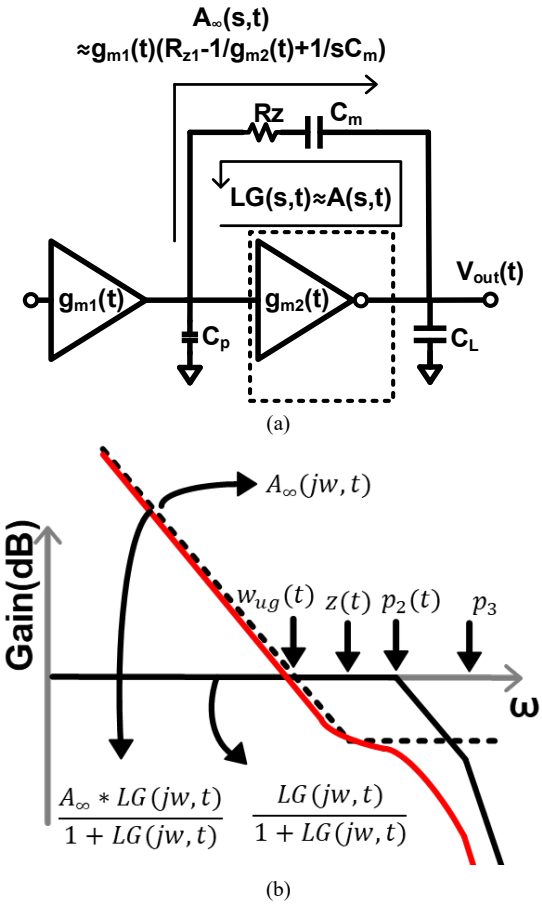


Fig. 6. (a) Design-oriented analysis and (b) Bode plot

III. CIRCUIT DESCRIPTION

Fig. 7 shows a top block diagram of the proposed ADC. A zoom ADC topology is selected to overcome limited swing range of FIAs. 5-level flash ADC and 5-bit asynchronous SAR ADC are used as a multi-bit quantizer. Data-weighted averaging method is used for dynamic element matching to cope with linearity issue of the main feedback DAC. A loop filter is designed to 2nd order CIFF topology. The first

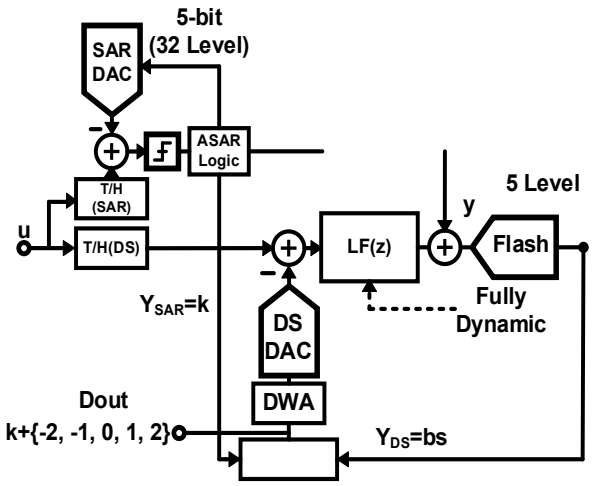


Fig. 7. Top block diagram

integrator employs chopping to mitigate 1/f noise. There are no static circuits such as OTAs and current sources. Hence, a designed ADC operates fully dynamically. The residue quantization error is canceled through feed-forward path [7]. Over-ranging is four to cover up the error of coarse SAR ADC. This implies that the coarse ADC has a ±1.5 LSB redundancy.

IV. MEASUREMENT

An audio analyzer, APx555 is used as a signal source. It has 120 dB SNDR resolution within signal bandwidth, but the output of the APx555 has a zero common-mode voltage. Therefore, signal conditioning is needed to filter out-of-band noise and makes a proper common-mode level. Fig.9 shows simplified block diagram. Analog front-end composed of anti-aliasing filter (AAF) and charge-bucket (CB) filter. The second-order multiple feedback topology is designed as an AAF. It attenuates the first aliasing band signal by -60 dB. Besides, the AAF converts zero common-mode level to the appropriate common-mode level of subsequent ADC. A CB filter is placed to assist the AAF in driving an ADC and preventing the signal contamination from kickback noise.

The prototype IC is implemented in a 0.18-μm CMOS process, and occupies 0.65 mm^2. Fig. 8 shows a chip-photograph. As shown in Fig.11., 101.6 dB SNDR is calculated from the FFT results when an ADC operates at 2.56 MHz of sampling frequency as shown in Fig. 10. 108 dBc of THD is measured, which means there is almost no room from noise margin. This is because coarse ADC's quantization error isn't fully canceled due to gain-error between flash and SAR ADC. The prototype ADC operates from 256 kHz to 3.75 MHz of sampling frequencies with SNDR > 100dB. SNDR decreases at very low frequency because input filter cannot prevent the noise aliasing of the signal source, and dynamic range is measured to 101 dB, as shown in Fig. 12. Dynamic range and SNDR have almost the same value. This is because small amplitude signal is buried by ground noise. We suspect the reason for that I/O driver's power isn't separated from digital power. Hence, when on-chip output buffer drives an external logic analyzer, digital circuits include timing logic of the loop filter is affected.

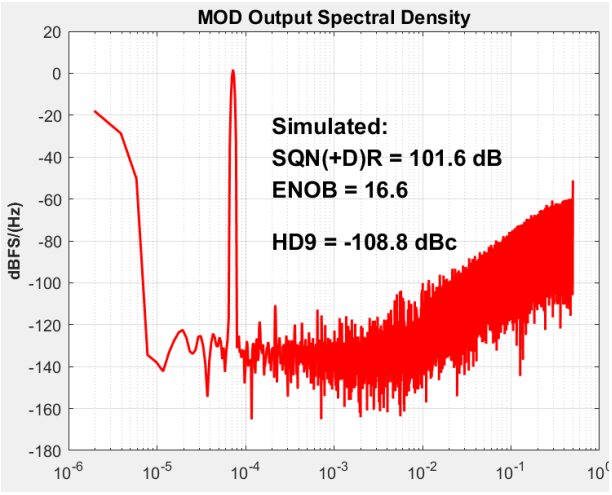


Fig.10. FFT result of prototype ADC at 2.56MHz f_s

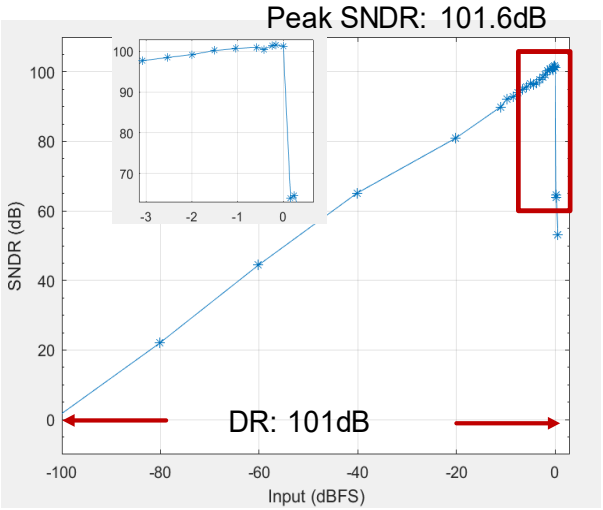


Fig.11. Measured SNDR, DR versus input amplitude

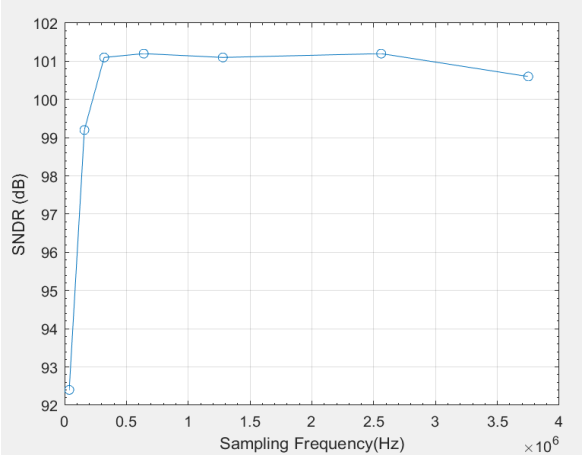


Fig.12. SNDR versus f_s from 37.5 kHz to 3.75 MHz.

V. CONCLUSION

A dynamic integrator using a 2-stage FIA is introduced to replace the conventional OTA based integrator. Simulation method to verify such time-variant system is briefly explained, and fully dynamic zoom ADC is implemented using the proposed integrator. The proto-type IC achieved 101.6 dB SNDR. Besides, SNDR > 100dB is accomplished within 256 kHz to 3.75 MHz fs. This research contributes to validity of multi-stage frequency compensated FIA design and its verification.

REFERENCES

[1] M. Zhao, Y. Zhao, H. Zhang, Y. Hu, Y. Bao, L. Ye, W, Qu, and Z. Tan, "A 4-μW bandwidth/power scalable delta-sigma modulator based on swing-enhanced floating inverter amplifiers," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 709–718, Nov. 2021.

[2] X. Tang, et al. "A 0.4-to-40MS/s 75.7dB-SNDR Fully Dynamic Event-Driven Pipelined ADC with 3-Stage Cascoded Floating Inverter Amplifier", *IEEE International Solid- State Circuits Conference (ISSCC)*, pp. 376-377, Feb. 2021.

[3] X. Tang, X. Yhao, W. Zhao, C. Hsu, J. Liu, L. Shen, A, Mukherjee, W. Shi, S.-Li, D.Z. Pan and N. Sun, "A 13.5-ENOB, 107-μW noise-Shaping SAR ADC with PVT-robust closed-Loop dynamic amplifier," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3248–3259, Dec. 2020.

[4] X. Tang, L. Shen, B. Kasap, X. Yang, W. Shi, A. Mukherjee, D.Z. Pan and N. Sun, "An energy-efficient comparator with dynamic floating inverter amplifier," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1011–1022, Apr. 2020.

[5] M. Terrovitis and K. Kundert, "Device noise simulation of ΔΣmodulators," The Designer's Guide Community, Aug. 1999 [Online]. Available: https://designers-guide.org/analysis/delta-sigma.pdf

[6] R. Schreier, J. Silva, J. Steensgaard and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 11, pp. 2358–2368, Nov. 2005.

[7] E. Eland, S. Karmakar, B. Gonen, R. van Veldhoven, and K. A. A. Makinwa, "A 440-μW, 109.8-dB DR, 106.5-dB SNDR discrete-time zoom ADC with a 20-kHz BW," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1207–1215, Apr. 2021.

Yohan Choi (S'18) received a B.S degree in radiologic science from Korea University, Seoul, South Korea, in 2017, where he is currently pursuing an integrated M.S. and Ph.D. degree in the area of integrated circuits and systems. In 2017, he was selected as a scholarship student of the Korea Semiconductor Industry Association. His research interests include high-precision sensor interfaces and oversampling ADC designs.

Chul Woo Kim (S'98–M'02–SM'06) received the B.S. and M.S. degrees in electronics engineering from Korea University, Seoul, Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2001. He was an Intern with Design Technology, Intel Corporation, Santa Clara, CA, USA, in 1999. In 2001, he joined the IBM Microelectronics Division, Austin, TX, USA, where he was involved in cell processor design. He was a Visiting Professor with the University of California at Los Angeles, Los Angeles, CA, USA, in 2008, and the University of California at Santa Cruz, Santa Cruz, CA, USA, in 2012. Since 2002, he has been with the School of Electrical Engineering, Korea University, where he is currently a Professor. He has co-authored two books entitled CMOS Digital Integrated Circuits: Analysis and Design—4th Edition (McGraw Hill, 2014) and High-Bandwidth Memory Interface (Springer, 2013). His current research interests include wireline transceiver, memory, power management, and data converters. Dr. Kim was a recipient of the Samsung HumanTech Thesis Contest Bronze Award in 1996, the ISLPED Low-Power Design Contest Award in 2001 and 2014, the DAC Student Design Contest Award in 2002, the SRC Inventor Recognition Awards in 2002, the Young Scientist Award from the Ministry of Science and Technology of Korea in 2003, the Seoktop Award for excellence in teaching in 2006 and 2011, the ASP-DAC Best Design Award in 2008, the Special Feature Award in 2014, and the Korea Semiconductor Design Contest: Ministry of Trade, Industry and Energy Award in 2013. He served as a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, and was elected as a Distinguished Lecturer of the IEEE Solid State Circuits Society from 2015 to 2016. He is currently on the Editorial Board of the IEEE Transactions on Very Large-Scale Integration Systems and on the Technical Program Committee of the IEEE International Solid-State Circuits Conference.