

Design Methodology of Biopotential Amplifier with Adaptive CM Cancelling Technique

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Abstract – In this paper, the specifications of the previous biopotential amplifiers are reviewed in terms of maximizing the SNR. Based on the analysis, it is found out that the most important requirement for maximizing the SNR is the robustness to common-mode interference. In order to enhance both tolerance to CMI and T-CMRR simultaneously, a common-mode charge-pump (CMCP) and adaptive CMI cancelling loop are proposed in our previous work, where CMCP absorbs displacement current from the CMI source and adaptive CMI cancelling loop minimize the CMI shown at the amplifier output, respectively. Especially, the paper presents an analysis of the adaptive common-mode cancellation technique using an LMS algorithm that is dedicated for removing 50/60Hz noise during the biopotential recording.

Keywords—Analog Front-end, Biopotential Amplifier, Common-mode interference, Electrocardiogram (ECG), Wearable healthcare

I. INTRODUCTION

Long-term monitoring of electrocardiogram (ECG) is essential in diagnosing cardiovascular diseases such as paroxysmal atrial fibrillation, unstable or variant angina. However, acquiring the ECG signal under practical scenarios is not an easy task due to many disturbances from the recording environment. As depicted in Fig. 1(a), the biopotential is normally recorded via an impedance network which consists of contact impedance (Z_{EL}) and input impedance (Z_{IN}). Besides, the common-mode of the input varies due to the coupling from external power line (V_{CMI} and C_{CMI}), which is often referred as common-mode interference (CMI). With these environmental issues, the signal passes through an amplifier, which also adds intrinsic noise and nonlinear distortion and shown at the output. The effect of these non-idealities on SNR can be classified into attenuation, CM-DM conversion, non-linearity and intrinsic noise as shown in Fig. 1(b). The attenuation is due to voltage division itself from the impedance network at the input. The intrinsic noise (i.e. thermal and flicker noise) is generated from each circuit components and added to the signal while amplification. The non-linearity is also added due to a

disturbed biasing of the transistors by a large common-mode interference [1-2]. The CM-DM conversion is added to the signal due to intrinsic CMRR of the IA and imbalanced impedance network at the input (i.e. Z_{IN} and asymmetric Z_{EL} s) for each input nodes. The normalized amount of CM-DM conversion including these two effects are often described using the term total-CMRR (T-CMRR). The T-CMRR for a conventional IA shown in Fig. 1(a) can be represented as follows:

$$T - CMRR \approx \frac{\Delta Z_{EL}}{Z_{IN,CM}} + \frac{1}{CMRR_{IA}}$$

and it can be seen that T-CMRR can be enhanced when an IA that have both large CMRR ($CMRR_{IA}$) and high input impedance (Z_{IN}) are used. Note that the case when mismatch between the contact impedances (ΔZ_{EL}) are small is not considered since it is a variable that is set by the environment. In summary, the SNR of a biopotential amplifier can be represented by the following equation:

$$SNR = \frac{\alpha S}{N + C + D}$$

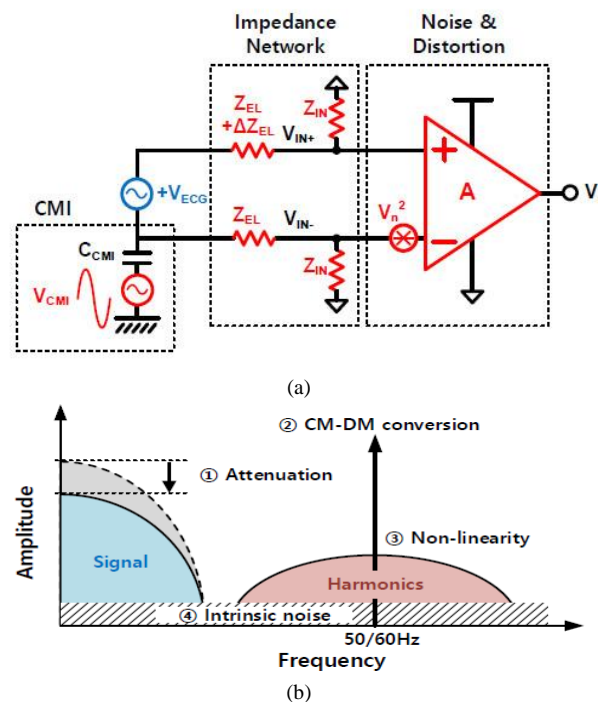


Fig. 1. (a) Sources of non-idealities that affects biopotential signal. (b) Effects of nonidealites on SNR.

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Manuscript Received Apr. 05, 2022, Accepted Aug. 09, 2022

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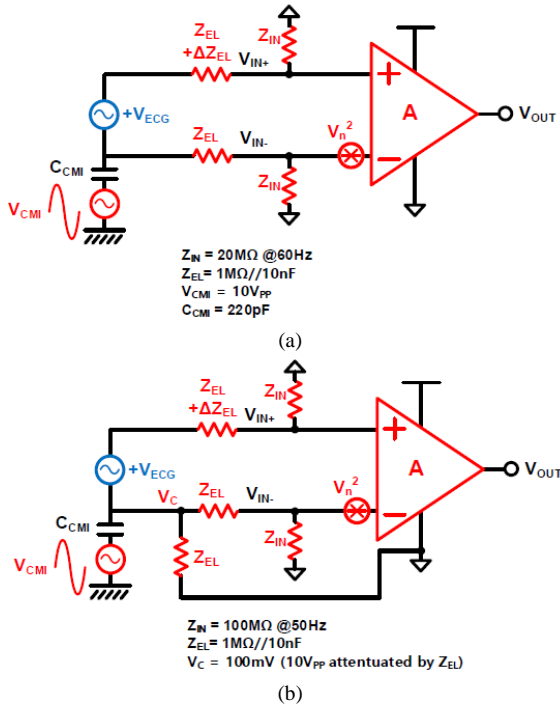


Fig. 2. Example scenarios for two-electrode ECG recording for calculation of SNR.

where α is the attenuation factor, S is the signal, N is the intrinsic noise, C is the CM-DM conversion and D is the nonlinear distortion. To remove each SNR-degrading factors in the above equation, it is well-known that the following specifications should be improved. First, the input impedance should be increased to prevent attenuation and CM-DM conversion. Second, T-CMRR should be improved by boosting both input impedance and CMRR of the IA itself. Third, the tolerance to CMI should be enhanced to withstand the nonlinear distortion due to CMI. Forth, the input-referred noise should be reduced. The primary among these requirements can be changed for each biopotential recording scenarios so that SNR is maximized. For example, we can consider a biopotential amplifier for two-electrode ECG recording using dry electrodes shown in Fig. 2(a) [2]. As can be seen in the figure, since the source impedance is 1M and input impedance is 20M at DC, is 0.95. Next, since the tolerance to CMI is 15V_{PP} and the CMI is 10V_{PP}, the nonlinear distortion due to CMI is negligible thanks to CM suppressing loop (i.e., $D = 0$). The intrinsic noise is $N = 1.64\mu\text{V}_{rms}$ when input referred. However, since the T-CMRR of the overall system is 66dB, CMRR of the overall system is 66dB, the CM-DM conversion is $C = 5\text{mV}$ when input-referred. From the above calculation, we can easily list the specification in order of importance: tolerance to CMI, T-CMRR, intrinsic noise and input impedance (in terms of attenuation). Another example that can be considered is an active electrode with conventional three-electrode configuration [3] as shown in Fig. 2(b). Assuming the same setting with the previous two-electrode case, the calculated factors are $\alpha=0.99$, $C = 1\text{mV}$, $N = 1.75\mu\text{V}_{rms}$ and $D = 0$.

Note that the T-CMRR varies from 42dB to 102dB due to contact impedance variation and distortion by CMI is negligible thanks to the biasing electrode. The priority of the specifications can be listed just like the previous example: T-CMRR, intrinsic noise, input impedance and tolerance to CMI. For both cases, it can be seen that the T-CMRR have first or second priority since it is typically much larger than the input-referred noise.

II. REVIEW OF PREVIOUS TECHNIQUES IN PERSPECTIVE OF SNR

For many years, various techniques are developed in order to remove the above nonidealities. The flicker noise is often removed by chopping. However, the input impedance is degraded, which result in T-CMRR degradation or signal attenuation. In order to enhance input impedance for these reasons, methods like active shielding, positive feedback or pre-charging are proposed. These techniques are valid in terms of preventing T-CMRR degradation [4], but not useful in terms of attenuation since the added circuit increases noise so that the SNR is maintained [5]. Note that T-CMRR is often limited by the impedance network nowadays, since an IA with CMRR larger than 100dB can easily be achieved using current-balanced IA or the averaging effect of the mismatch due to chopper [4]. To prevent the non-linearity by CMI (i.e. enhance the tolerance to CMI), current-absorbing circuit like common-mode charge pump (CMCP) or current sources are added at the input node [6]. However, these techniques degrade T-CMRR due to the mechanism shown in Fig. 3. Since the current-absorbing circuit generates common-mode current via each electrode impedances, the contact impedance mismatch (ΔZ_{EL}) results in an additional CM-DM conversion with an amount of $I_{CMI} \times \Delta Z_{EL}$, which is a critical source that degrades T-CMRR.

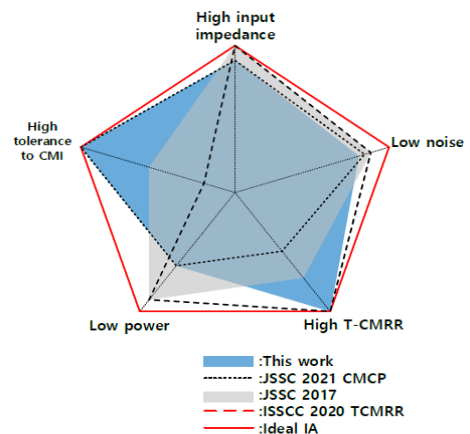


Fig. 3. Comparison of specifications for recent prior biopotential amplifiers.

In [6], the input impedance is boosted and tolerance to CMI is enhanced. However, the T-CMRR is not measured and moreover, the tolerance to CMI is still insufficient for cutting-edge applications like two-electrode ECG recording. In [4], the input impedance in common-mode is boosted and as a result, large TCMRR is achieved. However, since the chopping is not used, the noise is large at low frequency and tolerance to CMI is limited by the main operational transconductance amplifier (OTA), which makes the

amplifier not suitable for two-electrode ECGs. In [2], the tolerance to CMI is enhanced with acceptable power and noise performance. However, the T-CMRR is still low due to the degradation by the mechanism described above.

The basic mechanism of the design that addresses the above issue is already presented in [1]. In this paper, the detailed analysis on LMS algorithm and design consideration are provided.

III. DESIGN OF LMS ALGORITHM

A. Review of the previous work.

The schematic and timing diagram of the adaptive T-CMRR enhancing loop is shown in Fig. 4, where the current-absorbing circuit is implemented in the discrete-time domain using a common-mode charge pump (CMCP) [5]. The level shifts by Φ_{CMI} via capacitor C_{CF} is used for CMI reduction. The level shifts in DM (Φ_{AF} , Φ_{AFD} and their inverses) are generated by multiplying Φ_{CMI} , Φ_{CMLD} with its appropriate signs from LMS and CM-DM-conversion is cancelled by the level shifts in DM via capacitor arrays (C_{DF} and C_{DFD}). To realize the LMS algorithm for adaptive CMI cancellation, we must be able to monitor the CMI. The CMI is reconstructed from Φ_{CMI} , which contains the amount and direction of level shifts applied to CMI. In addition, both the gain and phase must be controlled in the cancellation loop, which is implemented using in- and quadrature-phase of the reconstructed CMI (i.e., V'_{CMI} and V'_{CMLD}). The reconstructed CMI and the output voltage are 1b quantized, multiplied, and accumulated for a sign-sign LMS algorithm that controls C_{DF} and C_{DFD} . Note that nonlinearity of C-DACs or mismatch between each C_F s have little effect on T-CMRR as these non-idealities are already included in LMS settling.

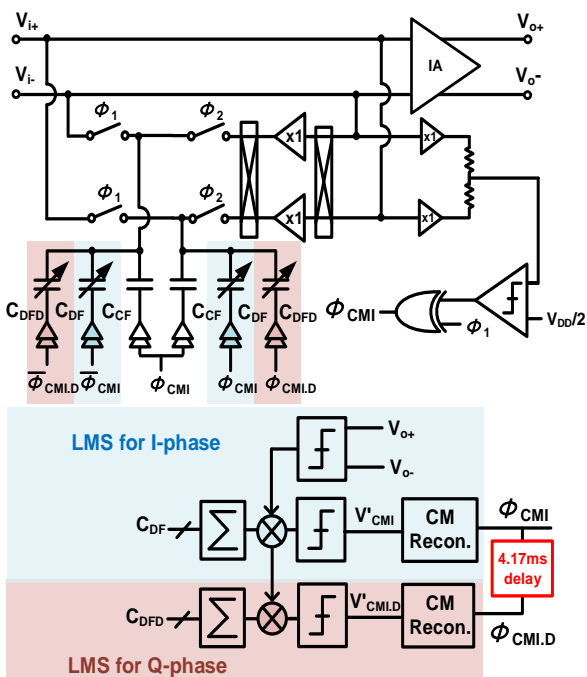


Fig. 4. IA with common-mode charge pump and adaptive CM cancellation.

B. Operation of quadrature LMS algorithm

Since both the gain and phase of the CMI at the output changes, it is obvious that both of them need to be tracked, which is done via quadrature-domain. As you asked, we simulated two scenarios: LMS with I phase-only and LMS with I-Q phase using MATLAB and the results are shown in the figures shown below. As shown in the first figure, the LMS is not effective for canceling out the Q-phase 60Hz noise when only I-phase LMS is enabled, but the LMS can remove all the noise when both I-phase and Q-phase are enabled.

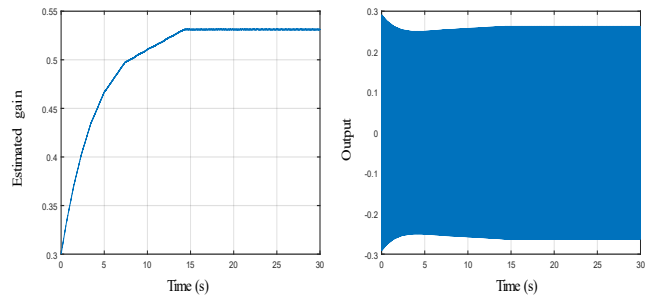


Fig. 5. MATLAB simulation result of I-phase-only LMS

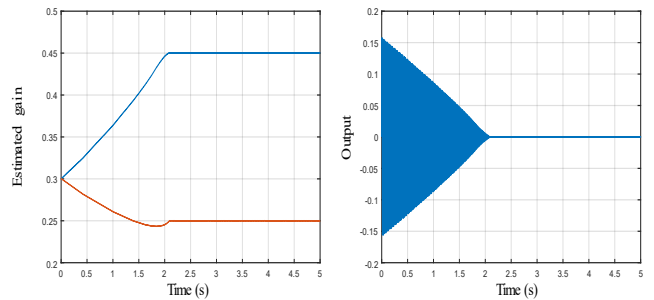


Fig. 6. MATLAB simulation result of I-Q phase LMS

C. Stability of the LMS loop

Regarding the stability of the LMS loop, the stability of a general LMS loop is determined by the inequality shown below.

$$0 < \mu < \frac{2}{\lambda_{max}}$$

where μ is the coefficient-updating step and λ_{max} is the greatest eigenvalue of the autocorrelation matrix of the noise. The meaning of the above equation is that μ should be smaller enough so that the sign which was negative at the n^{th} sample would not be the opposite direction at the $n+1^{th}$ sample without enough cancellation of the noise. In the proposed loop, the condition described above is well satisfied by keeping the resolution of the capacitor array to be small enough.

D. Linearity of the capacitor DAC

In order to maximize T-CMRR, the capacitor DAC that consists C_{DF} and C_{DFD} should have good resolution. The capacitor DAC consists of a thermometer-coded 9-bit

capacitor DAC with 500aF LSB. In this work, the linearity of the capacitor affects the operation if the input versus output is not monotonic, but has no effect if it is monotonic, even if it is nonlinear. The behavior can be explained by investigating the existence of local minimum, that the gradient descent converges into wrong solution. The amplitude of the output given by LMS can be described as follows:

$$|V_{OUT}| = -|(\delta_{F.real} - W_{1.CAP}) + j(\delta_{F.img} - W_{2.CAP})| \cdot |V_{CMI}|.$$

δ_F is the mismatch given by the circuit that has to be removed and $W_{1.CAP}$ and $W_{2.CAP}$ is the amplitude for subtraction defined by capacitor DAC, not the output code of the LMS algorithm itself. In the below simulation results (From Fig. 6 to Fig. 8.), distortion of V_{OUT} due to non-linearity is observed for three cases: without any non-linearity, non-linear but monotonic and non-linear an non-monotonic. From the figures, it can be seen that there are no local minimum for V_{OUT} when the DAC is monotonic (Fig. 6 and Fig. 7), but the local minimum are generated when the DAC is not monotonic as can be seen in Fig. 8 and it can also be seen that the convergence may be affected by the initial condition where the gradient descent begins. In the paper, the capacitor DAC may lose its monotonicity due to the process. However, above limitation is expected to be addressed by reducing LSB by using smaller process.

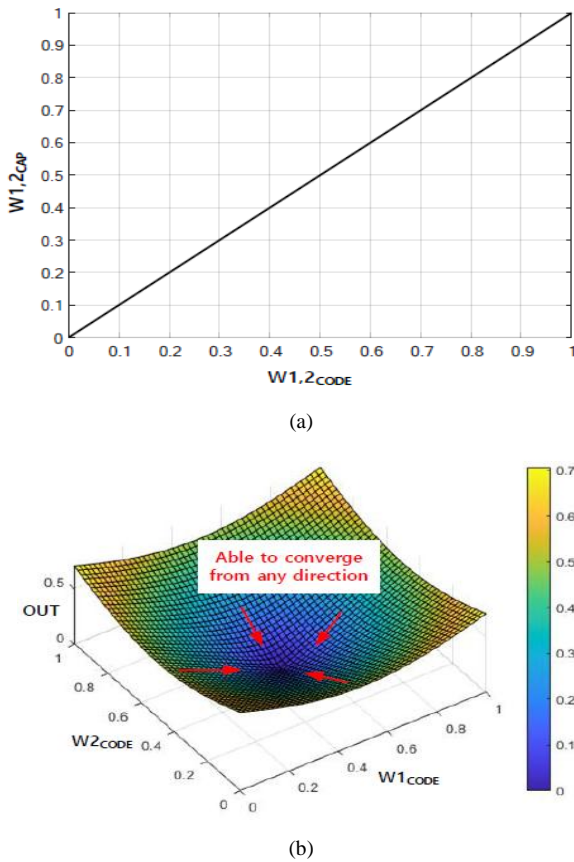


Fig. 6. Normalized output from quadrature LMS versus W1 and W2 for ideal capacitor DAC. (a) Input code versus output (b) 3-dimensional diagram for W1, W2 and resulted output.

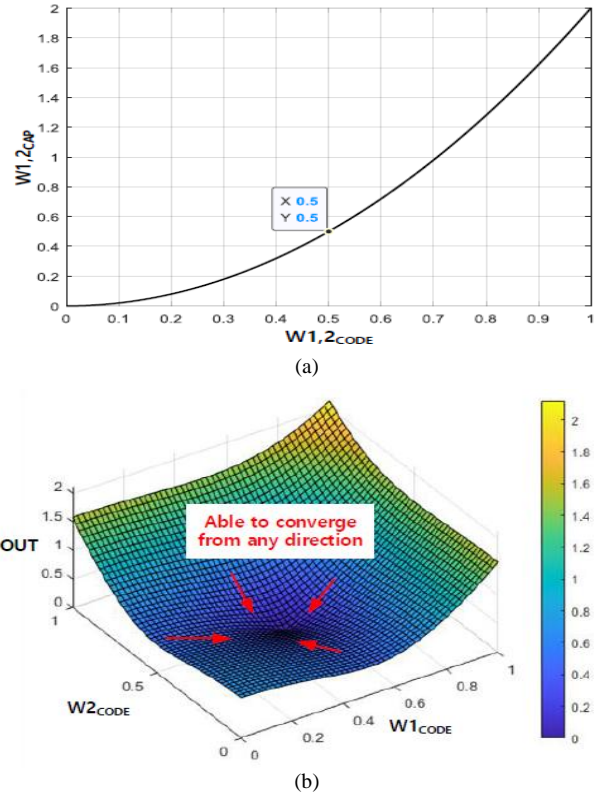


Fig. 7. Normalized output from quadrature LMS versus W1 and W2 for non-linear, monotonic capacitor DAC. (a) Input code versus output (b) 3-dimensional diagram for W1, W2 and resulted output.

IV. DESIGN CONSIDERATIONS OF IA WITH CMCP AND ADAPTIVE CM CANCELATION

A. Parasitic capacitance at the input node

The parasitic capacitance does not affect the performance of CMSL. Reflecting the parasitic capacitors, Fig. 2. in [2] can be changed as Fig. 8. In this scenario, the equation (2) and (3) in [2] is changed as follows.

$$V_{iCM}[n] = V_{iCM}[n-1] - r'V_{COMP}[n-1] + \frac{C_{CMI}}{C_{CMI} + C_{PAR}}(V_{CMI}[n] - V_{CMI}[n-1])$$

$$r' \approx \frac{2C_F}{C_{CMI} + C_{PAR} + 2C_F}$$

The above result means that there is an attenuation when V_{CMI} is delivered to V_{iCM} and when the level shift by CMSL is delivered to V_{iCM} . In order to see the effect of the above changes to the tolerance to CMI, the tolerance is calculated again with the same idea presented in [4].

$$f_{CMCP} \frac{2C_F}{C_{CMI} + C_{PAR} + 2C_F} V_{DD} > \max \left(\frac{C_{CMI}}{C_{CMI} + C_{PAR}} \frac{dV_{CMI}}{dt} \right)$$

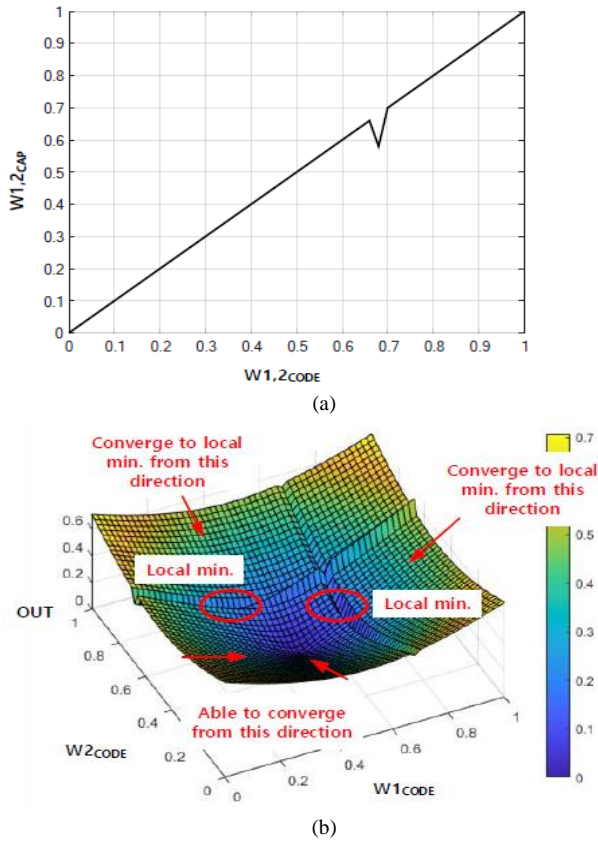


Fig. 8. Normalized output from quadrature LMS versus W1 and W2 for non-linear, nonmonotonic capacitor DAC. (a) Input code versus output (b) 3-dimensional diagram for W1, W2 and resulted output.

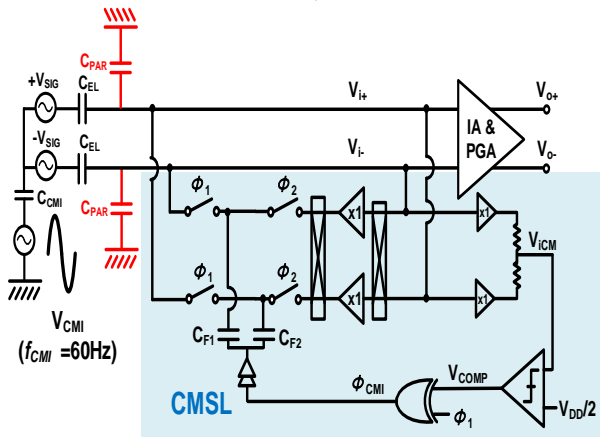


Fig. 9. Schematic of CMSL considering parasitic capacitances

$$\begin{aligned}
 Tol' &= \frac{f_{CMCP}}{\pi f_{CMI}} V_{DD} \cdot \frac{2C_F}{C_{CMI} + C_{PAR} + 2C_F} \cdot \frac{C_{CMI} + C_{PAR}}{C_{CMI}} \\
 &= Tol \cdot \frac{C_{CMI} + C_{PAR} + 2C_F}{C_{CMI} + C_{PAR}} \cdot \frac{C_{CMI} + C_{PAR}}{C_{CMI}}
 \end{aligned}$$

In the above equation, since C_{CMI} is typically larger than 200pF and C_F is 1.6pF, the C_F -related term in the above equation can be assumed to be very small. And if C_F -related term is removed, the tolerance remains the same regardless

of C_{PAR} . This means that the parasitic capacitance does not affect the performance of CMSL. The above result can be explained intuitively as follows: since the displacement current from the CMI source from the power line and the absorbing behavior of the current by CMSL is not changed due to C_{PAR} , there is no change in CM-suppressing operation and the tolerance remains the same.

B. Instrumentation amplifier

In this work, the capacitively-coupled IA with a chopper is adopted as a main amplifier. The reason why we have concluded using CCIA with chopper is that the CMRR of the IA can be improved by not only using CBIA, but also adopting chopper to CCIA and the CCIA with chopper does not require external capacitor for DC block, unlike CBIA. Improving the CMRR of the IA is too important in our work since there may exist an additional intrinsic tone in common-mode as described in [4].

C. Timing generation of CMCP

In Fig. 4, ϕ_1 is shorter than ϕ_2 (duty = 12.5%) since the operation during these two phases are completely different. In ϕ_2 , the buffer should charge C_F so that its top plate becomes the same as the input node and it requires enough settling time. Thus, we have scheduled a large portion of the time per a cycle to give enough settling time to the buffer. By contrast, in ϕ_1 , the level shift is induced to the input node by toggling the output of the logic gates, which does not require much time compared to the capacitor-charging operation in ϕ_2 . Thus, the time for ϕ_1 is set to be much less than ϕ_2 .

V. MEASUREMENT RESULTS

The proposed work is implemented using 180nm CMOS process. The cancellation of 60Hz noise is measured using the proposed chip and the result is shown in Fig. 11. It can be seen that the TCMRR is enhanced by the proposed work with the techniques described above. In order to quantitatively measure the enhanced TCMRR, the TCMRR is enhanced using the LMS with and without the proposed technique and the TCMRR enhancement of at least 50dB is measured.

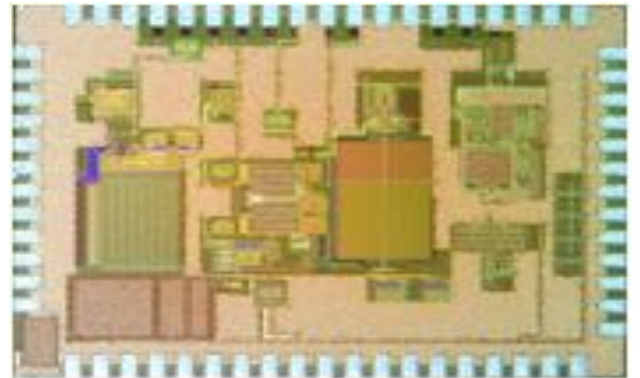


Fig. 10. Die photograph

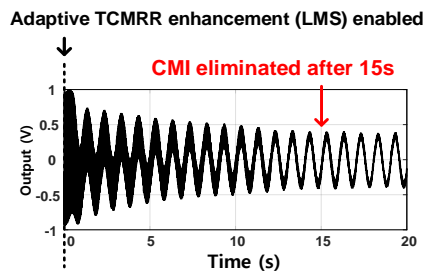


Fig. 11. Cancellation of 60Hz noise using the proposed work.

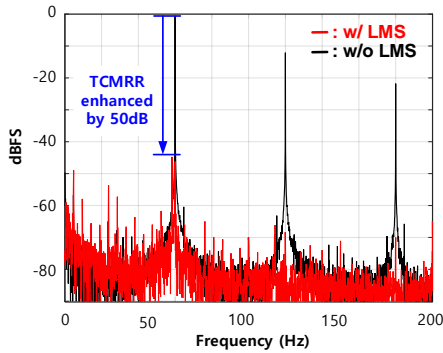


Fig. 12. Measured TCMRR enhancement using the proposed technique.

VI. CONCLUSION

In this work, the details and consideration for designing the common-mode charge pump with adaptive CM cancellation is provided. The above results shows that the stability of the LMS loop is basically not an issue and the linearity of the capacitor DAC should be designed to be monotonic at least. In addition, the tolerance to CMI including the parasitic capacitance, instrumentation amplifier and timing generation method is provided for the readers to adopt the adaptive CM cancelling technique for the future users of the technique. The measurement results support that the TCMRR enhancement can be achieved using the proposed work with the described details.

ACKNOWLEDGMENT

This work was supported by the Civil Military Technical Cooperation Program (No. 18-CM-SS-12) of Korea.

REFERENCES

[1] N. Koo, H. Kim and S. Cho, "A 22.6 μ W Biopotential Amplifier with Adaptive Common-Mode Interference Cancellation Achieving Total-CMRR of 104dB and CMI Tolerance of 15Vpp in 0.18 μ m CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2021, pp.396-398.

[2] N. Koo and S. Cho, "A 24.8-uW Biopotential Amplifier Tolerant to 15-VPP Common-Mode Interference for Two-Electrode ECG Recording in 180-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 2, pp. 591-600, Feb. 2021.

[3] J. Xu, et al, A 15-channel digital active electrode system for multi-parameter biopotential measurement," *IEEE*

Journal of Solid-State Circuits, vol. 50, no. 9, pp. 2090-2100, Sep. 2015.

[4] S. Zhang and Q. Li, "23.7 A 130dB CMRR Instrumentation Amplifier with Common-Mode Replication," in *2020 IEEE International Solid-State Circuits Conference (ISSCC)*, Jul. 2020, pp. 591-600.

[5] J. Lee, G. Lee, H. Kim, and S. Cho, "An Ultra-High Input Impedance Analog Front End Using Self-Calibrated Positive Feedback," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 8, pp. 2252-2262, Aug. 2018.

[6] H. Chandrakumar and D. Markovic, "An 80mVpp Linear-Input Range, 1.6G Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That Is Tolerant to 650-mVpp Common-Mode Interference," *IEEE Journal of Solid-State Circuits*, vol. 52 no. 11, pp.2811-2828, Nov. 2017.



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