A Voltage Mode PWM DC-DC Boost Converter with Adaptive Dead-time Generator for Solid-State Drives

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***Abstract* - This paper proposes a voltage mode PWM DC-DC boost converter for Solid-State Drive (SSD). SSD has recently been widely used to replace hard disk drives (HDD) in various systems. In order to drive SSD, a wide range of output voltages and high-efficiency voltage conversion are required. Therefore, the efficiency and stability of the boost converter are very important in each operating region. This paper presents a boost converter using type-3 compensator-based voltage mode control. It also proposed an adaptive dead-time generator to reduce efficiency reduction due to shoot-through current and diode conduction. The proposed converter is fabricated in TSMC 0.18um BCD process. In the simulation, a phase margin (PM) of 40 degrees or more was achieved in a wide output power voltage range of 5.5V-20V with a peak efficiency of 93.2%.**

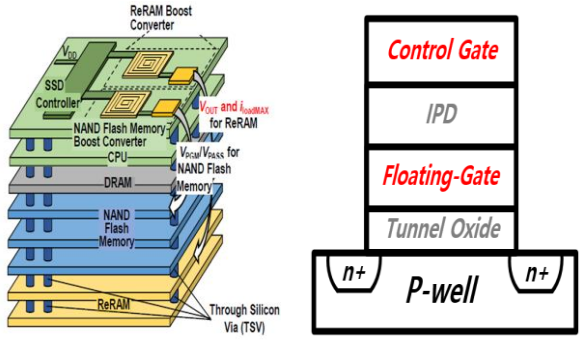
***Keywords*—Adaptive dead-time generator, Boost converter, Phase margin, Solid-state drives**

I. INTRODUCTION

Solid-state drive (SSD) is a method that stores data using semiconductors. It can solve the data processing speed limit of the existing Hard-disk drive (HDD) [1]. In particular, it has fast data read/write performance that can keep up with the speed of CPU and RAM, so overall PC performance can be improved. In addition, it has been used rapidly in recent years thanks to low operating noise, low power consumption, and good durability.

The internal structure of the SSD consists of a memory for storing data, a controller, and a buffer memory, as shown in Fig. 1(a) [2]. In general, a flash memory-based storage SSD requires a power management integrated circuit (PMIC) for using flash memory as well as power supply for various interfaces and controllers. Fig. 1(b) shows the structure of the NAND flash memory cell. The memory cell performs data write/erase operations through Fowler-Nordheim (F-N) tunneling [3]. Therefore, a high program voltage should be applied to the gate for data processing of the memory cell. In the read/write operation, the flash memory requires a very wide range of output voltages (10V-20V) which is higher than the input voltage (5V), as shown in Fig. 2. Recently, the application of SSD to portable computing devices such as laptops is expanding, and the input voltage is supplied by variable batteries. So, it is essential to design a DC-DC boost converter that operates stably in a wide output voltage range and has high efficiency to improve usage time.

In this work, a voltage-mode pulse width modulation (PWM) dc-dc boost converter is implemented. Section II describes the structure and details of the proposed boost converter control circuit. Section III shows the simulation results, and a conclusion is provided in Section IV.



(a) (b)

Fig. 1. Structure of (a) 3D-integrated solid-state drive and (b) NAND flash memory cell.

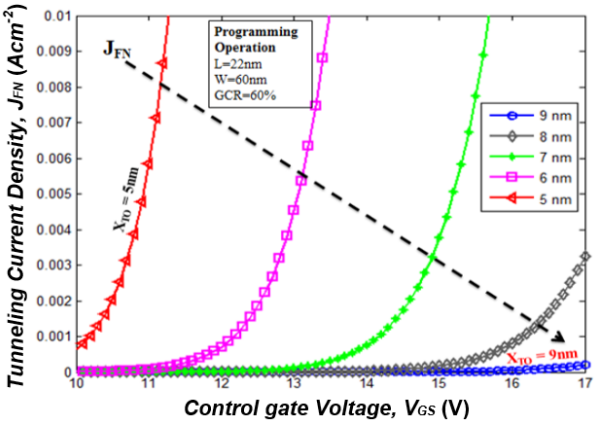


Fig. 2. Fowler-Nordheim (F-N) tunneling current density (J_{FN}) versus Control gate voltage (V_{GS}) for different tunnel oxide thickness (X_{TO}).

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II. CIRCUIT IMPLEMENTATIONS OF PROPOSED BOOST CONVERTER

A. Overall System Architecture

Fig. 3 shows the block diagram of the proposed boost converter. A power stage is composed of off-chip inductor, output capacitor, and two LDMOS switches to endure the voltage stress due to high output voltage. The controller consists of an error amplifier, a comparator, and a SR latch to make a PWM signal (D) while a type-III compensator is applied to ensure stability in a wide output voltage range. The adaptive dead-time generator produces two non-overlap duty signals (D1, D2) according to the switching node voltage signal (Vsw).

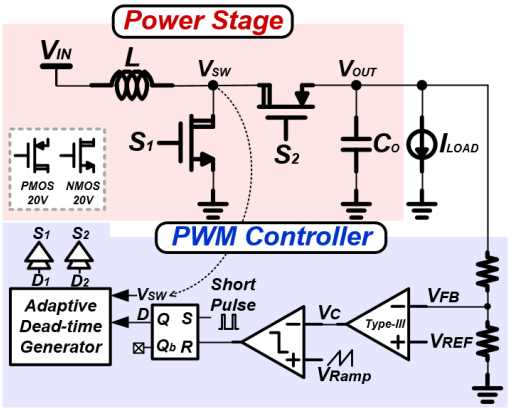


Fig. 3. Block diagram of the proposed boost converter.

B. Compensation Method of Boost Converter

In the DC-DC converter design, a compensator is very important for stable DC voltage regulation. The wrong compensator design causes oscillation of the output voltage, which results in damage or malfunction of the loading block [4].

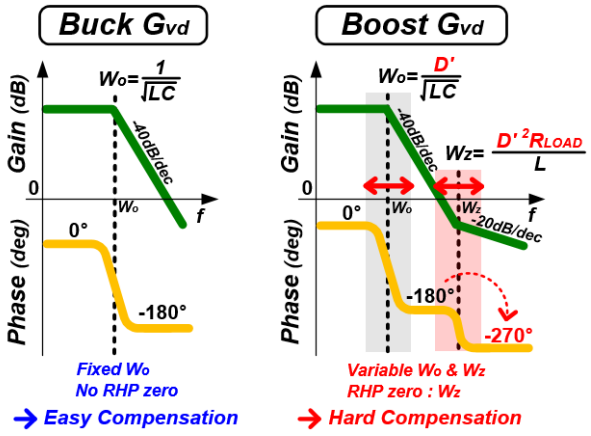
Equations (1) and (2) show the duty-to-output transfer function (*Gvd*) of buck and boost converter, respectively, and Fig.4 shows a bode plot [5].

In the case of buck converter, there is only a resonant pole frequency, w_o, which is determined by the inductor and output capacitor value (L, C) of the converter. This value does not change even if the input or output voltage varies, so

$$G_{vd}(s)_{\text{buck}}=\frac{V_{OUT}}{D}\frac{1}{1+\frac{s}{Qw_o}+\left(\frac{s}{w_o}\right)^2},\quad w_o=\frac{1}{\sqrt{LC}}. \quad (1)$$

$$G_{vd}(s)_{\text{boost}}=\frac{V_{OUT}}{D'}\frac{1-\frac{s}{w_Z}}{1+\frac{s}{Qw_o}+\left(\frac{s}{w_o}\right)^2},$$
$$w_o=\frac{D'}{\sqrt{LC}},\quad w_z=\frac{D'^2R}{L}. \quad (2)$$

In the case of buck converter, there is only a resonant pole frequency, w_o, which is determined by the inductor and output capacitor value (L, C) of the converter. This value does not change even if the input or output voltage varies, so it makes compensator design easy. On the other hand, in the case of boost converter, even if the LC value is fixed, wo can be changed according to the D which is changed by input or output voltage, so it makes compensation difficult. In addition, there is a right half plan (RHP) zero in the boost converter, which deteriorates the stability of the converter because it lowers the phase of the transfer function while the gain increases. Therefore, in the boost converter design, it is required to design the compensator that ensures stability in the whole input and output voltage ranges.



(a) (b)

Fig. 4. Bode plots of duty to output transfer function (*Gvd*), (a) buck and (b) boost converter.

Fig. 5 shows the circuit configuration and the location of pole and zero frequencies of the type-III compensator according to the passive component's value [6]. The type-III compensator is a good method to ensure the stability and obtain the wide loop bandwidth of the dc-dc converter. In this paper, the controller of the proposed boost converter is designed by applying the type-III compensator. The details of design method are as follows:

1. Select the switching frequency f_{sw} and crossover frequency f_c.

$$f_{sw}=1\text{ MHz},\ f_c=32\text{ kHz}. \quad (3)$$

2. Calculate the resonant pole frequency f_o and RHP zero frequency f_{rhp}, and ESR zero frequency f_{esr} in the worst case. The worst case is the condition which the output voltage and load current are maximum.

$$f_o=\frac{D'}{2\pi\sqrt{LC}}=\frac{0.25}{2\pi\sqrt{3.3\text{uH}\cdot10\text{uF}}}=6.9\text{ kHz}. \quad (4)$$

$$f_{rhp}=\frac{D'^2R_{Load}}{2\pi L}=\frac{0.25^2\cdot40}{2\pi3.3\text{uH}}=120\text{ kHz}. \quad (5)$$

$$f_{esr}=\frac{1}{2\pi C_oR_{esr}}=\frac{1}{2\pi10\text{uH}\cdot20\text{m}\Omega}=795\text{ kHz}. \quad (6)$$

3. Determine the required pole and zero frequencies.

$$f_{z1} = 0.6 f_o = 4.1 \text{ kHz}. \quad (7)$$

$$f_{z2} = 1.2 f_o = 8.3 \text{ kHz}. \quad (8)$$

$$f_{p1} = 2 f_{rhp} = 240 \text{ kHz}. \quad (9)$$

$$f_{p2} = f_{esr} = 795 \text{ kHz}. \quad (10)$$

4. Calculate the resistor and capacitor values. The R_2 is selected randomly as the appropriate value for the static power loss of less than 1mW.
Vm is the peak voltage value of the ramp (sawtooth) signal in PWM controller, and X is the ratio of f_o to f_{z1}.

$$R_2 = 1 \text{ M}\Omega. \quad (11)$$

$$C_1 = \frac{1-{}^{f_o}/_{f_{rhp}}}{2\pi f_o R_2} = 22 \text{ pF}. \quad (12)$$

$$R_1 = \frac{1}{2\pi f_{p1} C_1} = 30 \text{ k}\Omega. \quad (13)$$

$$C_2 = \frac{V_{OUT} f_o}{2\pi D' V_m R_2 f_{esr} X f_c} = 600 \text{ fF}. \quad (14)$$

$$R_3 = \frac{1}{2\pi f_{p2} C_2} = 330 \text{ k}\Omega. \quad (15)$$

$$C_3 = \frac{1}{2\pi f_{z1} R_3} = 120 \text{ pF}. \quad (16)$$

Vm is the peak voltage value of the ramp (sawtooth) signal in PWM controller, and X is the ratio of f_o to f_{z1}.

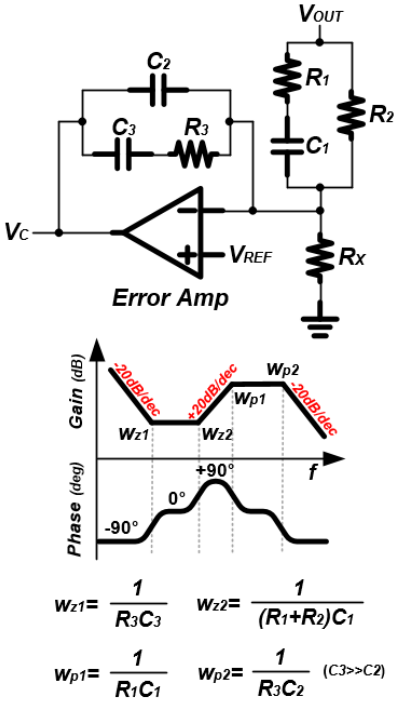
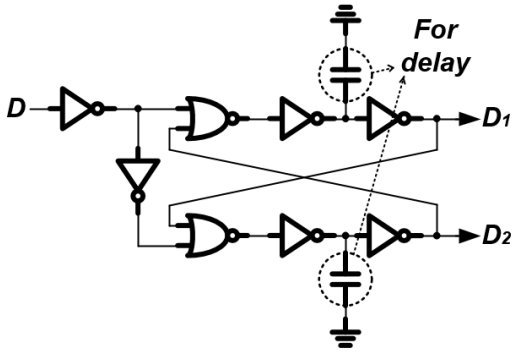


Fig. 5. Type-III compensator.

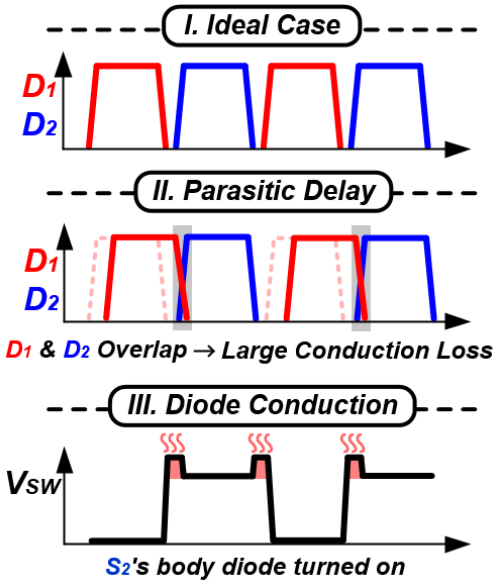
C. Adaptive Dead-time Generator

Fig. 6 shows the structure and issues of the conventional dead-time generator. It generates the dead-time signal by using the delay through the capacitor between the inverter chains [7]. This circuit can be designed very simply, but there are several issues. First, the dead-time signals may overlap due to the parasitic delay that occurs when the logic gate or the generated duty signal (D_1 or D_2) is transmitted to the gate of the power switch. It makes the two power switches to turn-on at same time, resulting in the shoot-through current. It causes the large conduction loss. Second, if the delay due to the capacitor or dead-time is too long, the body diode of S_2 switch is conducted during that time, resulting in conduction loss due to the body diode. Therefore, the conventional dead-time generator has problems that may reduce the overall power efficiency of the converter.

Fig. 7 shows the structure and waveforms of the proposed adaptive dead-time generator. This circuit applies the duty signal, D, made by PWM controller and switching node voltage, V_{SW}, of the boost converter as input signals. M_C is 20V LDMOS, which limits the high switching node voltage, V_{SW} (≥ 5V) to 5V. Since the gate logic consists of 5V CMOS, M_C is needed to protect against high voltage V_{SW}. D_1 and D_2



(a)



(b)

Fig. 6. (a) Structure and (b) issues of conventional dead-time generator.

are the signals applied to the S_1 switch and S_2 switch of the converter, respectively. The operation of the circuit is as follows. When D is low, the converter's S_2 switch is turned on and V_{SW} is V_{OUT}. When D is switched from low to high, D_2 changes from low to high, and the S_2 switch is turned off first. After that, when D_{2D} becomes high and D_1 changes from low to high by delay cell, the S_1 switch is turned on and V_{SW} becomes ground. On the contrary, when D changes from high to low, D_1 first change to low, and the S_1 switch is turned off. In this case, the switching node is floated, so V_{SW} increases due to the inductor current that charges the parasitic capacitor of the switching node. Therefore, $V_{SW,Lb}$ changes from high to low, and D_2 also goes to low, so the S_2 switch is turned on. As a result, the proposed dead-time circuit can generate the adaptive dead-time to prevent the signal overlap and too long dead-time.

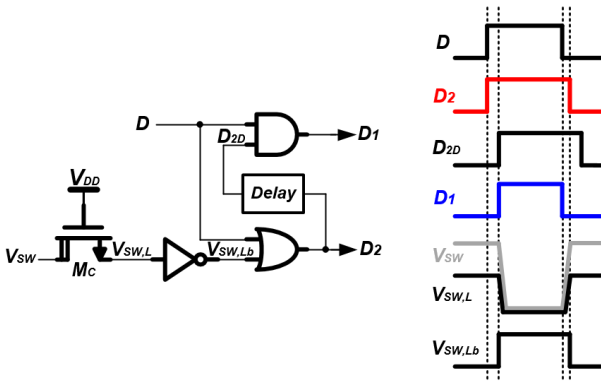


Fig. 7. Proposed adaptive dead-time generator.

III. SIMULATION RESULTS

The proposed boost converter is fabricated in TSMC 0.18um BCD process. Fig. 8 shows the chip micrograph, and the total area occupies 2.675 mm × 2.32 mm. Power stage's off-chip inductor and capacitor values are 3.3uH and 10uF, respectively. The power switch is manufactured in 20V LDMOS and the controller is 5V CMOS. Table I is the summary table of the proposed boost converter. The converter operates at the 5V input voltage and the output voltage's range is 5.5V to 20V. The load current range is from 10mA to 500mA. The proposed converter operates at 1MHz switching frequency, and the simulated peak efficiency is achieved to 93.2%.

The simulated steady-state waveforms are shown in Fig. 9. Fig. 9(a) is when V_{IN}=5V, V_{OUT}=5.5V, I_{LOAD}=0.1A, and Fig. 9(b) is when V_{IN}=5V, V_{OUT}=20V, I_{LOAD}=0.5A. Therefore, the operation of the proposed converter is stable from the minimum output voltage to the maximum output voltage region.

Fig. 10 shows the switching node voltage waveforms of the boost converter. It is the waveforms when operating with conventional dead-time generator and the proposed adaptive dead-time generator. It can be seen that the region where body diode conduction occurs significantly decreased when the proposed dead-time generator is used.

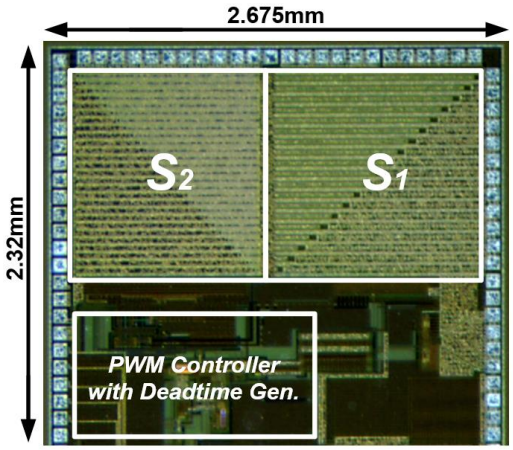
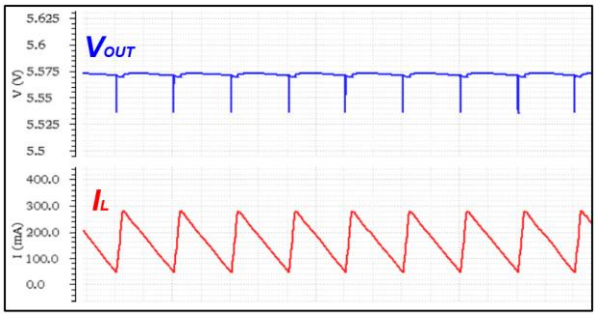
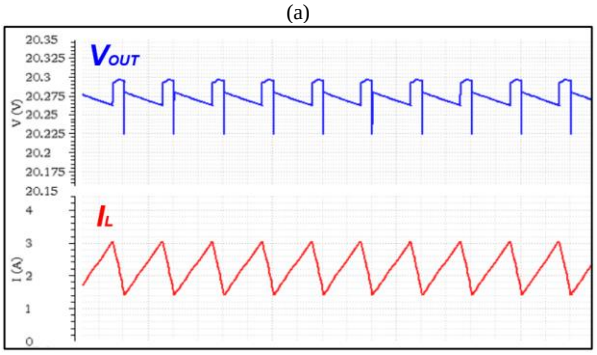


Fig. 8. Chip micrograph.



(a)



(b)

Fig. 9. Simulated steady-state waveforms under (a) V_{IN}=5V, V_{OUT}=5.5V, I_{LOAD}=0.1A, (b) V_{IN}=5V, V_{OUT}=20V, I_{LOAD}=0.5A.

TABLE I. Specifications of the proposed dc-dc boost converter

Parameter	Value
Process	0.18um BCD
Input Voltage	5V
Output Voltage	5.5 – 20V
Inductor (uH)	3.3
Output Capacitor (uF)	10
Load Current (mA)	10 – 500
Switching Frequency	1 MHz
Peak. Efficiency	93.2%

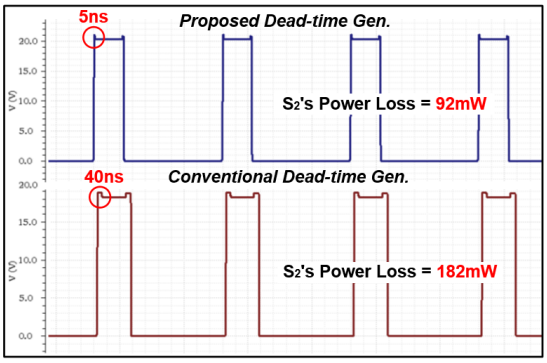


Fig. 10. Waveforms of switching node voltage under V_{IN}=5V, V_{OUT}=20V, I_{LOAD}=0.5A.

Fig. 11 and Fig. 12 show the simulated bode plots of the proposed boost converter loop according to the different output voltage and load current. The phase margin (PM) of 40 degrees or higher was obtained under whole output voltage and load current conditions, so the proposed boost converter can operate stably in very wide operating range.

Fig. 13 shows the simulated power efficiency of the proposed boost converter according to the different load currents and output voltages. Peak efficiency is achieved 93.2% under V_{IN}=5V, V_{OUT}=5.5V and I_{LOAD}=350mA.

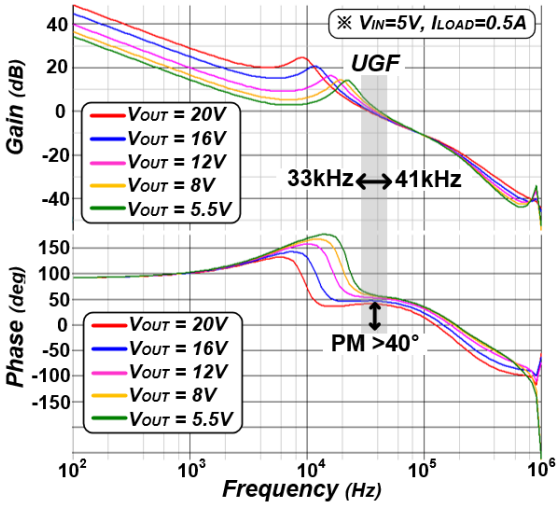


Fig. 11. Bode plot of the loop under different output condition.

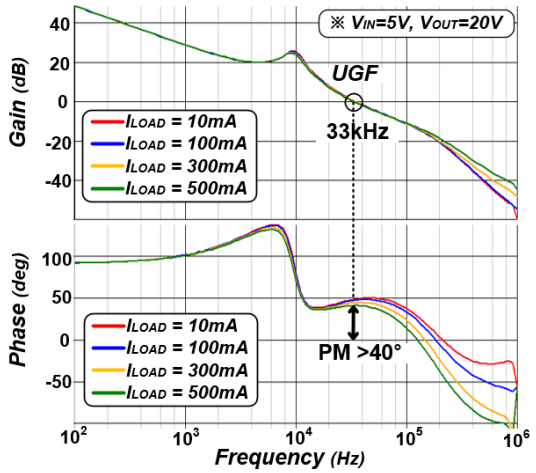


Fig. 12. Bode plot of the loop under different load condition.

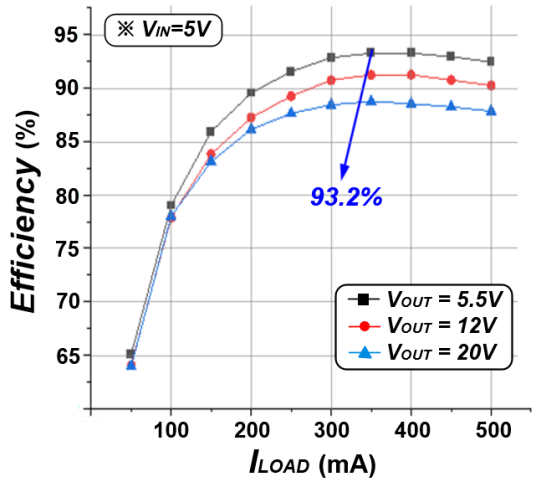


Fig. 13. Simulated efficiency with different V_{OUT} under different I_{LOAD}.

IV. CONCLUSION

In this paper, a voltage mode PWM DC-DC boost converter with adaptive dead-time generator is presented for solid-state drives application. The type-III compensator is implemented for stable operation of the boost converter in a wide output voltage range. In addition, the proposed adaptive dead-time circuit generates the dead-time according to switching node voltage signal of the boost converter, it mitigates the power dissipation caused by the signal overlap or body diode conduction. The proposed boost converter is fabricated in 0.18um BCD process, operating at 1MHz switching frequency, and 5V supply voltage. Simulation results show that it achieves the phase margin of 40 degrees or more under the whole output voltage and load current conditions. Therefore, the proposed boost converter can operate stably under the output voltage range of 5.5-20V. And the peak efficiency is achieved to 93.2%. As a result, the proposed boost converter can be a good candidate for solid-state drives application that requires high efficiency and a wide output voltage range.

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